Nanoimprint System Alignment and Overlay Improvement for High Volume Semiconductor Manufacturing

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Abstract

Imprint lithography is an effective and well-known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In this work, improvements to the alignment system, together with the High Order Distortion Correction (HODC) system have enabled better distortion and overlay results. On test wafers, XMMO of 3.2nm and 2.8nm in x and y respectively was demonstrated. There is also an opportunity to further improve results by applying wafer chucks with better flatness specifications. Further advances have also been made through the application of a multi-wavelength alignment strategy. Finally, we discuss how computational methods can enhance NIL productivity and reduce the number of learning cycles.

Keywords: nanoimprint lithography, NIL, alignment, overlay, XXMO, TTM, HODC, throughput, simulation

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.
Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In 2018, Hiura et al. reported a mix and match overlay (MMO) of 3.4 nm and a single machine overlay (SMO) across the wafer was 2.5nm using an FPA-1200 NZ2C four station cluster tool. These results were achieved by combining a magnification actuator system with a High Order Distortion Correction (HODC) system, thereby enabling correction of high order distortion terms up to K30.

The purpose of this paper is to describe the improvements to alignment, overlay and throughput in order to meet specifications for advanced memory devices. We also introduce a section on computational models that are being developed for NIL in order to enhance productivity and reduce the number of learning cycles.

2. Alignment and Overlay

a. Overlay Functionality for Nanoimprint Lithography

In order to address overlay in a Nanoimprint system, there are many factors that need to be considered, some of which are quite different than what is required for photolithographic tools. Generally speaking, the process can be broken down into two categories; Alignment and Overlay (See Figure 1.) In this paper we separately address alignment and overlay, as described in the next two sections of the paper.

![Figure 1. Factors that influence overlay in a nanoimprint tool](https://www.spiedigitallibrary.org/conference-proceedings-of-spie)
b. Through The Mask (TTM) Alignment System

The NZ2C system employs a Through The Mask (TTM) alignment system as shown in Figure 2a. First order terms are passed through Moiré marks on the mask and wafer with a sensitivity on the order of 1nm.

Figure 2. a) Through The Mask (TTM) alignment system, b) Signal blooming (highlighted in yellow) was reduced using a dipole/polarized illuminator, c) comparison of the TTM measurement versus results on an overlay tool before and after improvement.

Improvements to the alignment system were realized by moving to a dipole illumination system and optimizing the intensities of multiple wavelengths in the TTM system. The results are shown in Figures 2b and 2c. Figure 2c shows the reduction in signal blooming after applying a dipole/polarized illuminator. Figure 2c shows a comparison of the TTM measurement versus results on an overlay tool before and after optimization. The 3-sigma error has been reduced from 3.6nm to 1.4nm.

c. Overlay and High Order Distortion Correction (HODC) System

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and lens during the exposure process. A different approach is required for the imprint tool in order to do high order distortion controls (HODC). HODC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis

Heat input on a field by field basis is realized through the use of DMD array which imparts heat through the mask onto a stepper field of a wafer. The basic operation of the system, along with initial results has been described in previous publications.\textsuperscript{11,12} The system is shown schematically in Figure 3.
Recent efforts have been driven by applying low friction coatings to the wafer chucks and improving chuck flatness as shown in Figure 4. The combination of the HODC system together with flatter, low friction chucks, enables better overlay. The graph on the right of Figure 4 illustrates a 22 percent improvement in performance.
d. Test Wafer Results

The TTM and HODC systems were applied to test wafers and the results are reported in Figure 5 and 6. Figure 5 depicts Cross Matched Machine Overlay (XMMO) on an existing level patterned with an ASML 1950 ArF immersion tool. A total of 84 fields were measured, including twelve points per field. The results are an average across twenty-five wafers. XMMO of 3.2nm and 2.8nm mean plus three sigma was achieved in x and y, respectively.

![Cross Matched Machine Overlay](image)

Figure 5. XMMO using an FPA-1200 NZ2C imprint system. XMMO of 3.2nm and 2.8nm mean plus three sigma was achieved in x and y, respectively

Similarly, Figure 6 depicts NIL Mix and Match Overlay (NIL MMO) on an existing level patterned with the FPA-1200 NZ2C tool. A total of 84 fields were measured, including twelve points per field. The results are an average across three wafers. NIL MMO of 2.2nm and 2.4nm mean plus three sigma was achieved in x and y, respectively. Residual distortions were 0.7nm, mean plus three sigma.

![NIL to NIL 1st Layer after Si etching process](image)

Figure 6. NIL MMO using an FPA-1200 NZ2C imprint system. MMO of 2.2nm and 2.4nm mean plus three sigma was achieved in x and y, respectively
3. Computational Improvements

Newly developed is a resist drop fill simulator designed to minimize fill time (thereby increasing throughput) and reduce non-fill defects.\textsuperscript{13} The model must account for the dissipation of trapped gas between drops that causes non-fill defects. An example is shown in Figures 7. In Figure 7, two different drop patterns (Parameter sets A and B) were both simulated and run on the imprint tool. The imprint process was stopped before completion of the process, so that the model and simulations could be compared. The colored points in each graph indicate non-fill. There is good agreement in the non-fill defect pattern for each case. Further simulations on an optimized resist drop pattern show non-fill defectivity trending to zero after a fill time of 1.2 seconds, in excellent agreement with actual fill time results.

![Parameter set A](image1.png) ![Parameter set B](image2.png)

**Figure 7.** Comparison of non-fill defectivity for the drop simulation package and actual fill time results.

This newly developed computational fluid dynamics model is also able to predict thickness and slope of the formed resist after imprint.\textsuperscript{13} This capability may play an important role in distortion correction as explained below.

There is an additional distortion term that must also be addressed for the case of nanoimprint lithography. NIL drop patterns are typically designed to minimize resist fill time and create a uniform residual layer beneath the resist pattern. However, it is important to recognize that there are both long wavelength flatness errors coming from the wafer chuck and existing pattern topography from previously patterned levels that cause out of plane errors. When the mask comes in contact with the resist on the wafer, these out of plane errors can then induce mask bending, resulting in an additional distortion term.

To minimize this distortion, a Drop Pattern Compensation (DPC) Model has been implemented to minimize the added distortion terms. As an example (Figure 8), improvements can be realized with a favorable mask bending shape. In this case, mask bending compensates the non-flatness induced overlay errors to achieve a near-zero bending strain mismatch.

![Mask](image3.png)

**(b) After contact**

**Figure 8.** Schematic of the DPC process

Cherala et al. results are presented for a wafer in which the overlay errors within a field were reduced from 5.4nm to 3.4nm, 3 sigma.\textsuperscript{14} Additional improvements to the DPC model can be found in Reference 15.
Canon has also started to apply machine learning to enhance process robustness, leading to more repeatable results from wafer to wafer. This has been accomplished by analyzing both the phase spectrum and power spectrum of the Moiré signal, and comparing the results to off-line metrology tools, using a lightweight neural network model (See Figure 9.). The result is enhanced process robustness with a real time process time of just 1msec. We have just starting the learning process and have quickly seen an improvement to better than 2.0nm. Note the good agreement between the predicted error and measured error. We expect to reduce this error by half as more jobs are fed through the tool this year.

Figure 9. Lightweight neural network model applied to reduce alignment errors.

3. Throughput

Throughput is one of the key contributors to cost of ownership. In this section, we discuss how a throughput of up to 100 wafers per hour can be achieved.

a. Throughput Overhead

Previous papers have discussed throughput breakdown in detail. Overheads to the imprint TAKT time have been reduced by applying a multi-field dispense strategy, as opposed to dispensing and imprinting in a sequential fashion. The reduction in overhead is on the order of .24 seconds, resulting in an increase in throughput to 90 wafers per hour. Figure 9 shows that non-fill defectivity to nominally the same for the multi-field approach.

Figure 10. Defect inspection result comparison. The multi-field dispense results are comparable in defectivity to the sequential imprinting method.
b. Throughput and Drop Volume

Many factors influence resist spread. The list includes mask pattern, drop pattern, resist properties, wafer topography, drop volume and gas dispersion. In this section, we briefly discuss drop volume. Smaller droplet volume means drops can be placed closer together, resulting in faster coalescence and trapped gas dissipation. Figure 11 shows the total resist spread time as a function of drop volume. At a drop volume, resist spread is completed in 1.0 seconds.

![Drop Volume vs Spread Time](image)

Figure 11. Comparison of non-fill defectivity for the drop simulation package and actual fill time results.

4. Conclusions

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported. In this work, improvements to the alignment system, together with the High Order Distortion Correction (HODC) system have enabled better distortion and overlay results. On test wafers, XMMO of 3.2nm and 2.8nm in x and y respectively was demonstrated across a 25 wafer lot. Further improvements to the align system have been realized with a multi-wavelength strategy and machine learning. Throughput up to 100 wafers per hour was realized by decreasing the resist drop volume. Finally, we also introduced a section on computational models that are being developed for NIL in order to enhance productivity and reduce the number of learning cycles.

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References