

# Addressing Nanoimprint Lithography Mix & Match Overlay Using Drop Pattern Compensation

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## Abstract

Imprint lithography is a promising technology for replication of nano-scale features. For semiconductor device applications, Canon deposits a low viscosity resist on a field by field basis using jetting technology. A patterned mask is lowered into the resist fluid, which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Overlay budgets play a large role in defining production readiness. As an example, DRAM devices require overlay on the order of 15-20% of the half pitch. Canon uses a through the mask (TTM) alignment system to measure a Moiré image anywhere in the field. This system can also record alignment errors of all fields and all marks. The data collected by the TTM system correlates very closely with an Archer measurement tool. In addition, a High Order Distortion Correction (HODC) system, which applies a heat input on a field by field basis through the use of a DMD array has been combined with magnification actuators to correct high order distortion terms up to K30.

There is an additional distortion term that must also be addressed for the case of nanoimprint lithography. NIL drop patterns are typically designed to minimize resist fill time and create a uniform residual layer beneath the resist pattern. For device wafers, however, it is important to recognize that there are both long wavelength flatness errors coming from the wafer chuck and existing pattern topography from previously patterned levels that cause out of plane errors. When the mask comes in contact with the resist on the wafer, these out of plane errors can then induce mask bending, resulting in an additional distortion term.

To minimize this distortion, a Drop Pattern Compensation (DPC) Model has been implemented to minimize the added distortion terms. In this paper we present an updated study and report on nanoimprint mix and match overlay improvements using DPC. In addition, we describe how the mode array and peak to valley thickness of the resist impacts distortion correction.

**Keywords:** nanoimprint lithography, NIL, overlay, HODC, drop pattern compensation, DPC

## 1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features.<sup>1,2</sup> Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.<sup>3-9</sup> The patterned mask is lowered into the fluid, which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary,

thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste, leads to a cost model that is very compelling for semiconductor memory applications.

With respect to throughput, Hamaya et al. recently reported a multi-field dispense strategy to increase throughput to 90 wafers per hour for an NZ2C NIL four station tool.<sup>11</sup>

On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photo masks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was recently reported to have a defectivity of only 0.04/cm<sup>2</sup> as measured by a Lasertec tool with 50 nm sensitivity.<sup>12</sup> Presently, Ichimura et al. have exceeded the targets for both CDU and IP. In addition, master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20nm have been fabricated.<sup>13</sup>

Overlay budgets play a large role in defining production readiness. As an example, DRAM devices require overlay on the order of 15-20% of the half pitch. Canon uses a through the mask (TTM) alignment system to measure a Moiré image anywhere in the field. This system can also record alignment errors of all fields and all marks. The data collected by the TTM system correlates very closely with an Archer measurement tool.

In addition, a High Order Distortion Correction (HODC) system, which applies a heat input on a field by field basis through the use of a DMD array has been combined with magnification actuators to correct high order distortion terms up to K30. Hiura et al. applied the system to demonstrate cross matched machine overlay (XMMO) and single machine overlay (SMO) of 3.4nm and 2.5nm respectively.<sup>14</sup> A schematic of the various methods used to address alignment and distortion are shown in Figure 1. HODC system is shown in Figure 1

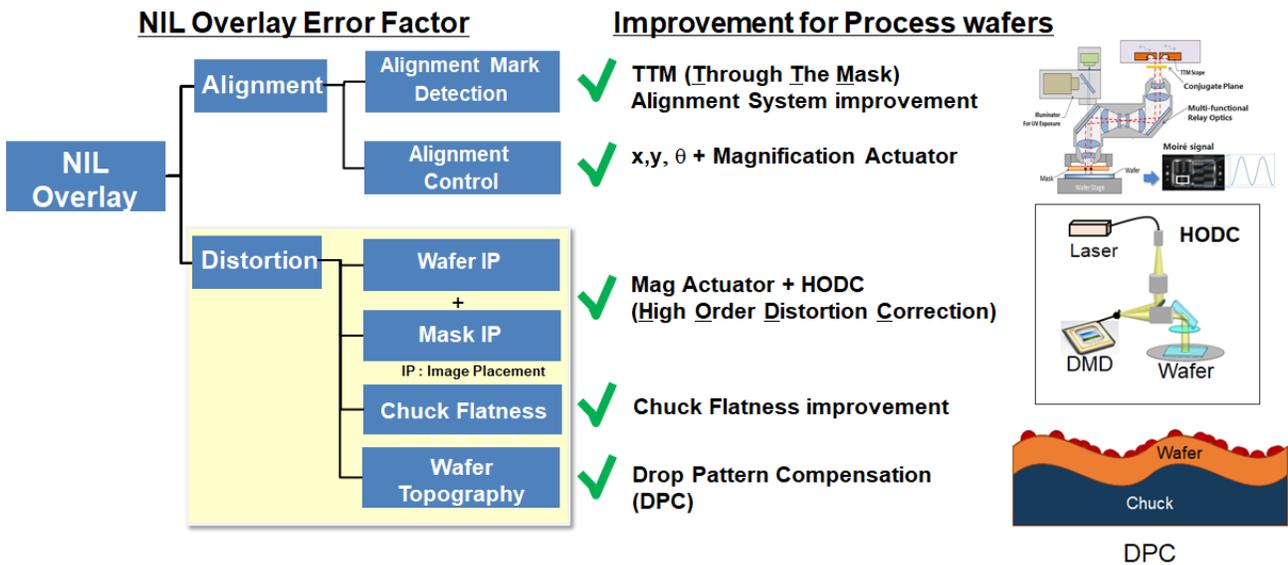


Figure 1. Methods for NIL to address alignment and distortion

There is, however, an additional distortion term that must also be addressed for the case of nanoimprint lithography. NIL drop patterns are typically designed to minimize resist fill time and create a uniform residual layer beneath the resist pattern. For device wafers, however, it is important to recognize that there are both long wavelength flatness errors coming from the wafer chuck and existing pattern topography from previously patterned levels that cause out of plane errors. When the mask comes in contact with the resist on the wafer, these out of plane errors can then induce mask bending, resulting in an additional distortion term.

To minimize this distortion, a Drop Pattern Compensation (DPC) Model has been implemented to minimize the added distortion terms. DPC was introduced last year at this symposium and cross matched overlay results to an ArF immersion

scanner were reported.<sup>15</sup> In this paper we present an updated study and report on nanoimprint mix and match overlay improvements using DPC. In addition, we describe how the mode array and peak to valley thickness of the resist impacts distortion correction.

## 2. Origin of Out of Plane Errors

The NIL process has five general steps to be completed. i) Dispense a low viscosity UV curable resist onto the wafer. ii) Align the mask to the dispensed drops to minimize overlay error. iii) Contact the mask with the wafer. iv) Wait for capillary fill and UV expose. v) Safely separate the mask without defects. During the NIL process, many technological efforts to minimize overlay errors are made, such as a through the mask (TTM) alignment system, a magnification/shape control system (MSCS), and a high order distortion correction system (HODC). These systems have demonstrated that in-plane overlay errors can be reduced significantly. However, there exists an additional distortion term which cannot be resolved by these systems. Although the NIL process requires a mask to remain perfectly flat in step 4, during the actual process, out-of-plane distortion is observed. One topographical cause of this distortion is wafer and wafer chuck flatness; another is existing patterned wafer topography.

Figure 2 illustrates the mask and wafer conforming process for each topographical mode. Since a resist layer thickness is uniform across a NIL stepper field, the mask inevitably follows wafer topography. Figure 2 (a) and (b) show the mask and wafer geometry before the mask comes into contact. In Figure 2 (c), flatness errors of the wafer and wafer chuck result in mask bending. This out-of-plane distortion results in bending strain mismatch at the mask-wafer interface, causing in-plane overlay (OL) error, as depicted by the direction of the arrows at the interface. Figure 2 (d) shows mask bending due to patterned wafer topography with half-wavelength on the order of 1 mm or larger, which also contributes to OL error.

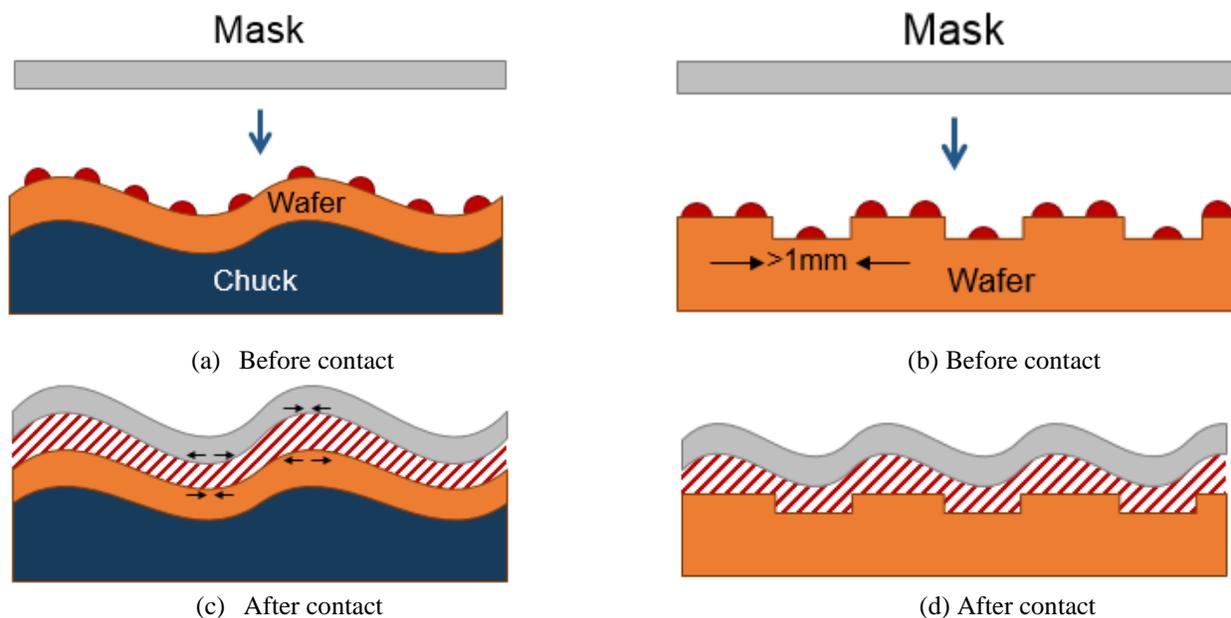


Figure 2. J-FIL: Conformal Process

An example due to topography induced OL distortion is shown in Figure 3.<sup>15</sup> The OL distortion images represent two sets of data: on a flat wafer and a programmed topography wafer (~20nm deep trench) shown in the middle image. Compared to a flat wafer, the OL distortion vectors align normal to the boundary of the wafer trench, which causes a 3.5nm OL degradation in the y-direction.

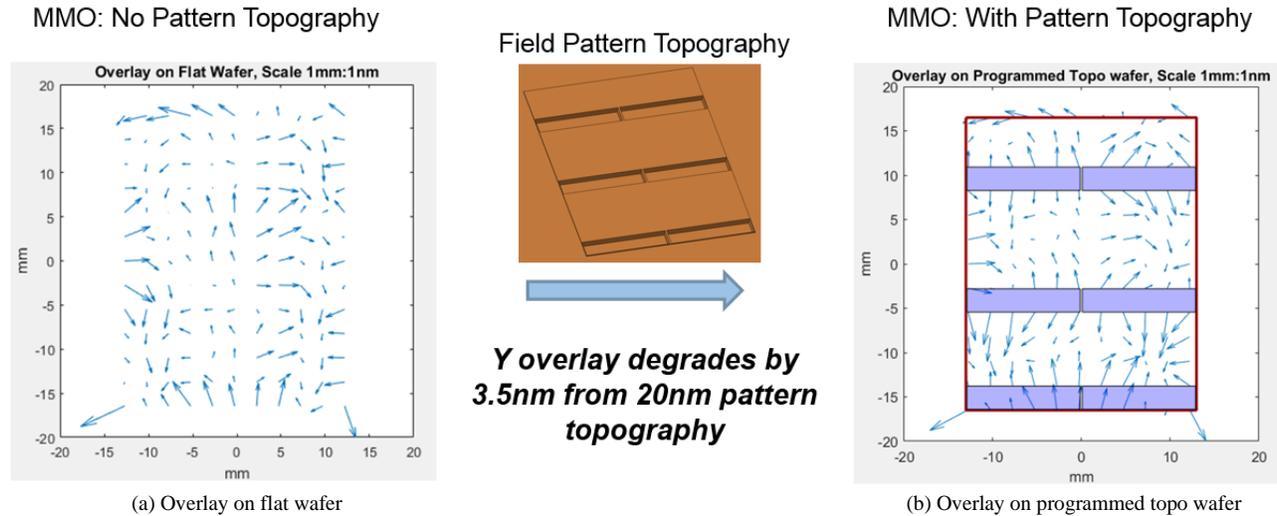


Figure 3. Topography induced OL distortion

### 3. Drop Pattern Compensation Model

In this study, resist drops are used to induce favorable mask bending in order to compensate overlay errors, such as non-flatness induced overlay errors to achieve a near-zero bending strain mismatch (See Figure 4.)

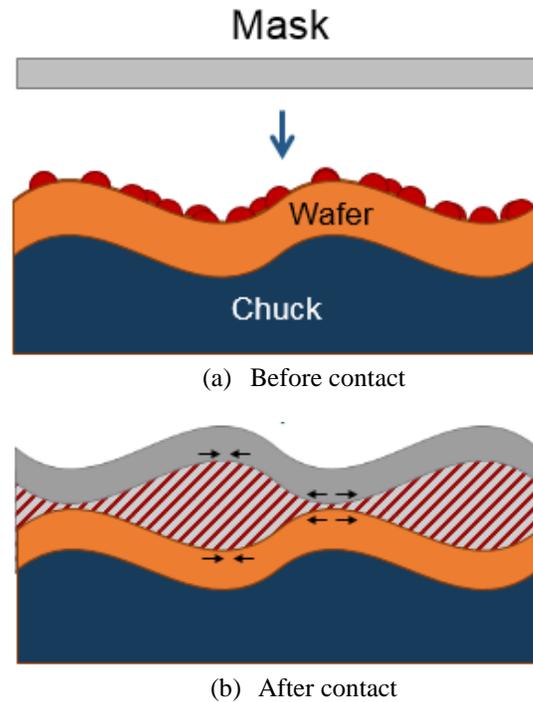


Figure 4. Drop Pattern for Favorable Mask Bending

### a. Model Basics

A classic plate bending model is used to capture chucked wafer topography as shown in Figure 5. From a geometric perspective, in-plane distortions ( $\Delta x$ ,  $\Delta y$ ) are calculated from the out of plane displacement ( $z(x,y)$ ) by relating them via the local slope:

$$\Delta x = \frac{t}{z} \frac{\partial z}{\partial x}; \Delta y = \frac{t}{z} \frac{\partial z}{\partial y}, \text{ where } t \text{ is mask thickness.}$$

Additionally, once in-plane distortions (i.e., OL distortions) are measured, out of plane displacement (i.e., the mask bending shape that follows the wafer topography) can be estimated from the equations. This model agrees well with finite element analysis and was also verified with interferometer (Zygo) flatness measurements.

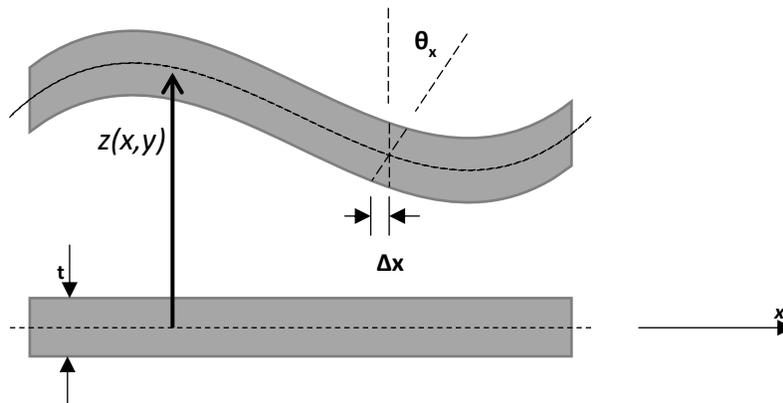


Figure 5. Plate bending model.

To estimate the mask shape from OL data, out of plane distortion needs to be defined using basis functions. Since the NIL pattern is defined within a rectangular domain (~26mm x 33mm) and topography of the wafer is a mostly periodic pattern, 2D Fourier functions are used in this study. A linear combination of basis functions is used to estimate the mask bending shape.

$$z(x, y) = \sum_{m,n=0}^{\infty} \left[ \left( a_{mn} \cos \frac{n\pi x}{L} \cdot \sin \frac{m\pi x}{H} \right) + \left( b_{mn} \cos \frac{n\pi x}{L} \cdot \cos \frac{m\pi x}{H} \right) \right] + \left[ \left( c_{mn} \sin \frac{n\pi x}{L} \cdot \sin \frac{m\pi x}{H} \right) + \left( d_{mn} \sin \frac{n\pi x}{L} \cdot \cos \frac{m\pi x}{H} \right) \right]$$

Where;

- a, b, c, d are Fourier coefficients
- m, n are the number of basis modes
- L is half width of the imprint domain
- H is half height of the imprint domain

Figure 6 illustrates a NIL stepper field and selected two-dimensional mode shapes for that field. The mode shapes in Figures 6 (b) – (f) were generated from the Fourier basis functions by varying m and n.

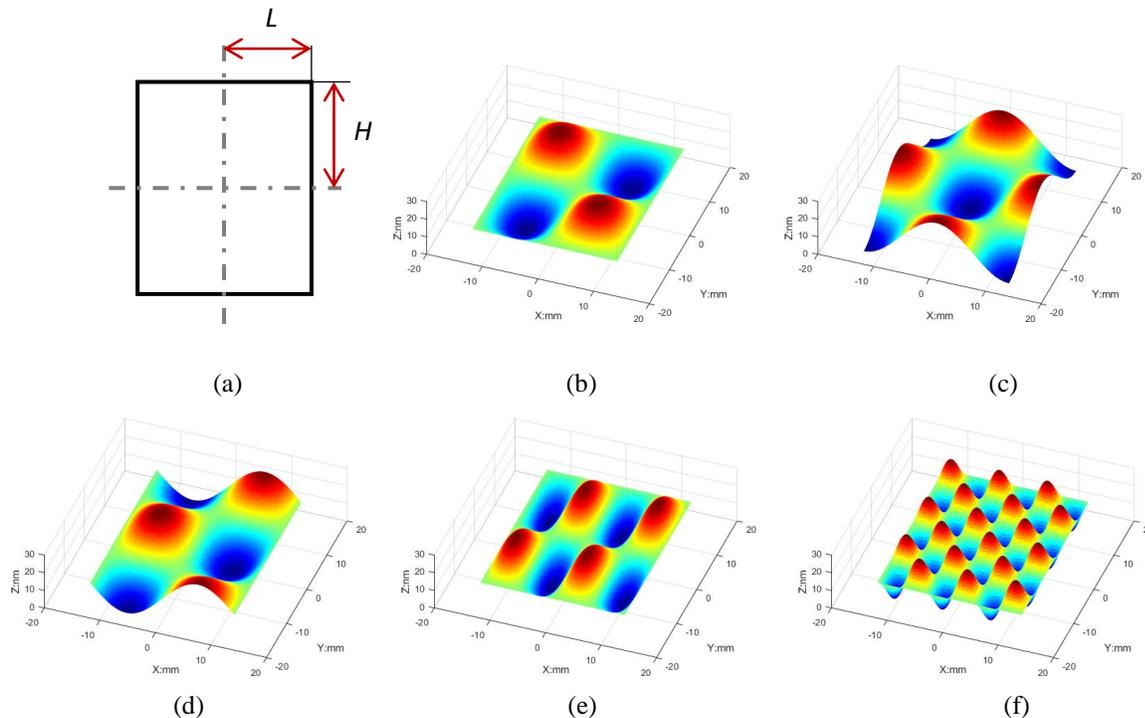


Figure 6. (a) NIL stepper field and (b)-(f) examples of mode shapes of 2D Fourier function

## 4. Results

### a. NIL mix and match overlay results

The performance of drop pattern compensation (DPC) is evaluated using device-like wafers. First, a wafer is imprinted using an initial drop pattern which is created for a uniform resist layer. Next, the alignment and process signatures are removed from the OL data gathered from the initial imprint step. The mask bending model can then be applied to the residual distortion, which contains the topography induced distortion, to obtain the wafer topography map. Based on the wafer topography map, a new optimized drop pattern is generated using a drop generation algorithm developed by Canon, compensating for the topography induced OL distortion. Then the DPC process is repeated until the OL distortion target meets specification. Figure 7 shows the DPC process flow.

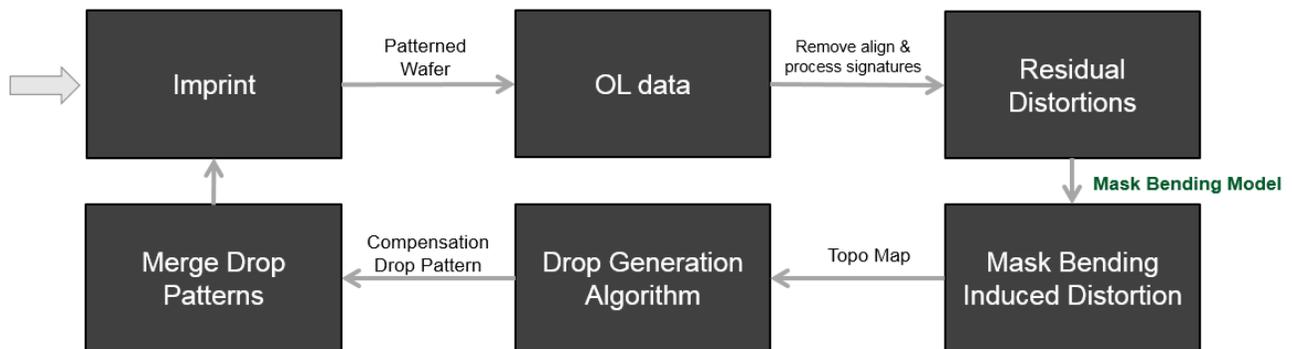


Figure 7. DPC Process Flow

An example of the model is shown in Figure 8, as applied to NIL mix and match overlay. Figure 8a reports the improvement to a full field, in which the original distortion error of 1.50nm was reduced to 1.03nm. Similarly, Figure 8b reports the improvement to a partial field, in which the original distortion error of 3.81nm was reduced to 3.00nm. Across the entire wafer, residual errors in the full field were reduced to less than 1.8nm and residuals in the partial fields were reduced to less than 3.2nm

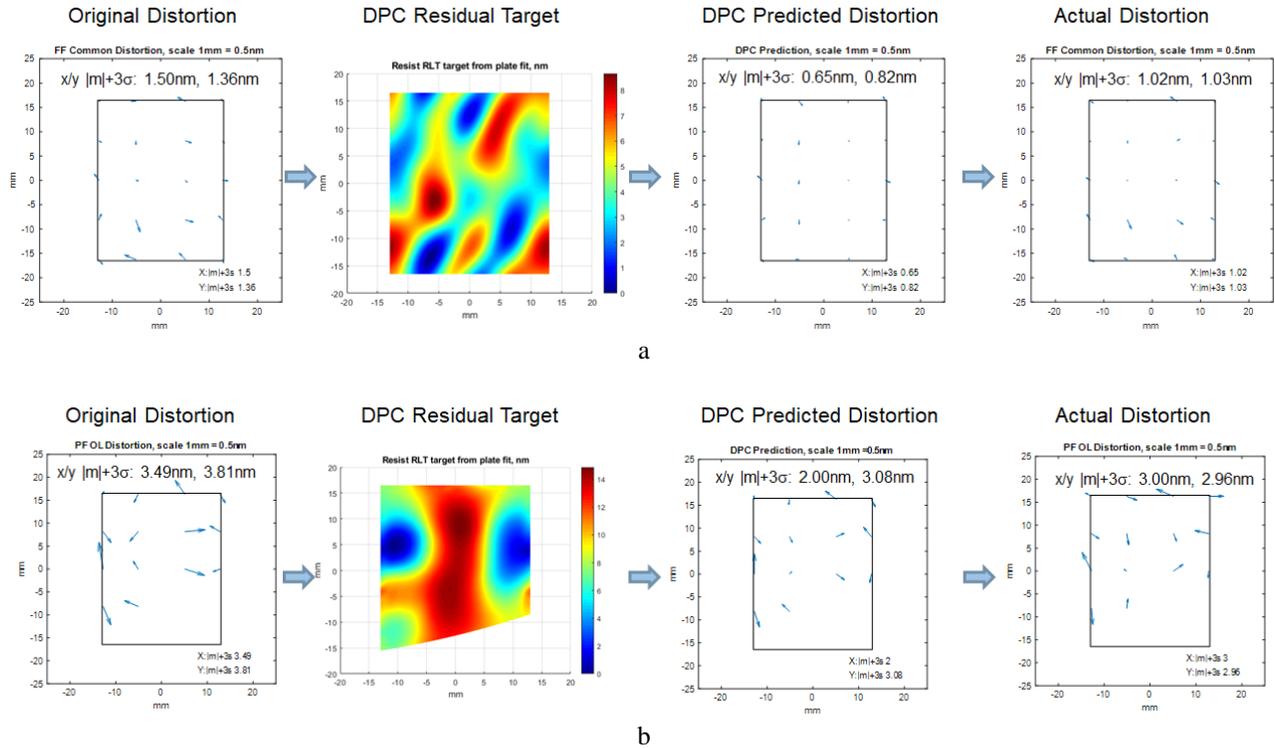


Figure 8. a) Drop compensation applied to a full field on a NIL mix and match overlay test wafer. Residual errors were reduced from 1.5nm to 1.03nm. b) Drop compensation applied to a partial field on a NIL mix and match overlay test wafer. Residual errors were reduced from 3.81nm to 3.00nm

### a. DPC functionality and analysis

A follow up study was run to understand how the number of modes influences image placement. Five different cases were studied: 1x1, 1x2, 2x2, 2x3 and 3x3. Figure 9 reports both the predicted image placement and measured image placement shift as a function of mode. It is clear that as number of modes increases, the measured image placement decreases.

It is likely that the higher frequency modes require a higher energy state which is more unstable, leading to a redistribution of fluid and a decrease in image placement correction. To better understand the behavior, an experiment was run to understand the impact of peak-to-valley resist thickness on image placement correction. We define an Efficiency Ratio (ER) as the percentage of the tested distortion over the estimated distortion as shown in Equation 1 below:

$$ER(\%) = \frac{\text{Tested Distortion}}{\text{Estimated Distortion}} \times 100 \tag{1}$$

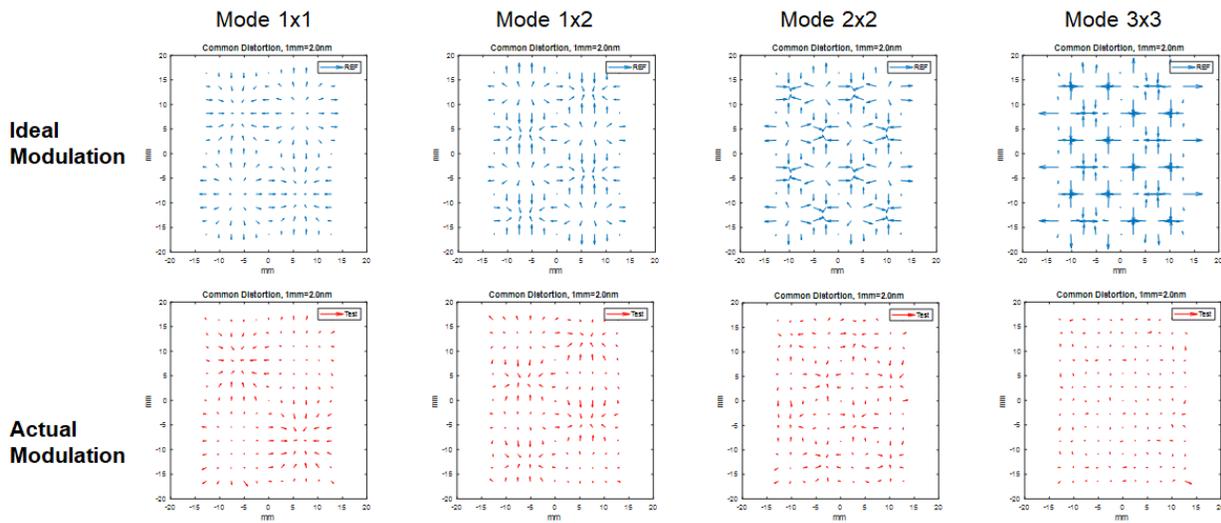


Figure 9. A comparison between the estimated image placement modulation and the actual modulation as a function of the number of modes.

The results of the study are shown in Figure 10, where the Efficiency Ratio is plotted as a function of peak-to-valley resist thickness. It is clear that an increase in peak-to-valley thickness improves the efficiency ratio up until the 3x3 mode.

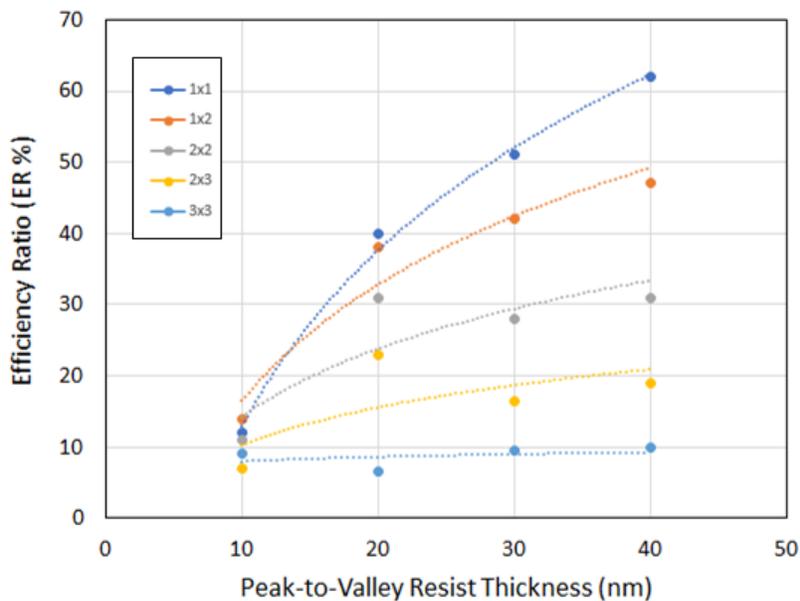


Figure 10. Efficiency Ratio as a function of peak-to-valley resist thickness. Five different modes and four different thickness were studied.

To better understand the impact of peak-to-valley resist thickness on actual distortion correction, a final experiment was run in which two different peak-to-valley resist thicknesses (35nm and 50nm) were applied to a device test wafer (Figure 11). Correction fits were generated, and the final overlay errors were mapped. The starting distortion was 3.4nm

and 5.0nm in x and y, respectively. After correction, the 50nm peak-to-valley resist map was more effective in correcting the distortion errors.

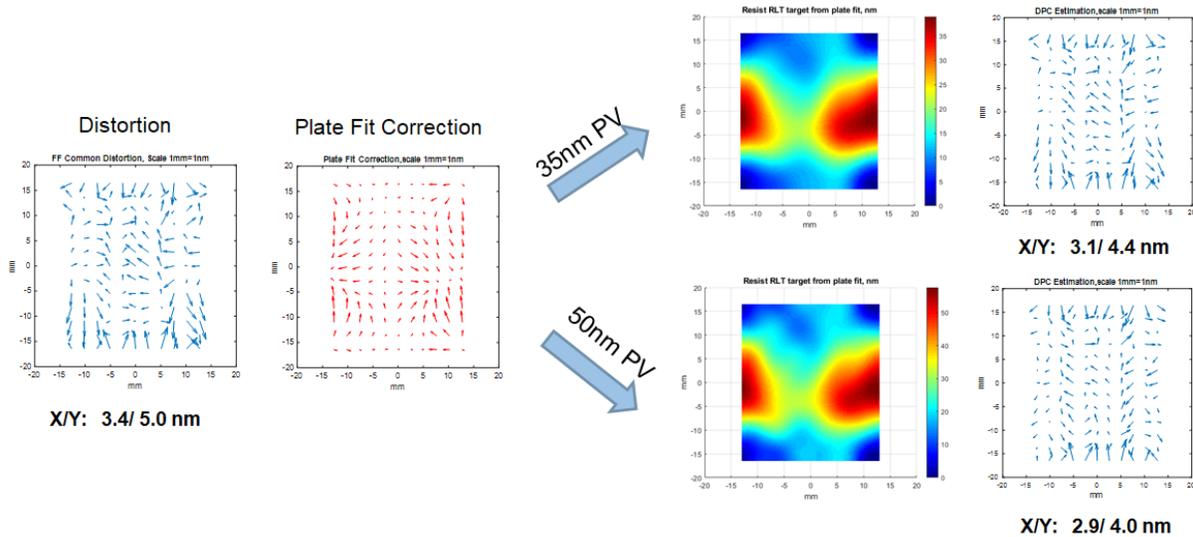


Figure 11. Two different peak-to-valley resist thicknesses (35nm, 50nm) were applied to a device test wafer. Correction fits were generated, and the final overlay errors were mapped. The starting distortion was 3.4nm and 5.0nm in x and y, respectively. After correction, the 50nm peak-to-valley resist map was more effective in correcting the distortion errors.

It should be noted that there are trade-offs in the NIL process when using thicker residual films. Thicker films make a standard subtractive pattern transfer process more challenging, and it likely that a reverse tone pattern transfer process will be needed for most DPC cases.<sup>16</sup>

## 5. Conclusions

Drop pattern compensation (DPC) was developed to address out of plane distortion errors for NIL in order to obtain the best possible overlay results. DPC can correct for both pattern topography and flatness induced OL distortions and is complementary with HODC technology. As a result, it is possible to use DPC to address:

- Chuck induced errors
- Pattern induced distortions
- Grid distortion errors from the scanner
- Stress induced distortion from previous levels
- For NIL, DPC can address mask bending induced overlay errors

In this work, DPC was applied to a NIL mix and match case and for full fields, overlay errors were reduced about one nm. DPC functionality was also examined as a function of mode and peak-to-valley resist thickness. We observed that higher nodes are less effective in correcting distortions unless thicker peak-to-valley thicknesses are applied.

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