Invited Paper

Lithography Today: Challenges and Solutions across a Diverse Market

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Abstract

In 1970, Canon introduced its PLA mask aligner tool for the patterning of features on the order of 10 microns. Wafer sizes at the time were on the order of 50 to 75 mm, and circuitry was relatively simple. Since this time, the device landscape and pattern requirements have changed significantly over the last 50 years as has the markets that are served. Sensors and power devices are still made on relatively small wafers, while the integrated circuit manufacturing has standardized largely on 300mm wafers at various resolutions depending on devices or packaging. Displays are manufactured on much larger glass substrates with higher resolution mobile displays on Gen 6 substrates with large television displays up to Gen 10 which are several meters square.

Canon has focused on providing a wide range of lithography equipment to cover the complete needs of our customers. From launching the first proximity mask aligners in 1970, in accordance with Moore's law, the lithography equipment has evolved in order to increase the degree of integration of semiconductor devices and reduce the critical dimensions of the devices. As for flat panel display lithography equipment, a mirror projection exposure tool, the MPA was introduced in the early 1980s.

In recent years, i-line lithography equipment has been used for advanced packaging, specifically Fan Out Wafer Level Packaging interposers due to the demand for ultra-dense packaging for smartphones and wearables.

Most recently Canon has developed a nanoimprint solution for the patterning of advanced memory devices. Imprint lithography is an effective and well-known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment.

In this paper we review the Canon product line and describe how it is being used to address semiconductor patterning, packaging and flat panel display manufacturing.

Keywords: lithography, photolithography, nanoimprint lithography, NIL, alignment, overlay, throughput

1. Introduction

The year 2020 is an important year for Canon. In addition to the Olympic Games planned for the summer of 2020, 2020 represents the fiftieth anniversary of Canon's lithography equipment business, In 1970, Canon introduced its PLA mask aligner tool for the patterning of features on the order of 10 microns. Wafer sizes at the time were on the order of 50 to 75 mm, and circuitry was relatively simple.

Since this time, the device landscape and pattern requirements have changed significantly over the last 50 years as has the markets that are served. The diversity of the market and the required lithographic equipment is illustrated in Figure 1, with the required resolution plotted against the size of the device substrate. Sensors and power devices are still made on relatively small wafers, while the integrated circuit manufacturing has standardized largely on 300mm wafers at various resolutions depending on devices or packaging. Displays are manufactured on much larger glass substrates with higher resolution mobile displays on Gen 6 substrates with large television displays up to Gen 10 which are several meters square.

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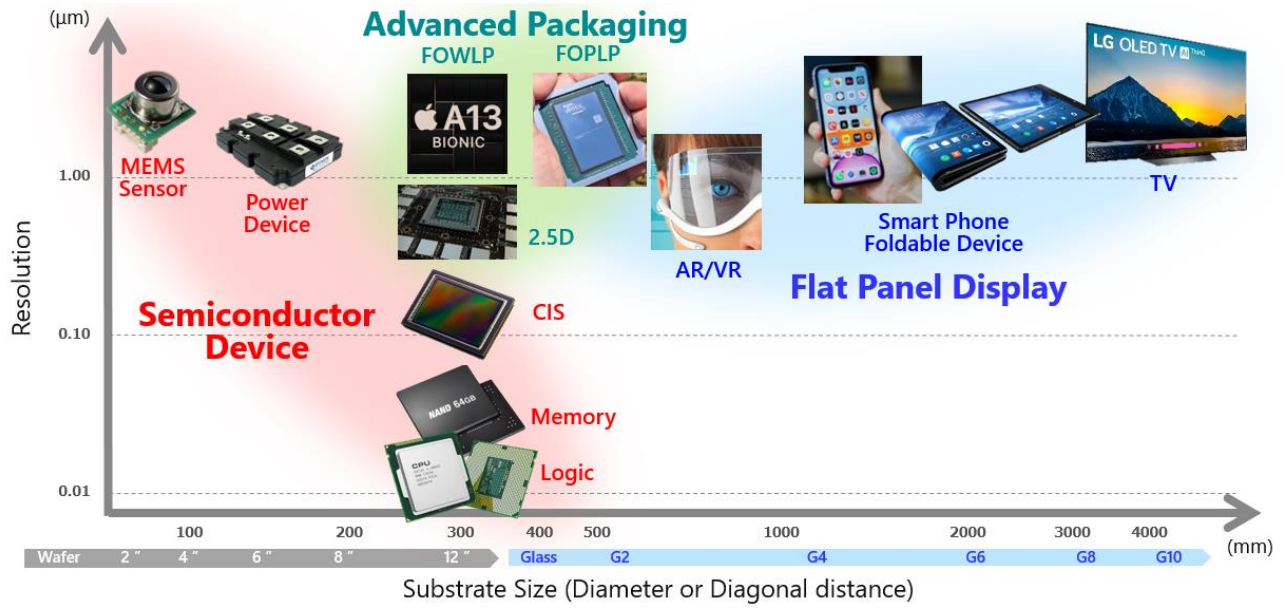


Figure 1. The diversity of the market and the required lithographic equipment, with the required resolution plotted against the size of the device substrate

Canon has focused on providing a wide range of lithography equipment to cover the complete needs of our customers as shown on in Figure 2. From launching the first proximity mask aligners in 1970, in accordance with Moore's law, the lithography equipment has evolved in order to increase the degree of integration of semiconductor devices and reduce the critical dimensions of the devices as shown by the red line in the figure.

As for flat panel display lithography equipment, shown in the blue line, a mirror projection exposure tool, the MPA was introduced in the early 1980s.

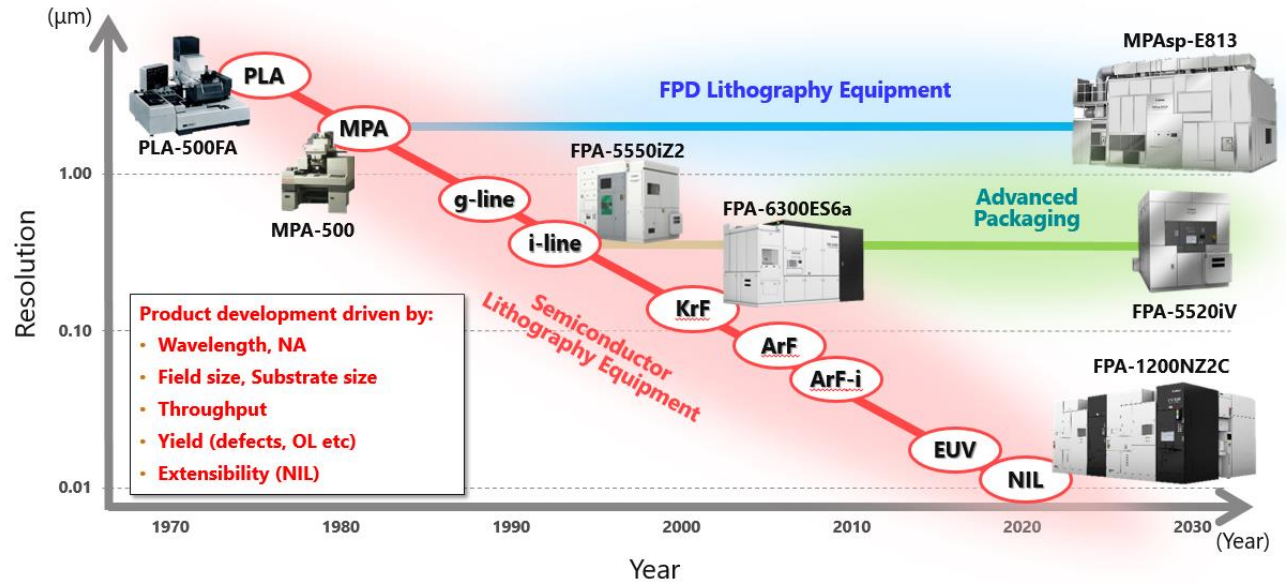


Figure 2. Canon's lithography product line developed over the course of 50 years.

In recent years, i-line lithography equipment has been used for advanced packaging, specifically Fan Out Wafer Level Packaging interposers due to the demand for ultra-dense packaging for smartphones and wearables. Advanced Packaging is indicated by the green line.

Most recently Canon has developed a nanoimprint solution for the patterning of advanced memory devices. In this paper we review the product line and describe how it is being used to address semiconductor patterning, packaging and flat panel display manufacturing.

2. Printing Solutions

a. i-line solutions for semiconductor device patterning

Canon's high throughput i-line system is the FPA-5550iZ2. System throughput is 240 wafers per hour and the daily productivity record is 5150 wafers per day.

Overlay in the semiconductor industry has become increasingly difficult and the challenges are no different for i-line tooling. Canon uses a shot shape compensator located at the top of the projection optics to enhance overlay. The relative horizontal and vertical movements of the two aspherical lenses compensate XY magnifications and skew errors of the shot. With this shot shape compensator, we have reached a mix and match machine overlay of 14 nm, 3σ.

Mark design adds additional complications. For example, in 3D NAND, due to the increase of the number of stacked layers, the alignment mark step does not come out to the surface. Other challenges include planarized marks and low transmittance induced by the use of carbon hard masks. Low contrast marks can be handled using a combination of bright field and dark field measurement techniques. Bright-field measurement is a method of measuring marks using the difference in reflectivity of alignment marks. Making it effective in detecting alignment marks without steps. Dark field measurement can be used to measure the edge of the alignment mark step. Detection wavelength can also be used to improve alignment mark visibility. As shown in Figure 3, by selecting both optimum measurement method and wavelength for each process, alignment can be performed with good contrast.

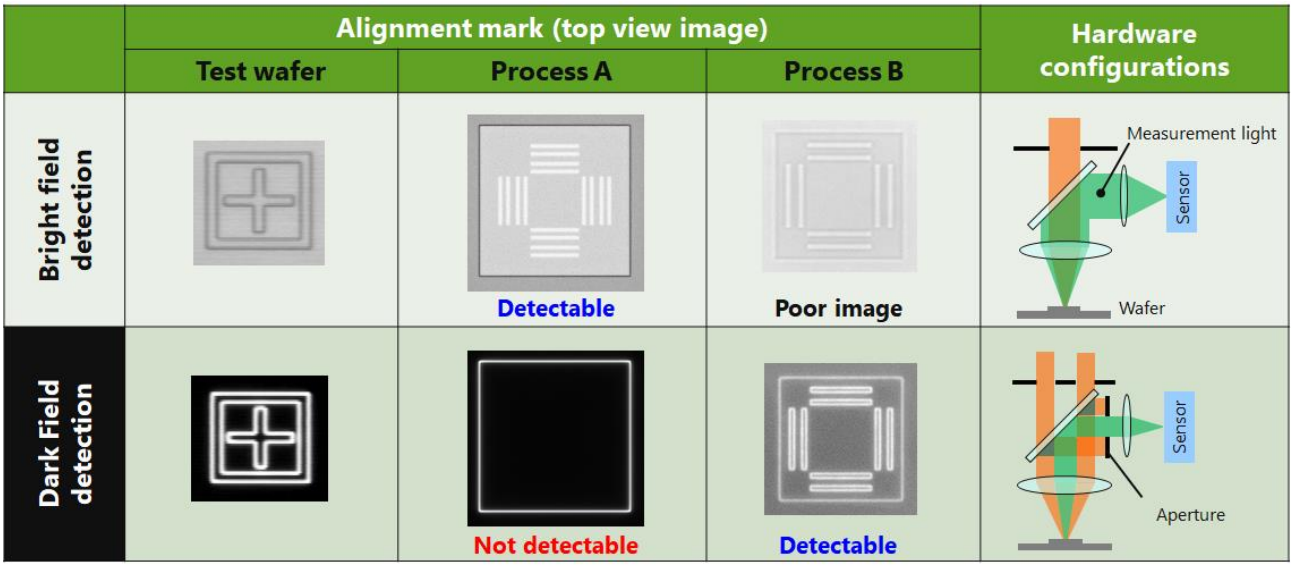


Figure 3. By selecting both the optimum measurement method and wavelength for a particular process, alignment can be performed with good contrast

b. KrF solutions for semiconductor device patterning

Canon's most advanced KrF scanner is the FPA-6300ES6a. This product offers the world's highest productivity of 5600 wafers per day with high uptime and OL accuracy. The tool also offers excellent process robustness.

KrF systems are routinely used in the Word Line Pad (WLP) process for 3D NAND, in which the 3D NAND stacked structure needs to make electrical contact in the memory cell peripheral region. As shown in Figure 4, the 3D NAND staircase is formed with a series of thick film exposures. For a typical lithography level, the resist is exposed, and the etching and trimming is repeated to from four to eight steps of the staircase.

It is well known, however, that thicker resists can have variations in sidewall slope, resulting in excursions of the step length within a staircase pattern. Canon has introduced a Scan Flex method to improve sidewall profile using a multi-focus exposure within a single scan. The scanning exposure with the wafer tilted enlarges the depth of field.

Since the slope angle can be adjusted by focus, it's an effective technique for profile optimization in various thick film processes. The exposure result of Scan Flex tilted 350 microradians provides a perfect straight profile as shown in Figure 5.

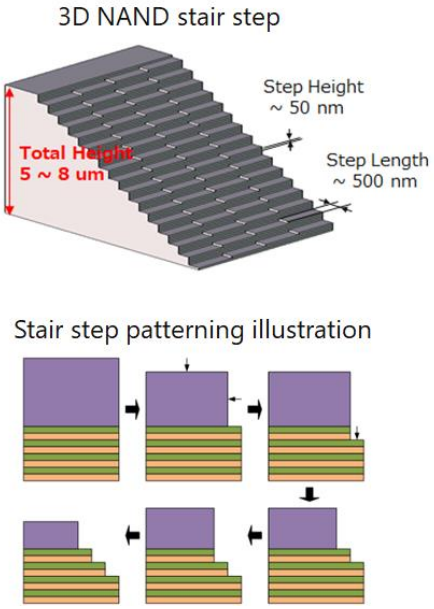


Figure 4. 3D NAND staircase process

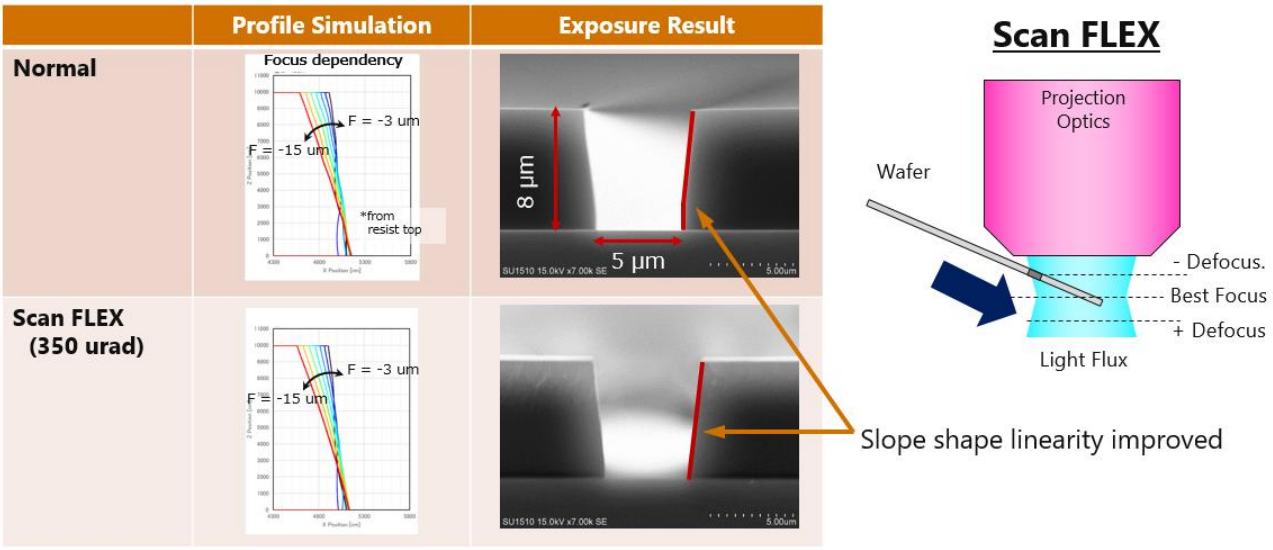


Figure 5. Scan Flex method to improve sidewall profile using a multi-focus exposure within a single scan. The scanning exposure with the wafer tilted enlarges the depth of field, resulting in improved resist sidewall profile.

c. i-line solutions for packaging

The packaging landscape is described in Figure 6. The X axis indicates packaging sizes in mm and the Y axis indicates resolution of required for the redistribution layer in microns. For the fan out of wafer level packages this has recently been reduced from 2 µm to 0.8 µm.

In addition, the chips used for the most advanced artificial intelligence on both the cloud side and the edge side have multiple cores with different architectures to significantly increase multi-threading performance. Hence the chip sizes are becoming larger than 50 mm.

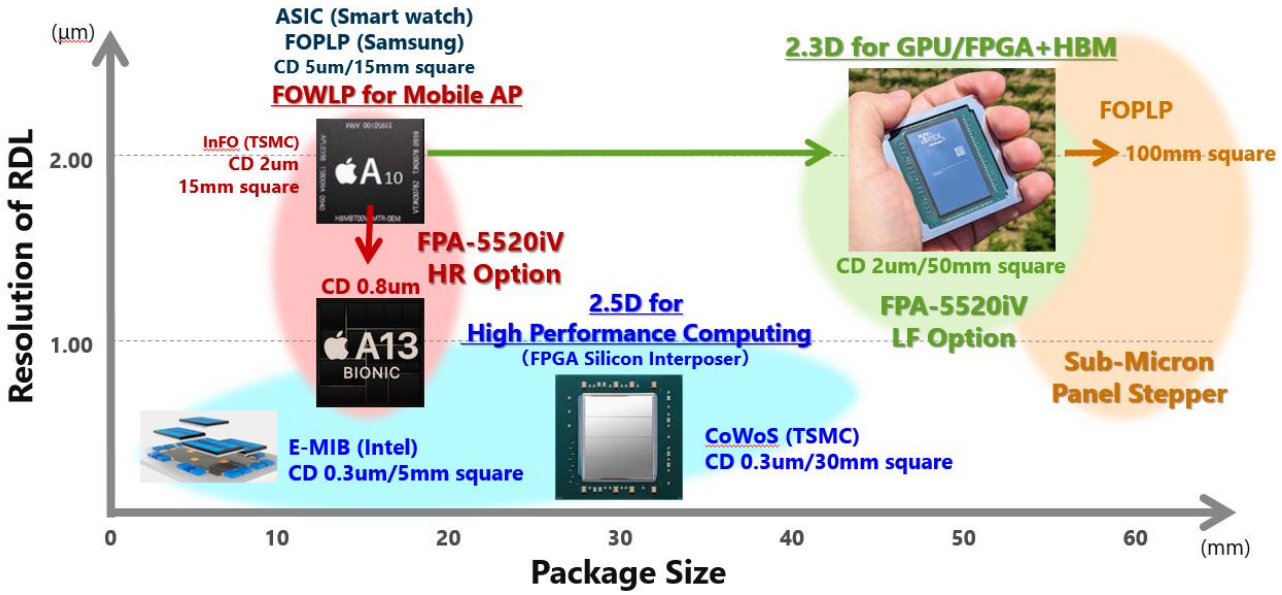
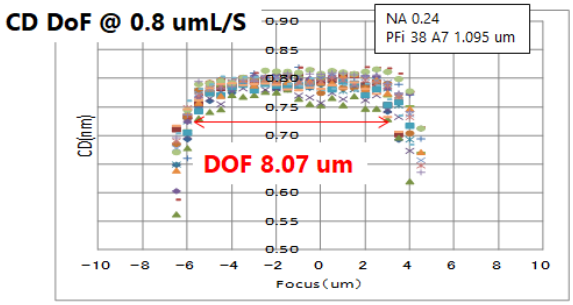


Figure 6. Packaging landscape: Resolution vs. package size

To meet the new package size requirements, Canon has now introduced a new wide field projection optics (UL82). The exposure size of 55 mm x 55 mm. The resolution is 0.8 µm, and DOF is ± 4 µm (See Figure 7.), giving a deep depth of focus. Currently, the optics are used in the mass production process of advanced fan out wafer level packaging and this system will be a key driver for the future expansion of this technology.

Lens features	
Wide range NA variation	0.12~0.24
High Resolution	≦ **0.8 um**
Wide field imaging	**55 mm x 55 mm**
Low distortion for overlay	≦ 150 nm



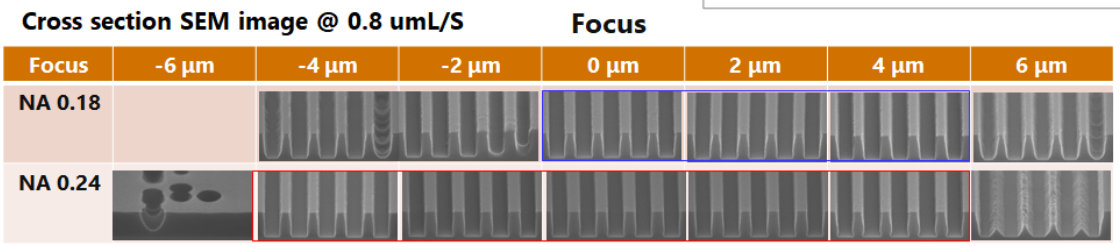
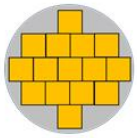
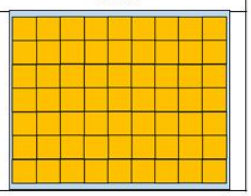


Figure 7. Large field imaging for packaging applications

To address additional current packaging constraints, Canon is also developing a sub-micron panel stepper. The panel stepper can print on larger substrates up to the industry standard 510mm by 515 mm with a resolution of 0.8µm over a 55 mm square field. An example of panel printing is shown in Figure 8. The panel stepper will be introduced in 2020.

Comparison for 55 mm package process

	Φ 300 mm WLP	510 x 515 mm PLP
# chip on 1 sheet	**15 chips**	**63 chips**
Effective chip area	64%	90%
Layout		

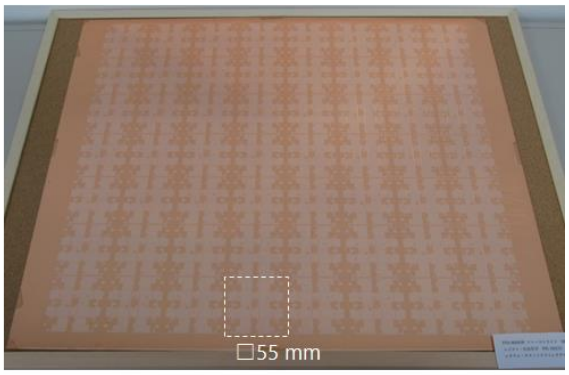


Figure 8. Panel package printing. Printing of larger fields on panels significantly increases the number of fields.

d. **Flat panel solutions**

LED and OLED products are ubiquitous today, as shown in Figure 9. Display sizes range from an inch up to eighty inches or more.

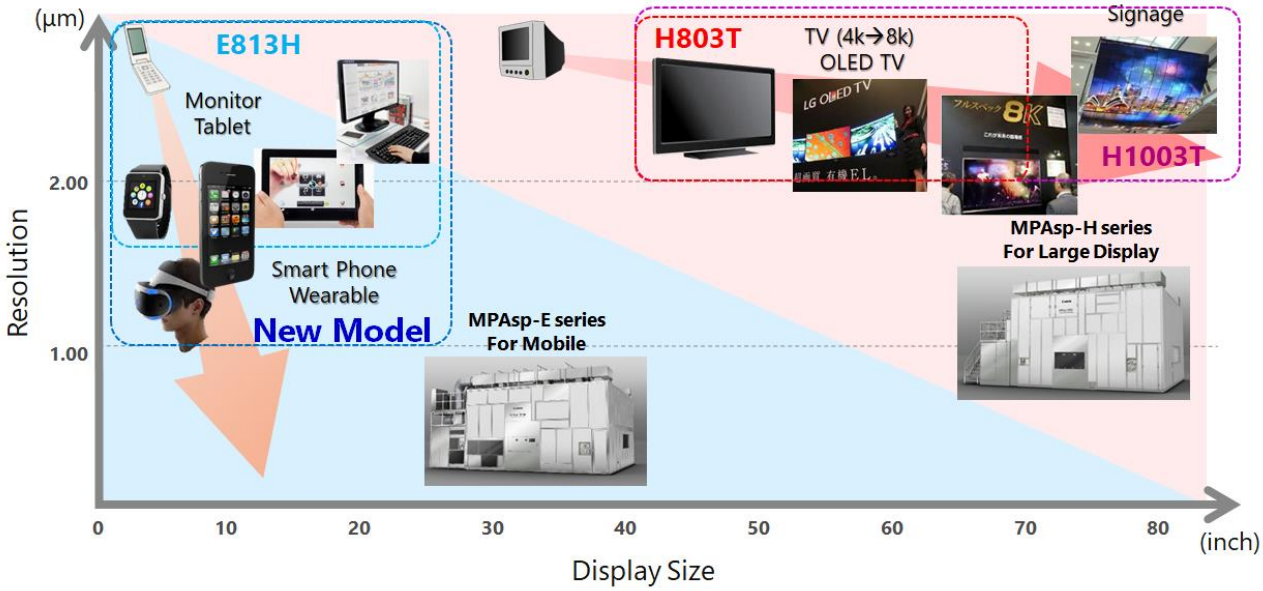


Figure 9. Display size and resolution

Mobile displays now require greater pixel resolution and Canon has developed high resolution mirror optics to address this. The advantage of the mirror optical system is that there are no lenses and hence no chromatic aberration, so the wavelength can be shortened while maintaining a wide wavelength band, as shown in Figure 10. There is however a trade-off between improved resolution and depth of field due to shorter wavelengths. Large, thin glass plates such as G6 have a warpage of about 8 µm after being placed on the chuck so it's very important to ensure a good depth of field.

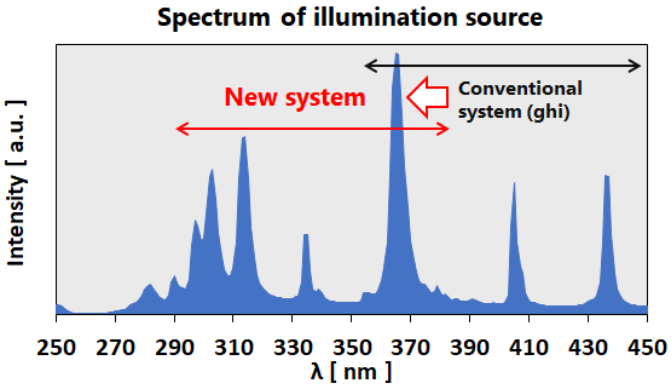


Figure 10. Divided Spectrum Illumination

Canon's new solution to this challenge has been the development of Divided Spectrum Illumination or DSI using a new band pass filter. DSI is an advancement of off axis illumination with a variable illumination on an annular radius, resulting in a 21% larger depth of field than standard off axis illumination. Wavelength reduction improves resolution to 1.2um for lines and 1.8um for contacts and can be improve further with the use of phase shift masks.

e. **Nanoimprint Lithography solutions**

Imprint lithography is an effective and well known technique for replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In 2018, Hiura et al. reported a mix and match overlay (MMO) of 3.4 nm and a single machine overlay (SMO) across the wafer was 2.5nm using an FPA-1200NZ2C four station cluster tool.[10] These results were achieved by combining a magnification actuator system with a High Order Distortion Correction (HODC) system, thereby enabling correction of high order distortion terms up to K30.

Current performance of Canon's NZ2C multi-station cluster tool is summarized below:

- An overlay of 3.2nm has been achieved.
- Throughput is now at 100 wafers per hour
- Defectivity of 0.2/cm^2 has been demonstrated
- And the tool particle adder count has been reduced to 0.0001 particles per wafer pass

Both performance and production capabilities contribute to cost of ownership, which is driven by the process, the mask and the litho tool. In this past we have compared CoO using ArF immersion and NIL for a dense array of contacts.[11] At 80 wafers per hour and a mask life of 80 lots, NIL reduces CoO mainly from the reduction in process steps and process cost. As we continue to increase throughput and extend mask life, the reduction in CoO becomes much more significant.

Canon has focused its NIL efforts to develop solutions for advanced memory devices. For 3D NAND patterning, pattern resolution and overlay have been addressed. Productivity will determine the insertion point for NIL. Looking beyond 3D NAND, resolution is satisfied for the 1A DRAM node, and we are getting close to meeting the specification for overlay. For logic, the 3nm node will need to see enhancements in resolution and improvements in defect density. As a result, we are now prepared to move on to the DRAM market.

Device scaling continues for both DRAM and Phase Change Memory. State of the art DRAM is now at 16nm. For 14nm, an overlay requirement of 15% - 20%, means meeting an overlay budget of 2.1 – 2.8nm. To meet this specification, along with enhancing productivity, NIL HVM readiness requires robust computational methods to provide automated and optimized patterning and overlay solutions.

Computational methods are used extensively for NIL. The process starts with a generation of a mask design, and GDS patterns are a standard in our industry. NIL requires that the GDS get converted to a PNG file that provides both pattern density and directionality information. This capability is also commercially available. From there we create a resist drop recipe from internally developed software. After dispensing, the system imprints, exposes and separates. The desired

outcome are well-defined and well-aligned patterns, that are quickly formed, with no non-fill defects and uniform residual film layer beneath pattern (See Figure 11). But there are many parameters that can influence the final result. First, we discuss patterning aspects and then follow with a discussion of overlay.

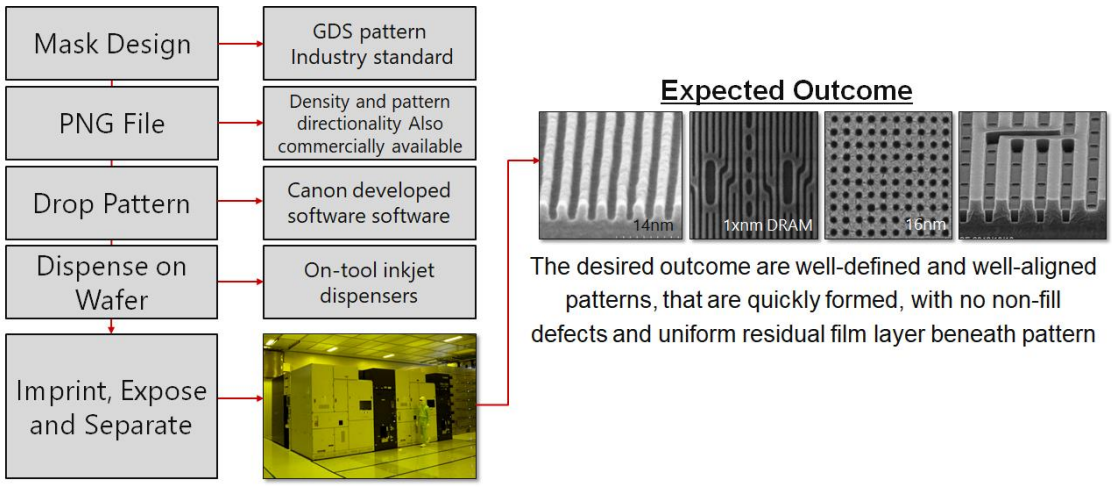


Figure 11. NIL process flow and computational methods designed for NIL

1. Computational patterning methods

To correctly develop a simulation program that can be used to enhance the patterning process, we need the correct inputs, including mask pattern, drop recipe, resist properties, wafer topography, mask profile and so on. What we care about is drop coalescence, spread time, elimination of defects, mask deformation and residual film thickness. We accomplish this by addressing the physics of various processes. The goal is a simulator that helps optimize the NIL process by increasing throughput and decreasing defectivity.

We have developed a new computational fluid dynamics (or CFD) simulator that successfully simulates the non-fill defect distribution for different drop patterns in a time frame (typically 2-3 hours) acceptable for development work. As an example, in Figure 12 we show two different drop patterns and report both the predicted non-fill defects and the actual measured defects after one second. Note that the non-fill defects tend to appear in a perpendicular direction to the gas channel flow for both the simulation and measured samples.

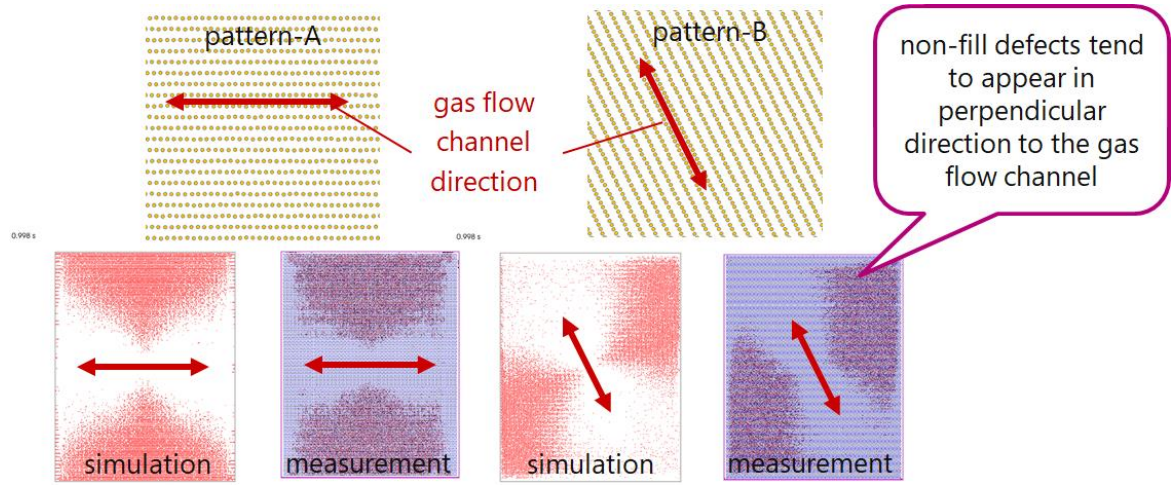


Figure 12. Non-fill defect distribution for two different drop patterns after one second. The CFD model closely replicates the measured results

Figure 13 shows how the simulator can be used to predict fill time, meaning the time at which all non-fill defects are removed. A non-optimized drop pattern still shows evidence of non-fill defects, even after two seconds. With an optimized drop pattern all non-fill defects are gone after 1.2 seconds, in good agreement with measured results.[12]

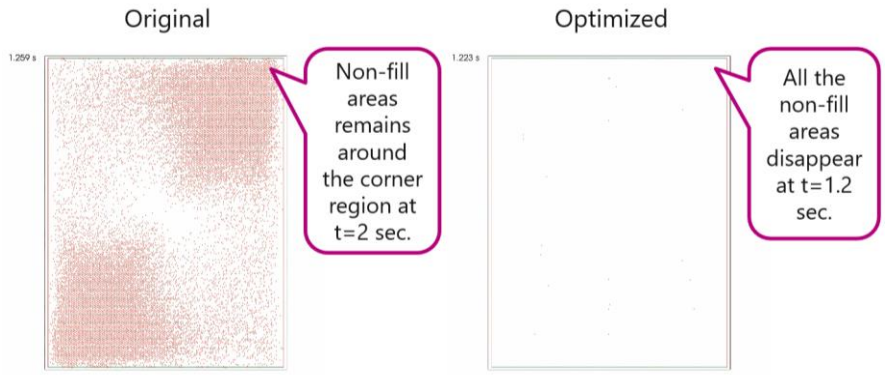


Figure 13. Non-fill defects for a non-optimized and optimized resist drop pattern.

In summary, a computational fluid dynamics model has been developed that accurately predicts resist spreading, resist filling and the dissipation of non-fill defects. The model can be used with any drop pattern generated from our internal software package, making it a valuable tool for optimizing throughput and eliminating non-fill defects. More details of the model can be found in reference 13.

The simulator also accurately predicts final film thickness as a function of drop pattern. We take advantage of this capability when doing overlay.

2. Alignment and Overlay for Nanoimprint Lithography

In order to address overlay in a Nanoimprint system, there are many factors that need to be considered, some of which are quite different than what is required for photolithographic tools. Generally speaking, the process can be broken down into two categories; Alignment and Overlay (See Figure 14.) In this paper we separately address alignment and overlay.

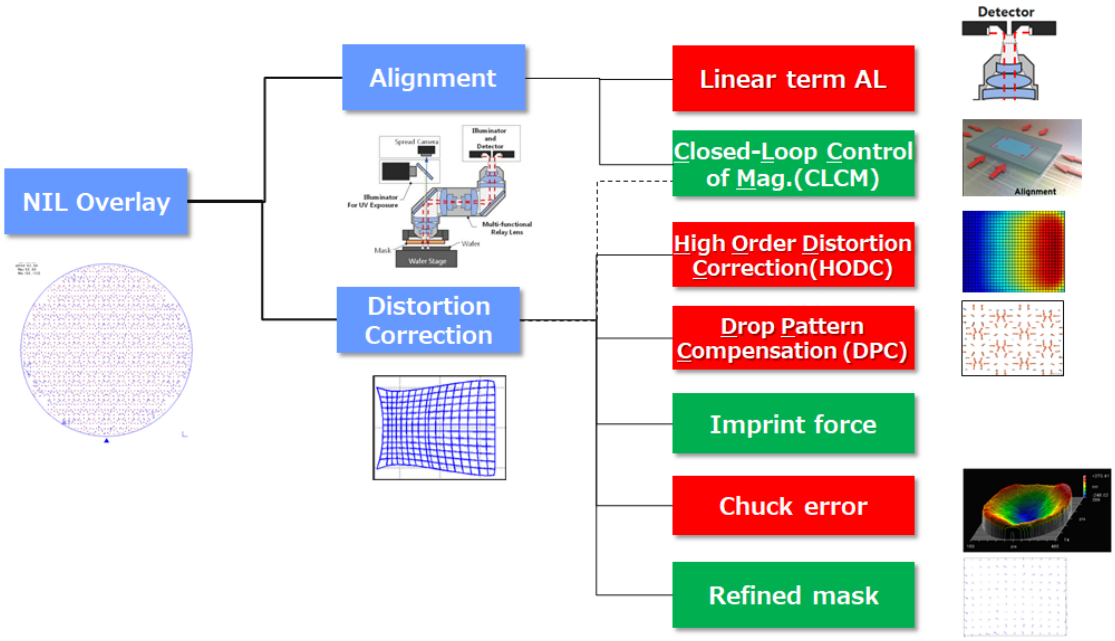
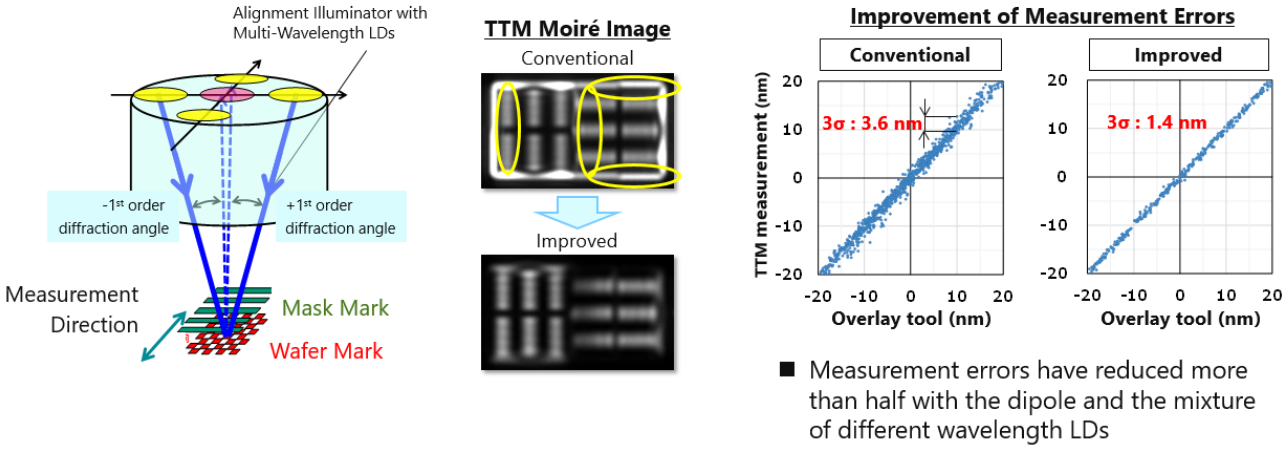


Figure 14. Factors that influence overlay in a nanoimprint tool

The NZ2C system employs a Through The Mask (TTM) alignment system as shown in Figure 15a. First order terms are passed through Moiré marks on the mask and wafer with a sensitivity on the order of 1nm.



a) b) c)

Figure 15. a) Through The Mask (TTM) alignment system, b) Signal blooming (highlighted in yellow) was reduced using a dipole/polarized illuminator, c) comparison of the TTM measurement versus results on an overlay tool before and after optimization.

By applying dipole illumination and a multi-wavelength illuminator we can reduce the blooming of the Moiré signal as shown in the center two images. The result is TTM align measurements that show only a 1.4nm 3 sigma variation when compared to the measurements from an Archer overlay tool. Canon has also started to apply machine learning to enhance process robustness, leading to more repeatable results from wafer to wafer. Details can be found in reference 14.

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and lens during the exposure process. A different approach is required for the imprint tool in order to do high order distortion controls (HDOC). HDOC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis

Heat input on a field by field basis is realized through the use of DMD array which imparts heat through the mask onto a stepper field of a wafer. The basic operation of the system, along with initial results has been described in previous publications.[15,16]

Recent efforts have been driven by applying low friction coatings to the wafer chucks and improving chuck flatness as shown in Figure 5. The combination of the HODC system together with flatter, low friction chucks, enables better overlay. The graph on the bottom right of Figure 16 illustrates a 50 percent improvement in performance

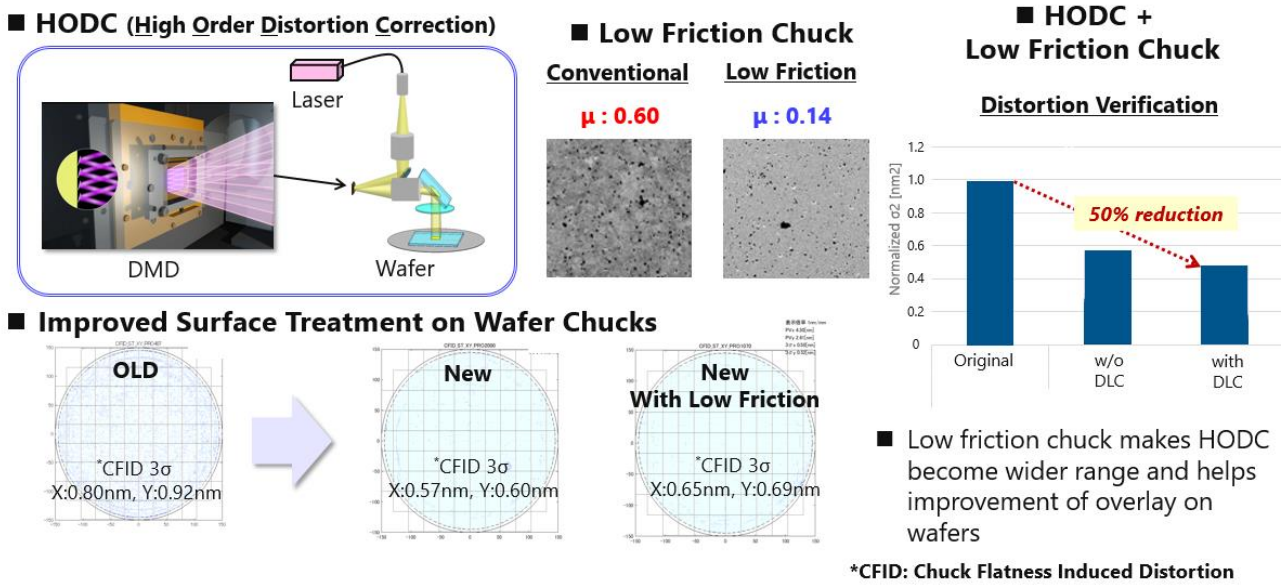


Figure 16. The combination of the HODC system together with flatter, low friction chucks, enables better overlay.

There is an additional distortion term that must also be addressed for the case of nanoimprint lithography. NIL drop patterns are typically designed to minimize resist fill time and create a uniform residual layer beneath the resist pattern. For device wafers, however, it is important to recognize that there are both long wavelength flatness errors coming from the wafer chuck and existing pattern topography from previously patterned levels that cause out of plane errors. When the mask comes in contact with the resist on the wafer, these out of plane errors can then induce mask bending, resulting in an additional distortion term.

To minimize this distortion, a Drop Pattern Compensation (DPC) Model has been implemented to minimize the added distortion terms. As an example (Figure 17), improvements can be realized with a favorable mask bending shape. In this case, mask bending compensates the non-flatness induced overlay errors to achieve a near-zero bending strain mismatch.

Cherala et al. results are presented for a device like wafer in which the overlay errors within a field were reduced from 5.4nm to 3.4nm, 3 sigma.[17] Additional improvements to the DPC model can be found in Reference 18.

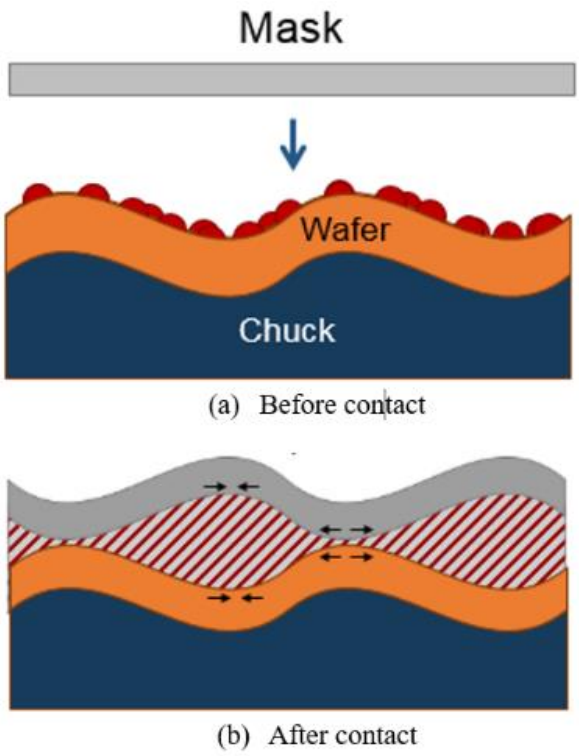


Figure 17. Schematic of the DPC process.

3. Conclusions

Canon has focused on providing a wide range of lithography equipment to cover the complete needs of our customers. From launching the first proximity mask aligners in 1970, in accordance with Moore's law, the lithography equipment has evolved in order to increase the degree of integration of semiconductor devices and reduce the critical dimensions of the devices.

In this paper we reviewed the Canon product line and describe how it is being used to address semiconductor patterning, packaging and flat panel display manufacturing. Improvements to KrF systems have enabled improved resist profiles in thick resists used to form the stair step structure in 3D NAND devices. In recent years, i-line lithography equipment has been used for advanced packaging, specifically Fan Out Wafer Level Packaging interposers due to the demand for ultra-dense packaging for smartphones and wearables.

Most recently Canon has developed a nanoimprint solution for the patterning of advanced memory devices. Imprint lithography is an effective and well-known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. In this work, we reviewed the computational methods that are applied towards patterning, alignment and overlay control.

Acknowledgments

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