

The Advantages of Nanoimprint Lithography for Semiconductor Device Manufacturing

Toshiya Asano¹, Keita Sakai¹, Kiyohito Yamamoto¹, Hiromi Hiura¹, Takahiro Nakayama¹, Tomohiko Hayashi¹, Yukio Takabayashi¹, Takehiko Iwanaga¹, Douglas J. Resnick²

¹Canon Inc., 20-2, Kiyohara-Kogyodanchi, Utsunomiya-shi, Tochigi 321-3292 Japan

²Canon Nanotechnologies Inc., 1807 West Braker Lane, Bldg. C-300 Austin, TX 78758 USA

Abstract

Imprint lithography is an effective and well known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Given the risks associated with this introduction, generally a combination of both performance and cost advantage is preferred. In this paper both performance attributes and cost are discussed. NIL resolution and linewidth roughness do not have the limitations of conventional projection lithographic method. Furthermore, it is not subject to patterning restrictions that forced the industry towards one dimensional patterning.

A cost example case of 20nm dense contacts is also presented. Because NIL utilized a single step patterning approach, process costs are substantially reduced relative to ArF immersion lithography. Overall, NIL currently realizes a 28% cost advantage for this case, but as mask life continues to improve, the cost advantages become much more significant.

Keywords: nanoimprint lithography, NIL, resolution, linewidth roughness, design freedom, mask life, CoO

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features.^{1,2} Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.³⁻⁹ The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to

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Any new technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Given the risks associated with this introduction, generally a combination of both performance and cost advantage is preferred. In this paper both topics are discussed. With respect to performance, we review resolution, linewidth roughness and design freedom. Cost advantages are driven by process cost reductions, tool throughput and extended mask life. All three topics are discussed and a cost comparison is presented for an array of dense contact holes.

2. Performance Advantages

a. Resolution

Generally speaking, NIL resolution is determined by the mask making process. In recent years, mask resolution has been enhanced through the implementation of multi-beam writers which can aperture each individual element down to 10nm or below. Pictured in Figure 1 are examples of imprinted lines and spaces and contact holes. To date, 14nm lines and spaces have been imprinted. In addition, production mask writers can now resolve contact hole arrays as small as 16nm. This type of resolution is important in particular for advanced DRAM devices as scaling continues over the next five years.

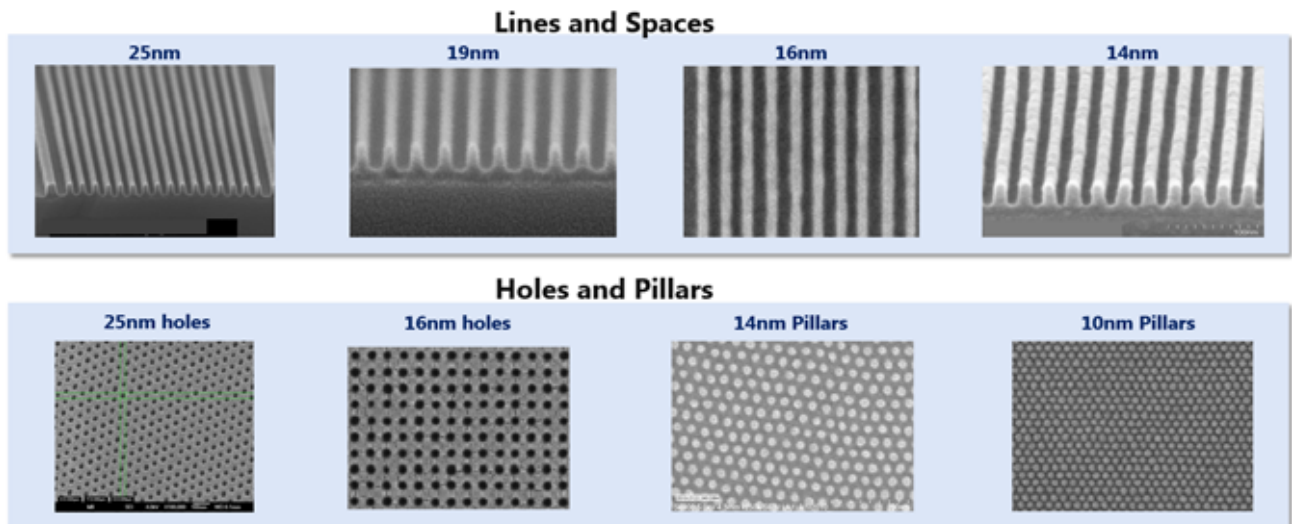


Figure 1. Line/space and contact hole resolution

b. Linewidth Roughness

It is well known that line edge and line width roughness (LWR) has an impact on transistor performance, affecting both threshold voltage and off state leakage.¹⁰ Lithographic approaches such as extreme ultraviolet lithography (EUV) typically see excessive LWR values when using low dose resists. LWR can be reduced by increasing dose, but not without impacting throughput.

For NIL, LWR can be kept below 3nm by applying non-chemically amplified low sensitivity electron beam resists. Mask write time, especially when using multi-beam writers is still very acceptable. Shown in Figure 2 is a graph of linewidth roughness as a function of feature size. There is a virtually no change in LWR down to 14nm.

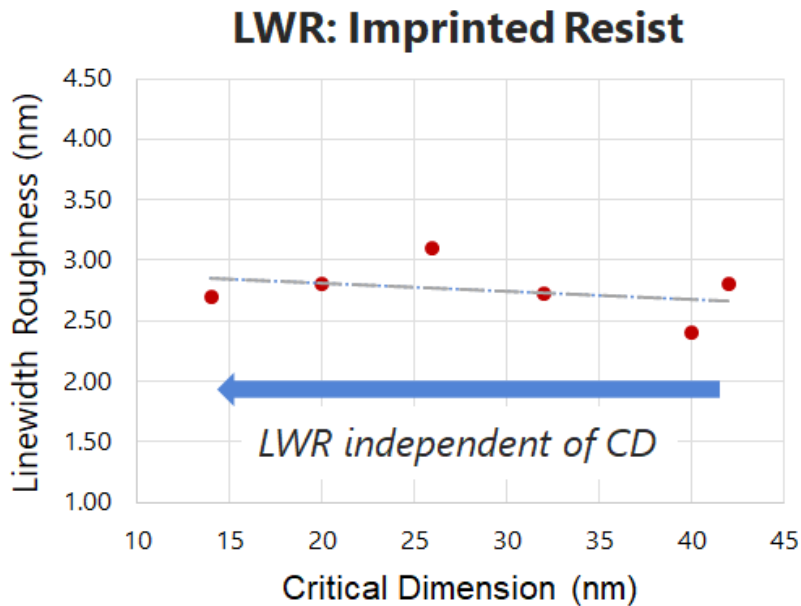


Figure 2. Linewidth roughness as a function of critical dimension. No degradation is observed down to 14nm.

c. Design Freedom

Because of resolution limitations for conventional lithography, two dimensional patterning became much more restricted after the 65nm logic node and the 38nm 2D NAND Flash node. Lithography based patterning limitations forced the industry to adopt much stricter one dimensional design rules which, in turn, impacted design complexity and device yield. NIL does not have these limitation, since resolution is limited only by what can be resolved in mask. Three different two dimensional patterns are shown in Figure 3: a) a 38nm 2D NAND Flash gate level, b) a 2xnm SRAM cell, and c) a 1xnm DRAM test cell.

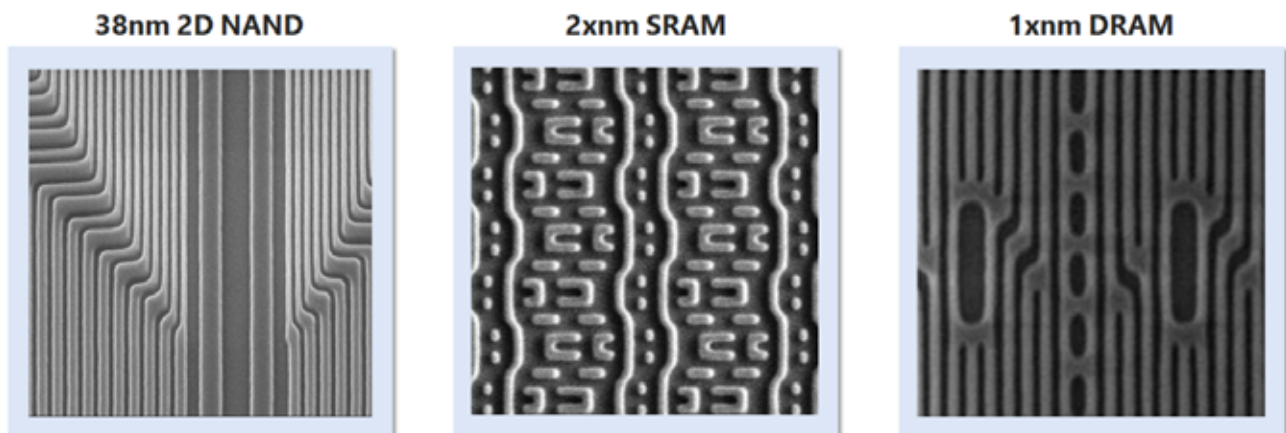


Figure 3: a) a 38nm 2D NAND Flash gate level, b) a 2xnm SRAM cell, and c) a 1xnm DRAM test cell.

It is interesting to note the design restrictions currently imposed by current multipatterning approaches that employ cut levels. Edge placement errors impact overlay budgets, and with the ability to avoid cutting levels, NIL has the potential to relax current overlay budgets, depending on the actual device level.

Furthermore, patterning capability is not restricted to two dimensions. Both the University of Texas and Toshiba Memory Corporation have demonstrated the ability to fabricate three dimensional structures, including a dual damascene example, as shown in Figure 4.^{11,12}

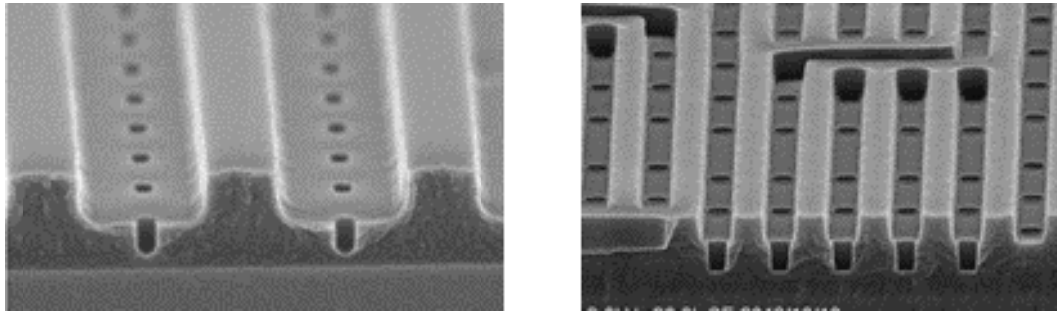


Figure 4. Three dimensional structures, including a dual damascene example.

3. Cost of Ownership

Although pattern multiplication processes have enabled the industry to continue to aggressively scale devices, the methods come with a cost; both technical and financial. The technical price we pay for pitch splitting comes in the way of critical dimension control and additional overlay terms (pitch walking). Despite the precision of our newest deposition and etch processes, the additional process steps used to reduce pitch introduce these types of errors. Any technology (NIL and EUVL for example) that can deliver a single lithography step process has the opportunity to deliver a simplified solution with better CD and overlay control.

a. Cost of Ownership Contributors

Contributors to cost of ownership (CoO) can be broken down into three groups: process CoO, lithography tool CoO, and mask CoO. Tool CoO includes tool fixed cost, running costs, the illumination source cost and the cost associated with resists (imprint resist for example). Mask CoO includes master mask price, replica mask price (which can be broken into two components: mask price and mask life) and mask cleaning cost (specifically the cost of cleaning the replica mask). Finally, the additional process steps must be taken into account. Possible contributors include deposition steps, track processes, wet and dry etching, wet cleans, and costs associated with other required lithography steps. As an example, for a NAND Flash gate level, a single optical litho step is required following a spacer based process used to decrease pitch by a factor of two.

CoO should be modelled for a particular device level (or levels), since the process flow can vary significantly from level to level. In this work, a dense 20nm contact array (for a DRAM device, for example) was modeled using a 2x ArFi SADP approach and a NIL approach.

b. Process Cost

The process steps required to define a 20nm dense contact array are significant using ArFi and greatly add to the overall cost of ownership for this device level. An example process flow is shown in Figure 5, which compares the processing steps for both ArFi and NIL. Also shown is a normalized plot of process cost for each lithographic approach. Not surprisingly, NIL process costs are reduced by a factor of about 3x.

Process Flow	ArFi 2x SADP Process Steps	NIL Process Steps
Oxide dep	✓	✓
Hardmask 1 dep	✓	
SoC deposition	✓	✓
SoG deposition	✓	✓
Primary Litho		
Trim etch	✓	
SoG etch	✓	✓
SOC etch	✓	✓
ALD sidewall deposition	✓	
ALD etchback	✓	
SoC etch	✓	
Blanket SOC deposition	✓	
Hardmask 2 deposition	✓	
Second Litho		
Trim etch	✓	
Hardmask 2 etch	✓	
SOC etch	✓	
ALD sidewall deposition	✓	
ALD etchback	✓	
SOC etch	✓	
Hardmask 1 etch	✓	
Oxide etch	✓	✓
Strip	✓	✓
KrF litho		
Cut etch	✓	
Strip	✓	
	23 process steps	7 process steps

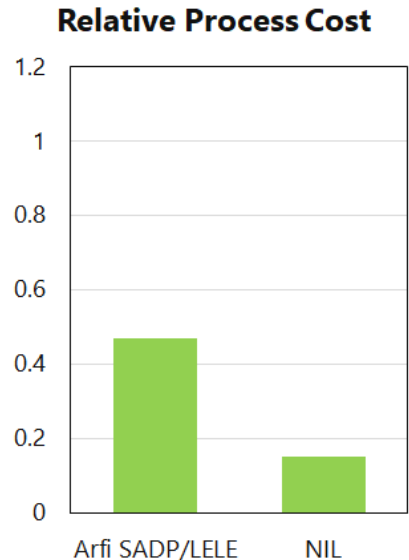


Figure 5. Process flow example comparing the number of process steps required to pattern a 20nm dense array of contact holes. The NIL process cost is reduced by about a factor of 3x.

c. Litho Tool Cost

The litho tool cost is affected by throughput. Previous papers have discussed throughput breakdown in detail.¹³ Overheads to the imprint TAKT time have been reduced by applying a multi-field dispense strategy, as opposed to dispensing and imprinting in a sequential fashion. The reduction in overhead is on the order of .24 seconds per field, resulting in an increase in throughput to 90 wafers per hour. Figure 6 shows that non-fill defectivity is nominally the same for the multi-field approach.

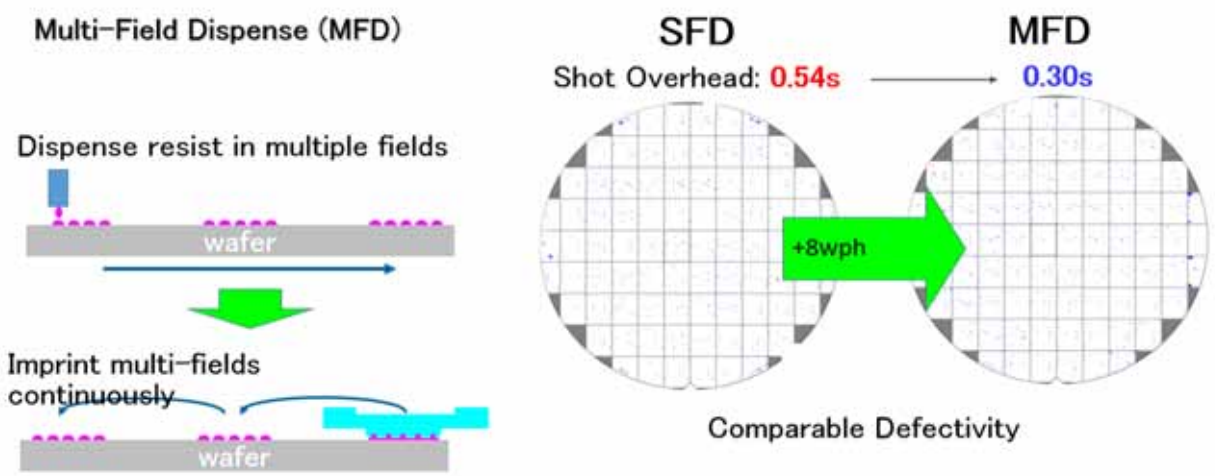


Figure 6. Defect inspection result comparison. The multi-field dispense results are comparable in defectivity to the sequential imprinting method.

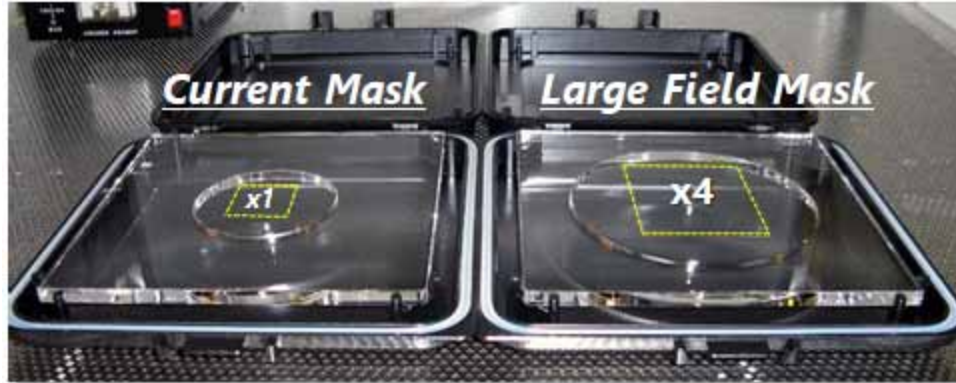


Figure 9. Comparison of the current NIL mask format and a NIL large field mask format.

d. Mask Cost

NIL requires both a master mask and multiple copies of a replica mask. As a result, the gating item on cost for NIL is the mask life of the replica mask. In 2017 the mask life target of 80 wafer lots was met. This year, Toshiba Memory Corporation has demonstrated a mask life of over 300 lots (Figure 11). The increase in mask life has been driven by a variety of techniques designed to mitigate particles in the wafer tool. The techniques cover source control, particle avoidance and particle collection, as shown in Figure 10. As a next step, we are considering the implementation of on-tool mask cleaning.

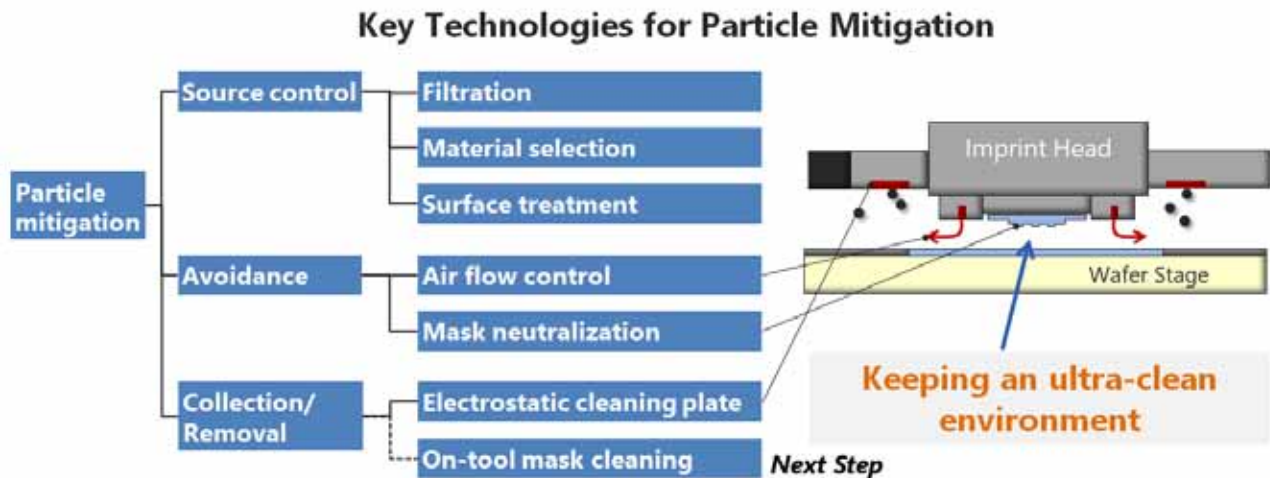


Figure 10. The increase in mask life has been driven by a variety of techniques designed to mitigate particles in the wafer tool. The techniques cover source control, particle avoidance and particle collection.

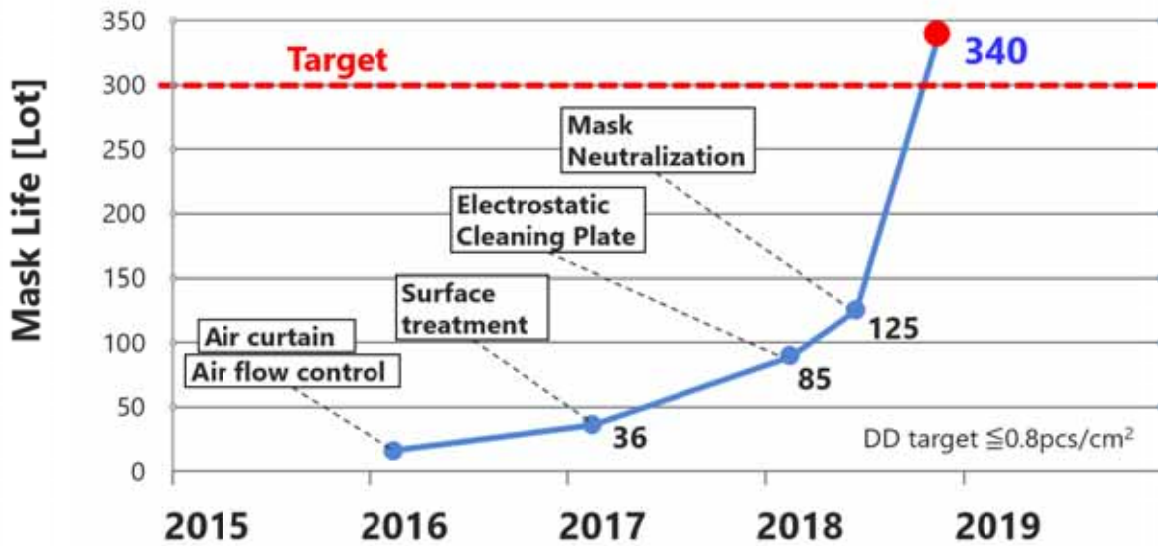


Figure 11. Mask life history. This year, Toshiba Memory Corporation has demonstrated a mask life of over 300 lots.

Shown in Figure 12 is relative mask cost for both ArF immersion and NIL. As expected, for an 80 lot mask life, ArF immersion has a cost advantage. But as mask life increases to 300 wafer lots and beyond, the cost difference becomes very small.

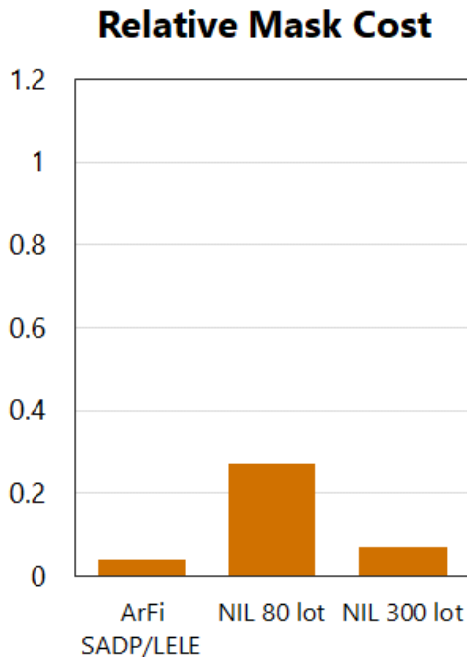


Figure 12. Relative mask cost for both ArF immersion and NIL. As expected, for an 80 lot mask life, ArF immersion has a cost advantage. But as mask life increases to 300 wafer lots and beyond, the cost difference becomes very small.

e. Cost of Ownership Summary

Figure 13 is a summary cost comparison between NIL and ArF immersion for a 20nm dense array of contact holes. At a throughput of 80 wafers per hour and a mask life of 80 wafer lots, NIL holds has a 28% cost advantage. As throughput increases to 90 wafers per hour and mask life exceeds 300 lots, the cost advantage now jumps to 52%. In addition, further cost reductions may be realized by moving to a large field mask which reduces the number of shots per wafer, as shown in section 3c.

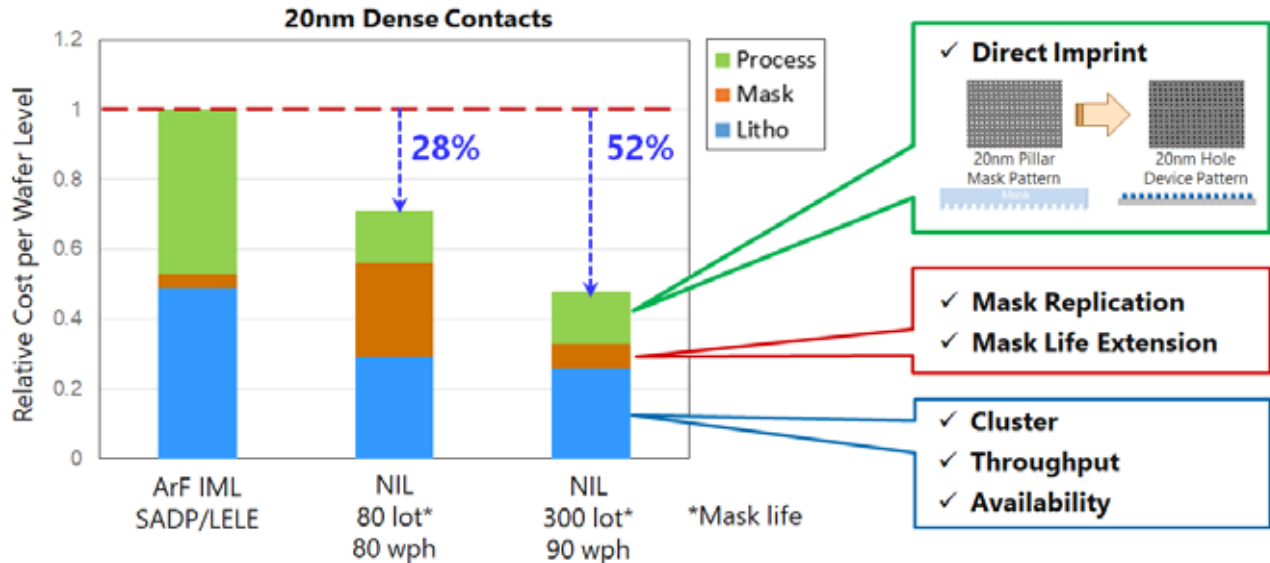


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4. Conclusions

Any new technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Given the risks associated with this introduction, generally a combination of both performance and cost advantage is preferred. In this paper both topics are discussed. In this paper both performance attributes and cost were discussed. NIL resolution and linewidth roughness do not have the limitations of conventional projection lithographic method. Furthermore, it is not subject to patterning restrictions that forced the industry towards one dimensional patterning.

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