Status of Overlay Performance for NIL High Volume Manufacturing

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Abstract

Nanoimprint lithography (NIL) techniques are known to possess replication resolution below 5nm. A specific form of imprint lithography using jetted resist has been developed for manufacturing advanced CMOS memory. Canon's NIL process involves field-by-field inkjet deposition of a low viscosity resist fluid followed by imprinting with nano-scale precision overlay. A mask with a relief structure is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is separated from the substrate leaving a patterned resist on the substrate.

The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In this work, improvements to the alignment system, together with the High Order Distortion Correction (HODC) system have enabled better distortion and overlay results on both test wafers and device wafers. The linear response of the HODC system was demonstrated for multiple high order terms and on test wafers, XMMO of 2.9nm and 3.2nm in x and y respectively was achieved. Additionally an SMO of 2.2nm and 2.4nm was achieved, with an opportunity to further improve results by applying wafer chucks with better flatness specifications.

Keywords: nanoimprint lithography, NIL, alignment, overlay, high order distortion

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

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Device wafers present a greater challenge, since the under layers on the wafer vary from level to level and cause degradation of alignment signals. The purpose of this paper is describe the improvements to alignment and overlay on both test wafers and device wafers.

2. Alignment and Overlay

a. Through The Mask (TTM) Alignment System

The NZ2C system employs a Through The Mask (TTM) alignment system as shown in Figure 1. First order terms are passed through Moiré marks on the mask and wafer with a sensitivity on the order of 1nm. On device wafers, it is possible to enhance the align signal and avoid blooming by using multiple wavelengths, and controlling the intensity of each wavelength. The method aids in controlling signal variations, resulting in reduced measurement errors. The impact of this upgrade is discussed in more detail in Section 3d.

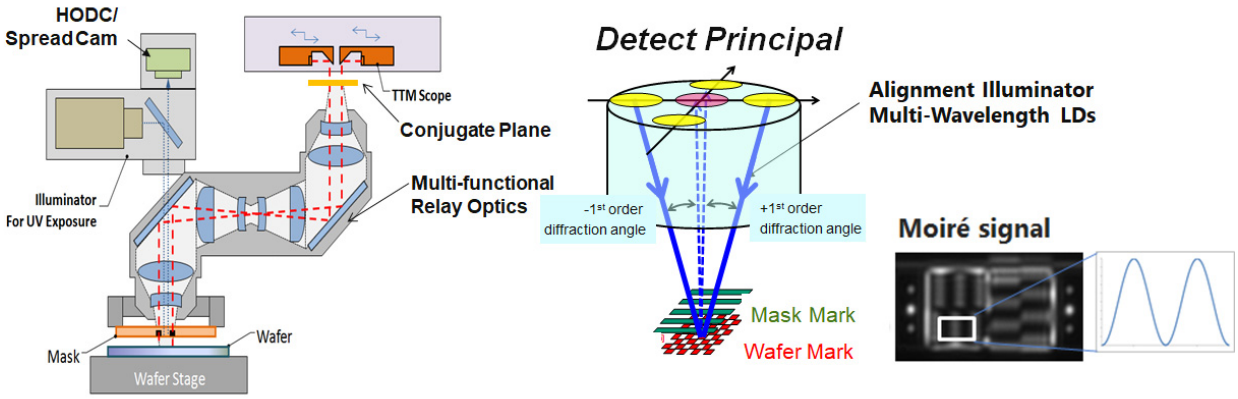

Figure 1. Through The Mask (TTM) alignment system

b. High Order Distortion Correction (HODC) System

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and Projection lens during the exposure process. But, the imprint tool doesn't have Projection lens. So, a different approach is required for the imprint tool in order to do high order distortion correction (HODC). HODC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis

Heat input on a field by field basis is realized through the use of DMD array which imparts heat through the mask onto a stepper field of a wafer. The basic operation of the system, along with initial results has been described in previous publications.[11,12] The system is shown schematically in Figure 2.

The combination of magnification actuation and the HODC system gives a very linear response for individual high order distortion terms as shown in Figure 3. Plotted in each graph is the actual distortion correction across a field as measured using Archer marks as a function of the anticipated correction, expressed in nanometers per square centimeter for K8 and K22. In this experiment, a test wafer was first patterned with an ArF immersion tool and corrections were applied using the FPA-NZ2C magnification and HODC system. The corrections are based on a measurement set of 143 sites within the field. As shown in each plot, the actual distortion corrections are linear with respect to the simulated input values.

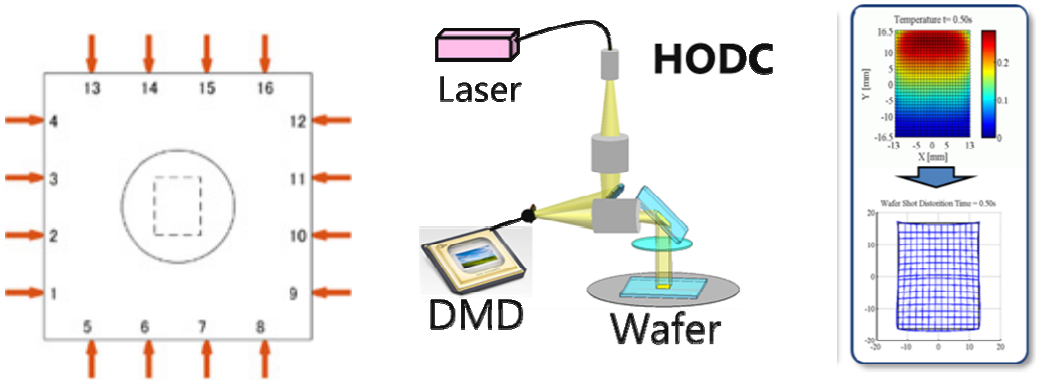

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Figure 2. a) Schematic drawing of the Mag actuator. b) Schematic drawing of the HODC system. c) Heat input needed to correct for existing distortion.

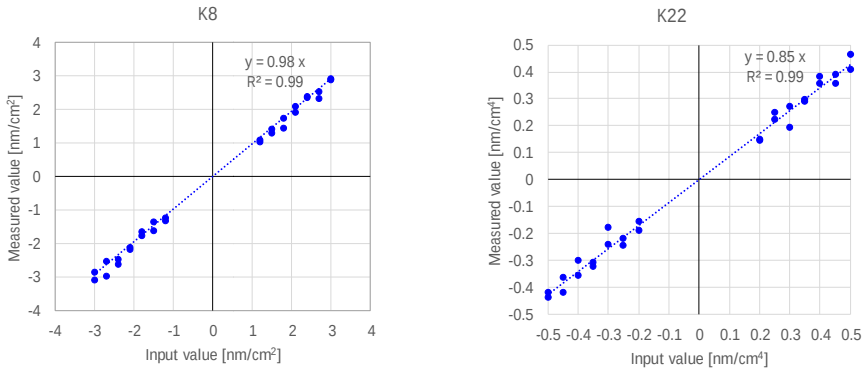

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Figure 3. a) Linearity of K8. b)Linearity of K22.

c. Test Wafer Results

The TTM and HODC systems were applied to test wafers and the results are reported in Figure 4 and 5. Figure 4 depicts Cross Matched Machine Overlay (XMMO) on an existing level patterned with an ASML 1950 ArF immersion tool. A total of 84 fields were measured, including twelve points per field. The results are an average across 23 wafers. XMMO of 2.9nm and 3.2nm mean plus three sigma was achieved in x and y, respectively.

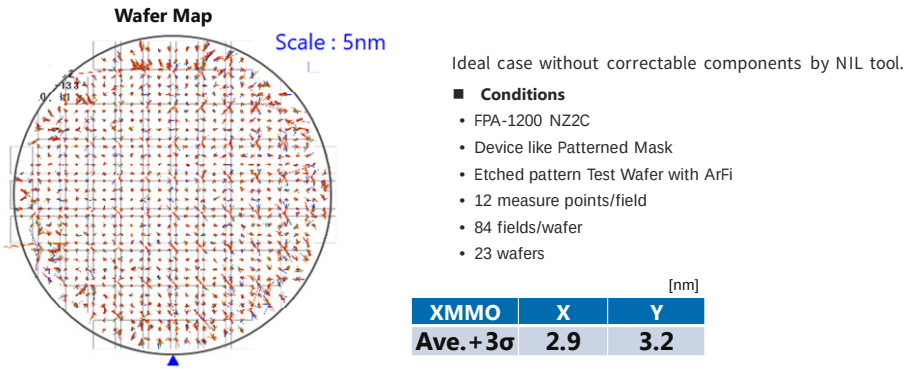

Figure 4. XMMO using an FPA-1200 NZ2C imprint system. XMMO of 2.9nm and 3.2nm mean plus three sigma was achieved in x and y, respectively

Similarly, Figure 5 depicts Single Machine Overlay on an existing level patterned with the FPA-1200 NZ2C tool. A total of 84 fields were measured, including twenty points per field. The results are an average across three wafers. SMO of 2.2nm and 2.4nm mean plus three sigma was achieved in x and y, respectively. Residual distortions were 0.7nm, mean plus three sigma.

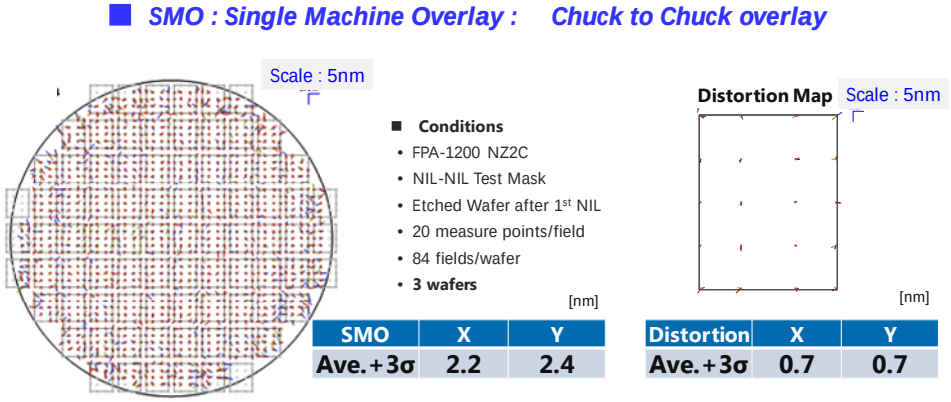

Figure 5. SMO using an FPA-1200 NZ2C imprint system. SMO of 2.2nm and 2.4nm mean plus three sigma was achieved in x and y, respectively

It is important to note that distortions are greater nearer the edge for this SMO test. Figure 6 breaks out full field overlay and partial field overlay for one particular test wafer. The full field overlay errors are on the order of 2.1nm. The partial field errors are closer to 3.5nm, on average.

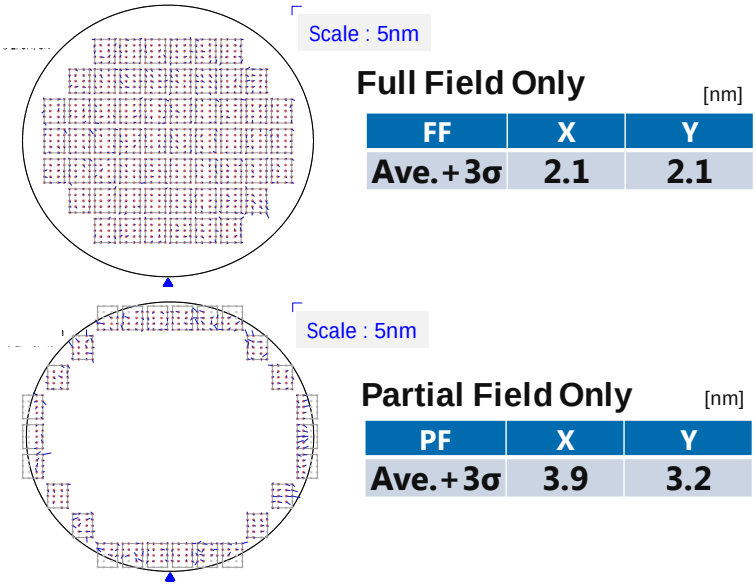

Figure 6. SMO results broken out for full fields and partial fields.

The reason for the difference is primarily due to the two chucks used in this experiment within a multi-station NZ2C system, as shown in Figure 7. The chuck used to pattern the zero level had greater flatness errors, and the errors were greatest near the wafer edge when compared to the chuck used to pattern the following level. The flatness error corresponds to a Chuck Flatness Induced Distortion (CFID) on the order of 3.0nm, consistent with the high overlay errors observed near the wafer edge. In the future, the newer chuck design will be applied to reduce overlay errors in all fields and also generate Dedicated Chuck Overlay (DCO) results.

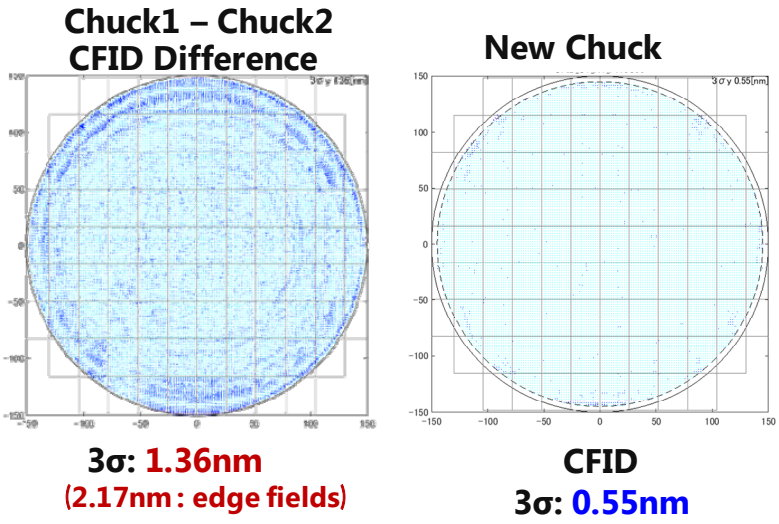

Figure 7. Chuck flatness induced distortion explains the higher overlay errors observed near the wafer edge. And new chuck was improved the CFID near the wafer.

d. Device Wafer Results

Verification of the improvements were observed by mapping the higher order distortion terms up to K29 as shown in Figure 8. Plotted are the errors for each term without any HODC correction, predicted value using HODC and a final correction on a device wafer. Very little difference is observed between the predicted value and the final correction.

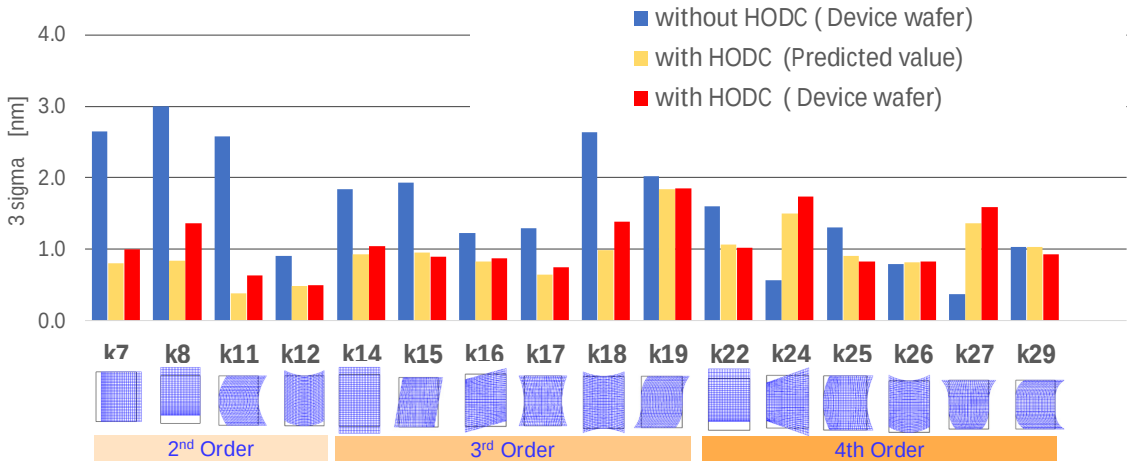

Figure 8. Overlay distortion for terms up to K29. There is good agreement between the predicted value and the final correction.

3. Conclusions

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment and overlay. In previous papers, overlay results have been reported on test wafers. In this work, improvements to the alignment system, together with the High Order Distortion Correction (HODC) system have enabled better distortion and overlay results on both test wafers and device wafers. The linear response of the HODC system was demonstrated for multiple high order terms and on test wafers, XMMO of 2.9nm and 3.2nm in x and y respectively was achieved. Additionally an SMO of 2.2nm and 2.4nm was achieved, with an opportunity to further improve results by applying wafer chucks with better flatness specifications.

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