Patterning, Mask Life, Throughput and Overlay Improvements for High Volume Semiconductor Manufacturing using Nanoimprint Lithography

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Abstract

Imprint lithography is an effective and well-known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In this work, we review progress on pattern capability, throughput, mask life and overlay. To minimize distortion and improve overlay, a Drop Pattern Compensation (DPC) method has been implemented to minimize the added overlay distortion terms. In this paper we describe the origins of the out of plane errors, and describe the method used to correct these errors along with some examples. Improvements to both cross matched machine overlay (XMMO) and imprint mix and match overlay (IMMO) are presented.

Keywords: nanoimprint lithography, NIL, throughput, overlay, mask life, XMMO, IMMO

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

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Photomask Technology 2019, edited by Jed H. Rankin, Moshe E. Preil, Proc. of SPIE Vol. 11148, 111480M · © 2019 SPIE · CCC code: 0277-786X/19/$21 · doi: 10.1117/12.2535912

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2. Performance Advantages

a. Resolution

Generally speaking, NIL resolution is determined by the mask making process. In recent years, mask resolution has been enhanced through the implementation of multi-beam writers which can aperture each individual element down to 10nm or below. Pictured in Figure 1 are examples of imprinted lines and spaces and contact holes. To date, 14nm lines and spaces have been imprinted with masks manufactured by both Dai Nippon Printing and Toshiba Memory Corporation.[10] In addition, production mask writers can now resolve contact hole arrays as small as 16nm. This type of resolution is important in particular for advanced DRAM devices as scaling continues over the next five years.

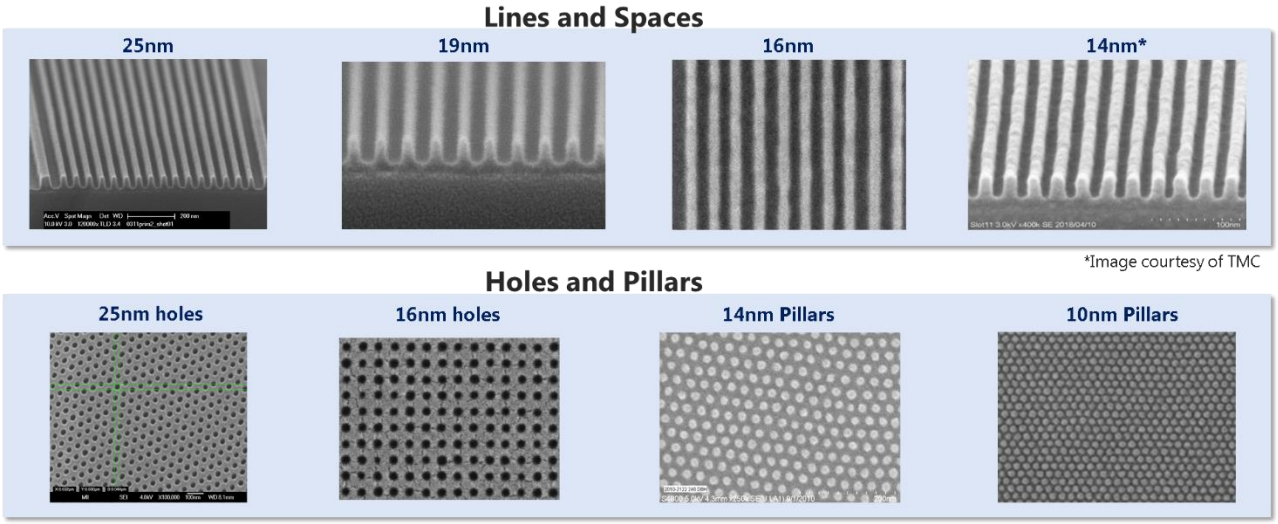


Figure 1. Line/space and contact hole resolution

b. Linewidth Roughness

It is well known that line edge and line width roughness (LWR) has an impact on transistor performance, affecting both threshold voltage and off state leakage.[11] Lithographic approaches such as extreme ultraviolet lithography (EUV) typically see excessive LWR values when using low dose resists. LWR can be reduced by increasing dose, but not without impacting throughput.

For NIL, LWR can be kept below 3nm by applying non-chemically amplified low sensitivity electron beam resists. Mask write time, especially when using multi-beam writers is still very acceptable. Shown in Figure 2 is a graph of linewidth roughness as a function of feature size. There is a virtually no change in LWR down to 14nm.

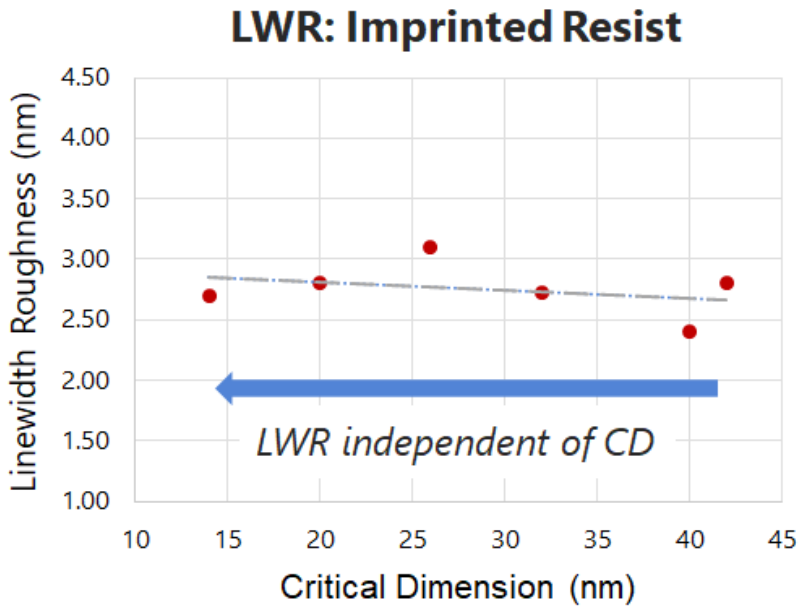


Figure 2. Linewidth roughness as a function of critical dimension. No degradation is observed down to 14nm.

c. Design Freedom

Because of resolution limitations for conventional lithography, two-dimensional patterning became much more restricted after the 65nm logic node and the 38nm 2D NAND Flash node. Lithography based patterning limitations forced the industry to adopt much stricter one-dimensional design rules which, in turn, impacted design complexity and device yield. NIL does not have these limitations, since resolution is limited only by what can be resolved in mask. Three different two-dimensional patterns are shown in Figure 3: a) a 38nm 2D NAND Flash gate level, b) a 2xnm SRAM cell, and c) a 1xnm DRAM test cell.

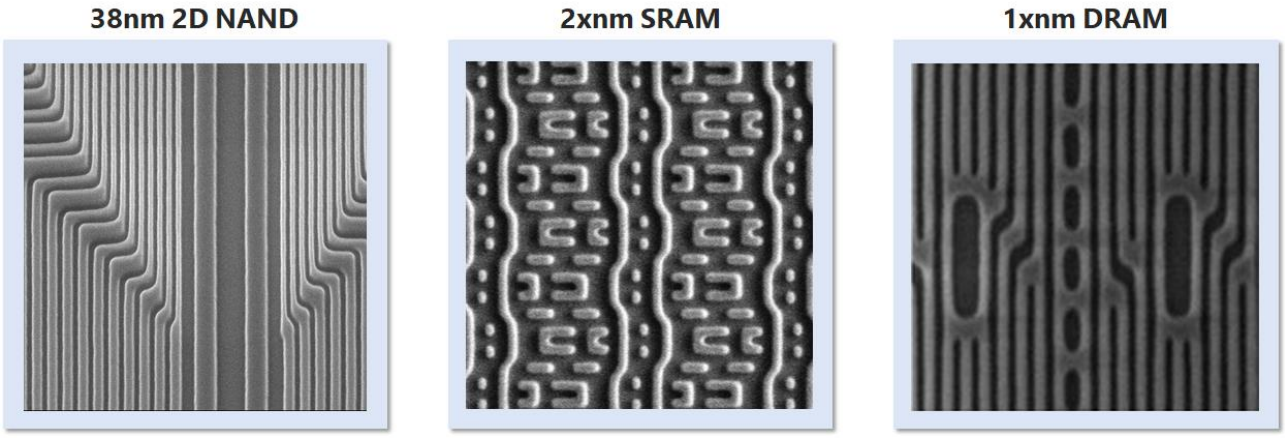


Figure 3: a) a 38nm 2D NAND Flash gate level, b) a 2xnm SRAM cell, and c) a 1xnm DRAM test cell.

It is interesting to note the design restrictions currently imposed by current multipatterning approaches that employ cut levels. Edge placement errors impact overlay budgets, and with the ability to avoid cutting levels, NIL has the potential to relax current overlay budgets, depending on the actual device level.

Furthermore, patterning capability is not restricted to two dimensions. Both the University of Texas and Toshiba Memory Corporation have demonstrated the ability to fabricate three dimensional structures, including a dual damascene example, as shown in Figure 4.[12,13]

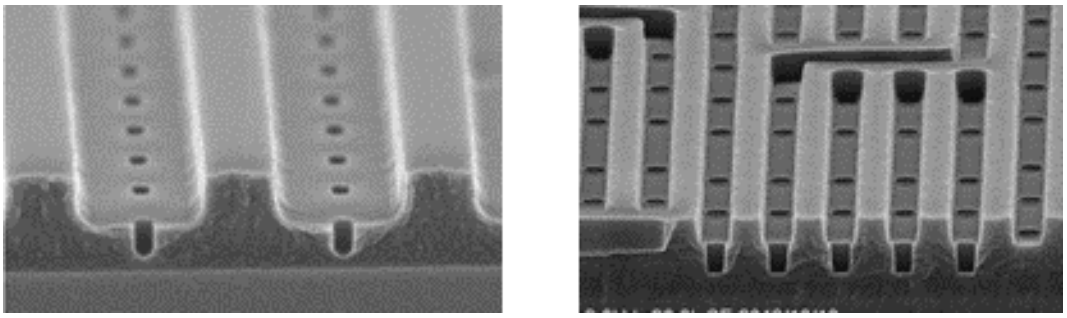


Figure 4. Three dimensional structures, including a dual damascene example.

3. Throughput

Throughput is one of the key contributors to cost of ownership. In this section, we discuss how throughput was enhanced to 90 wafers per hour and how the optimization of a resist filling simulation package contributes to making drop pattern generation more automated. Following that, we discuss how improvements in the alignment system help meet throughput targets.

a. Throughput and Resist Fill

Previous papers have discussed throughput breakdown in detail.[13] Overheads to the imprint TAKT time have been reduced by applying a multi-field dispense strategy, as opposed to dispensing and imprinting in a sequential fashion. The reduction in overhead is on the order of 0.24 seconds, resulting in an increase in throughput to 90 wafers per hour. Figure 5 shows that non-fill defectivity to nominally the same for the multi-field approach.

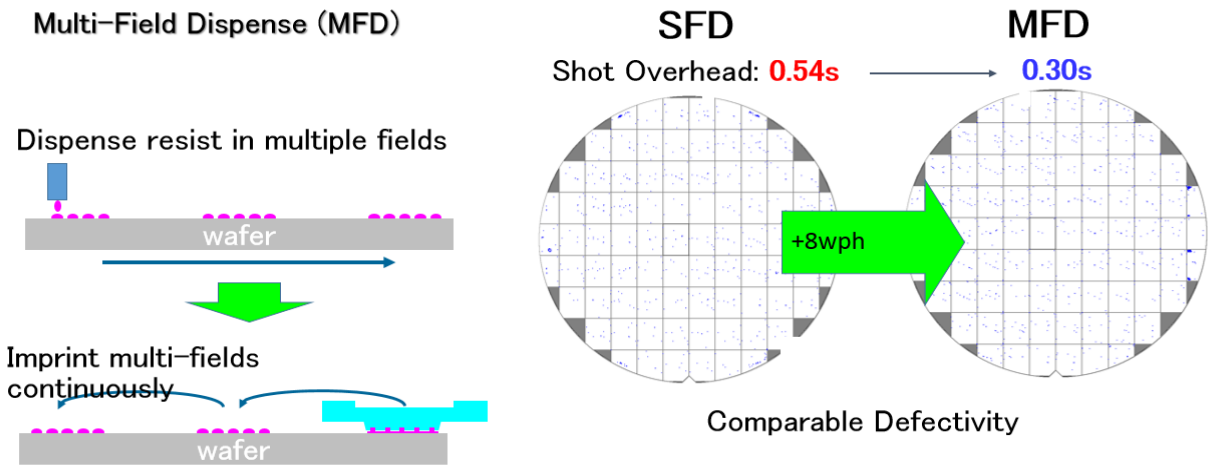


Figure 5. Defect inspection result comparison. The multi-field dispense results are comparable in defectivity to the sequential imprinting method.

Newly developed is a resist drop fill simulator designed to minimize fill time and reduce non-fill defects. The model must account for the dissipation of trapped gas between drops that causes non-fill defects. An example is shown in Figures 6. In Figure 6, the resist filling on a non-optimized drop pattern (left) is compared to an optimized resist drop pattern. After 1.1 seconds, it is apparent that the non-optimized pattern still has many non-fill areas. For the optimized pattern, the non-fill defectivity is reduced to zero after 1.1 seconds.

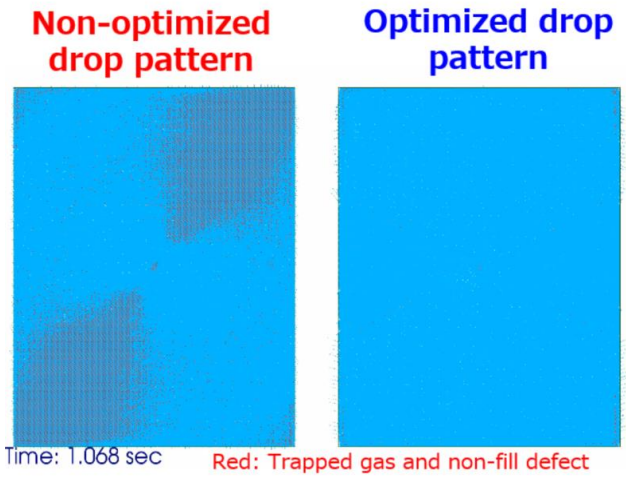


Figure 6. The resist filling on a non-optimized drop pattern (left) is compared to an optimized resist drop pattern. After 1.1 seconds, it is apparent that the non-optimized pattern still has many non-fill areas (areas in red). For the optimized pattern, the non-fill defectivity is reduced to zero after ~ 1.1 seconds.

4. Mask Life

NIL requires both a master mask and multiple copies of a replica mask. As a result, the gating item on cost for NIL the mask life of the replica mask. In 2017 the mask life target of 80 wafer lots was met. In 2019, Toshiba Memory Corporation has a demonstrated a mask life of over 300 lots (Figure 8).[14] The increase in mask life has been driven by a variety of techniques designed to mitigate particles in the wafer tool. The techniques cover source control, particle avoidance and particle collection, as shown in Figure 7. As a next step, we are considering the implementation of on-tool mask cleaning.

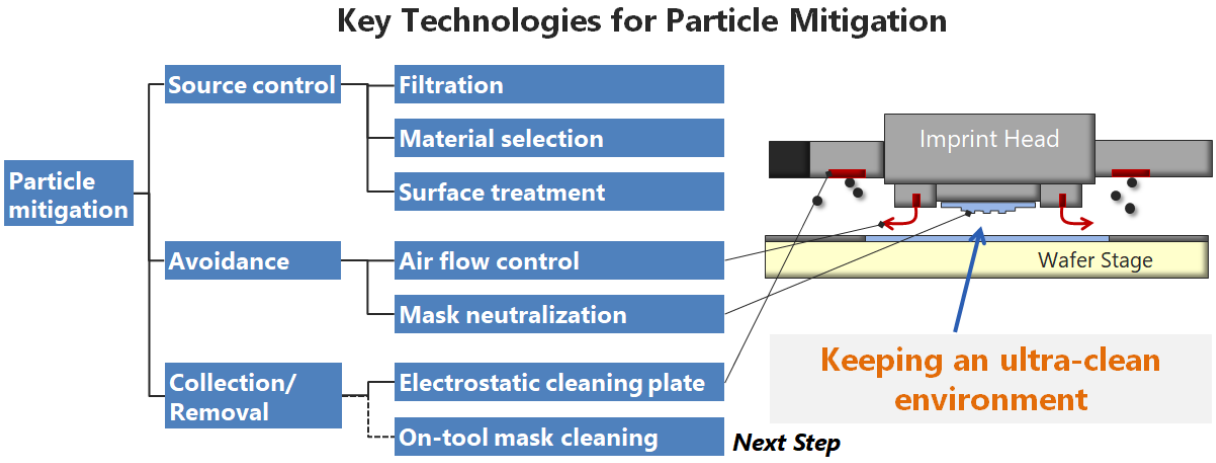


Figure 7. The increase in mask life has been driven by a variety of techniques designed to mitigate particles in the wafer tool. The techniques cover source control, particle avoidance and particle collection.

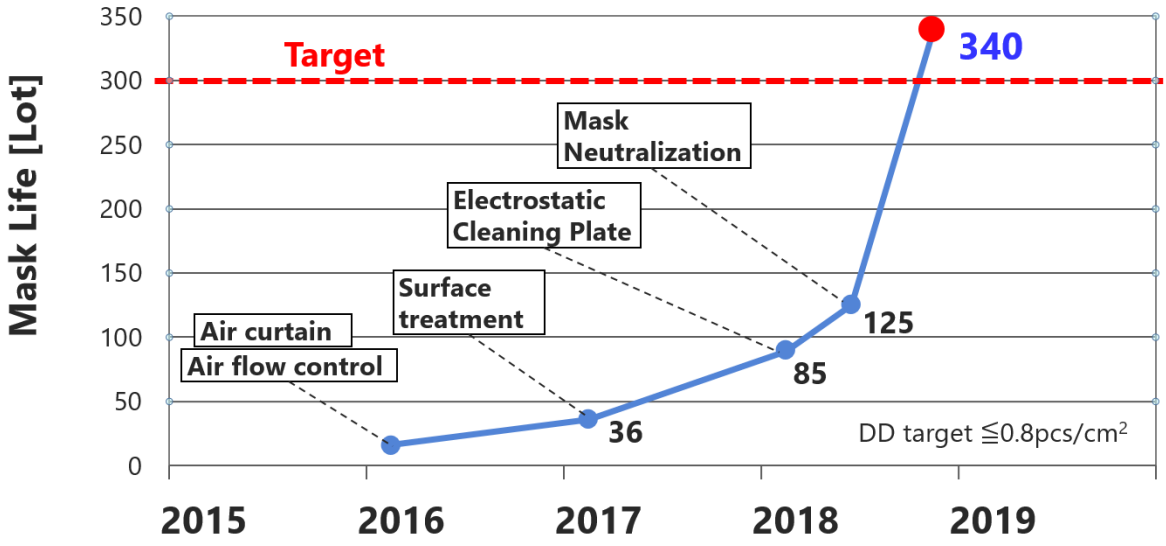


Figure 8. Mask life history. In 2019, Toshiba Memory Corporation has a demonstrated a mask life of over 300 lots.

5. Alignment and Overlay

a. Through The Mask (TTM) Alignment System

The NZ2C system employs a Through The Mask (TTM) alignment system as shown in Figure 9. First order terms are passed through Moiré marks on the mask and wafer with a sensitivity on the order of 1nm. On device wafers, it is possible to enhance the align signal and avoid blooming by using multiple wavelengths and controlling the intensity of each wavelength. The method aids in controlling signal variations, resulting in reduced measurement errors. The reader is referred to Reference 15 for more details on this subject.

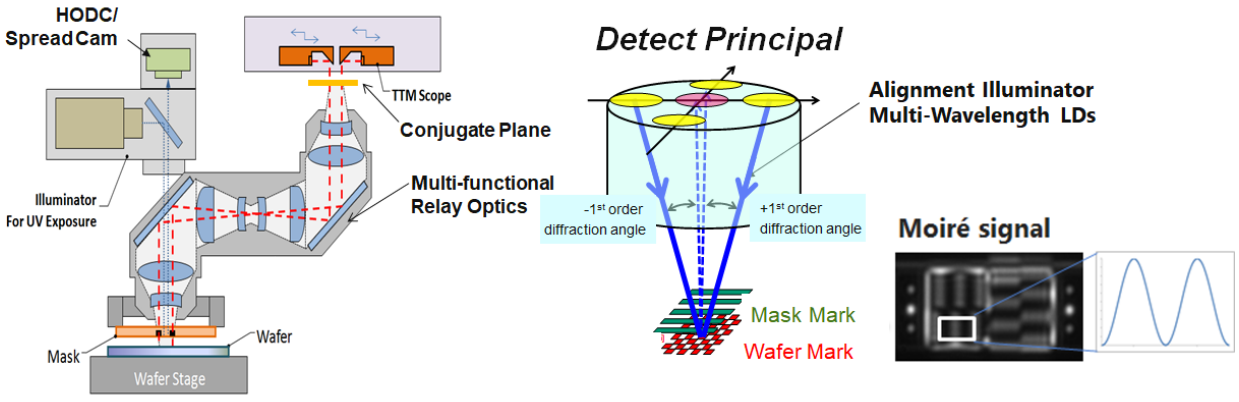


Figure 9. Through The Mask (TTM) alignment system

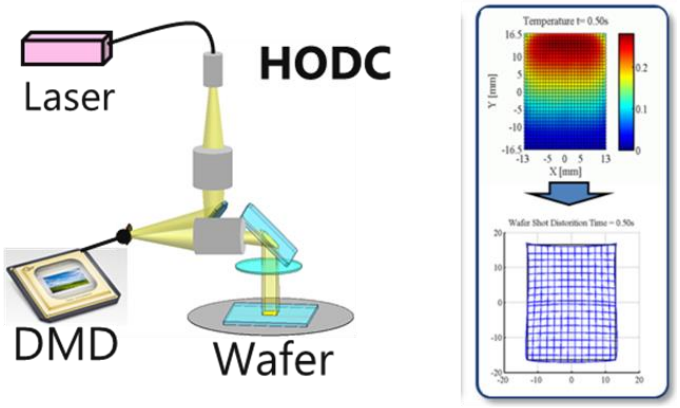
b. High Order Distortion Correction (HODC) System

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and

lens during the exposure process. A different approach is required for the imprint tool in order to do high order distortion controls (HODC). HODC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis

Heat input on a field by field basis is realized with DMD array which imparts heat through the mask onto a stepper field of a wafer. The basic operation of the system, along with initial results has been described in previous publications.[11,12] The system is shown schematically in Figure 10. By applying both the system magnification actuators and the HODC system, a cross matched machine overlay of better than 3.2nm was has been demonstrated.[15]



a b

Figure 10. a) Schematic drawing of the HODC system. b) Heat input needed to correct for existing distortion.

c. Drop Pattern Compensation

In a typical nanoimprint process, resist droplets are dispensed to fill all relief images on a mask and create a uniform residual resist film beneath below the imprinted features. Previously, we introduced a new method for addressing overlay distortion, in which a drop compensation pattern is applied to match wafer non-flatness and other distortions as a means for minimizing overlay errors.[16] The concept is illustrated in Figure 11, and shows a drop pattern designed to deliberately to create a varying resist film thickness which bends the fused silica mask and compensates the distortion introduced from either the silicon wafer or the wafer chuck. In this way, Drop Pattern Compensation (DPC) can be used to address lithography related distortion errors arising from:

- Chuck induced errors
- Pattern induced distortions
- Grid errors from a scanner
- Stress induced distortion
- Imprint related mask bending errors

By applying, the existing magnification actuator system, the heat-based HODC system and DPC, it now becomes possible to induce nanometer scale distortion corrections and address mix and match overlay errors. Two distortion correction examples are shown in Figures 12 and 13. Figure 12 is an example of how DPC can be applied to address Cross Matched Machine Overlay (XMMO) errors in which the first layer is patterned by an immersion scanner and the second is patterned using nanoimprint lithography. Figures 12a and 12b illustrate the existing field topography on a device-like wafer and the resulting overlay degradation after the nanoimprint process. By applying both HODC and DPC the ~5.4nm distortion error is reduced to 3.4nm in and 3.3nm in y.

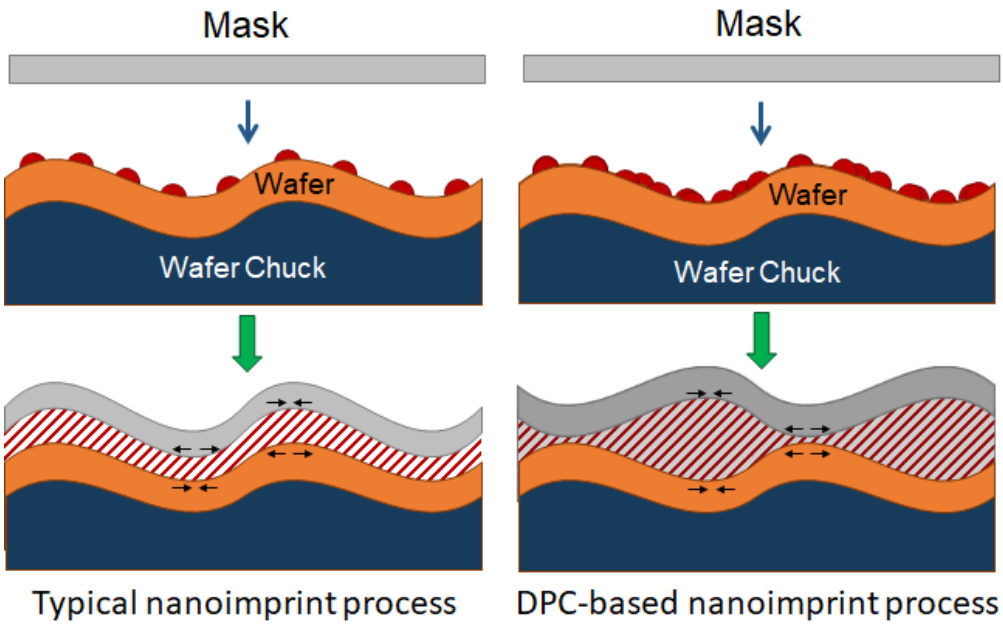


Figure 11. Left: Typical nanoimprint process. Right: DPC process, in which the residual resist film thickness is optimized to match mask and wafer bending

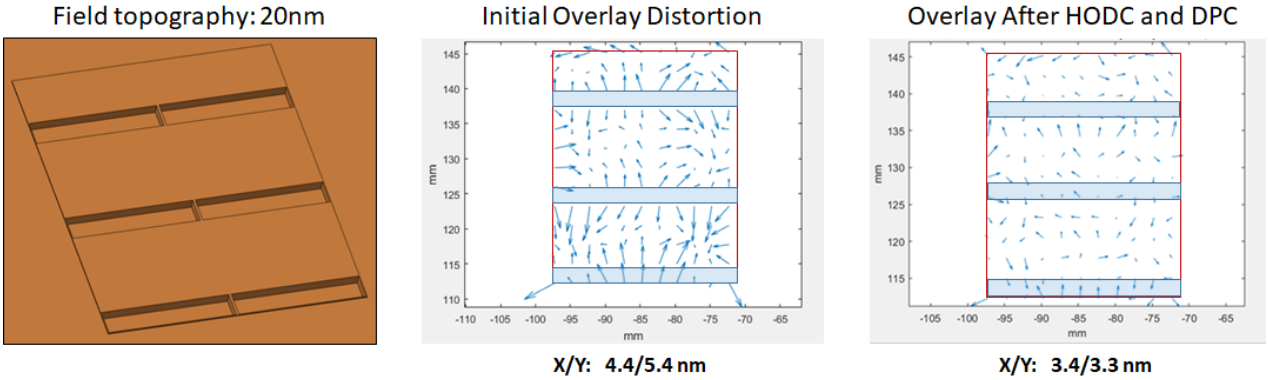


Figure 12. Cross matched machine overlay example: A 20nm topography within the field induces an overlay error of 4.4 nm in x and 5.4 nm in y. After applying both HODC and PDC, the error is reduced to 3.4 nm in and 3.3 nm in y.

The second example illustrates DPC correction applied to an imprint to imprint process, using two different masks and two different wafer chucks. Figure 3a shows the overlay distortion after the NIL process. Figure 3b depicts the DPC generated residual thickness variation applied to address the overlay errors. Figure 3c shows the expected overlay improvement. Finally, Figure 3d depicts the actual overlay after DPC is applied. The overlay error was reduced to 1.02 nm (mean + 3σ) in x and 1.03 nm (mean + 3σ) in y.

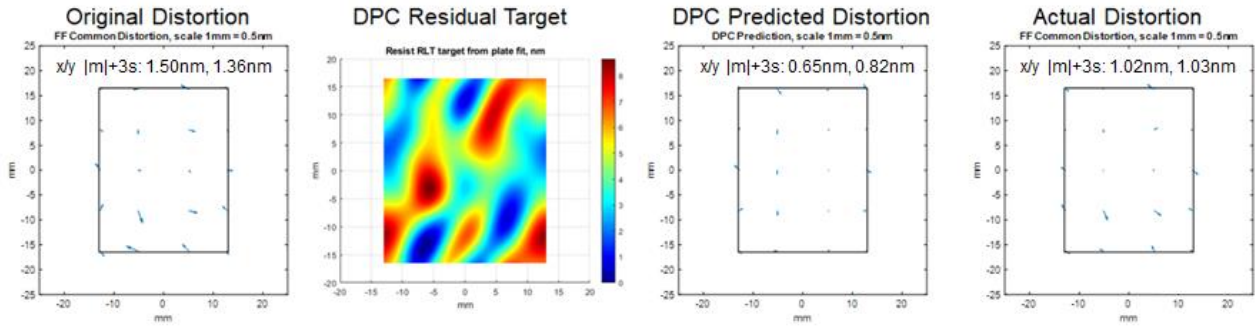


Figure 13: Imprint Mix and Match Overlay example: a) Initial overlay error is 1.50nm (mean + 3σ) in x and 1.36 (mean +3σ) nm in y. b) DPC residual resist thickness variation map. C) Expected overlay map after applying DPC. D) Actual overlay map after DPC. Overlay error was reduced to 1.02 nm (mean + 3σ) in x and 1.03 nm (mean + 3σ) in y.

4. Conclusions

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In this work, we have reviewed improvements to throughput, mask life and overlay. Using both the magnification actuators and the HODC system, XMMO of 2.9nm and 3.2nm in x and y respectively was demonstrated. Further improvements to overlay have been enabled through the applications of a drop compensation method which can be applied to address distortions arising from:

- Chuck induced errors
- Pattern induced distortions
- Grid errors from a scanner
- Stress induced distortion
- Imprint related mask bending errors

Improvements to both XMMO and IMMO were reported. Future studies will focus on refinements to the DPC approach in order to address the stringent overlay requirements of DRAM devices.

Acknowledgments

The authors would like to thank their colleagues in the support of this work. In additional, the authors would like to acknowledge the efforts of DNP and TMC.

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