Nanoimprint System Alignment and Overlay Improvement for High Volume Semiconductor Manufacturing

Yukio Takabayashi, Takehiko Iwanaga, Mitsuru Hiura, Hiroshi Morohoshi, Tatsuya Hayashi, Takamitsu Komaki

Canon Inc., 20-2, Kiyohara-Kogyodanchi, Utsunomiya-shi, Tochigi 321-3292 Japan

Abstract

Imprint lithography is an effective and well known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In this work, improvements to the alignment system, together with the High Order Distortion Correction (HODC) system have enabled better distortion and overlay results on both test wafers and device wafers. On test wafers, XMMO of 2.9nm and 3.2nm in x and y respectively was demonstrated. SMO of 2.2nm and 2.4nm was achieved, with an opportunity to further improve results by applying wafer chucks with better flatness specifications. Comparable results were also achieved on device wafers by applying a multi-wavelength alignment strategy and a feed forward strategy to realize align signal convergence within the allocated 0.60 second budget.

Keywords: nanoimprint lithography, NIL, alignment, overlay, XXMO, SMO, TTM, HODC

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.
Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In 2018, Hiura et al. reported a mix and match overlay (MMO) of 3.4 nm and a single machine overlay (SMO) across the wafer was 2.5nm using an FPA-1200 NZ2C four station cluster tool. These results were achieved by combining a magnification actuator system with a High Order Distortion Correction (HODC) system, thereby enabling correction of high order distortion terms up to K30.

Device wafers present a greater challenge, since the under layers on the wafer vary from level to level and cause degradation of alignment signals. The purpose of this paper is describe the improvements to alignment, overlay and throughput on both test wafers and device wafers.

2. Alignment and Overlay

a. Through The Mask (TTM) Alignment System

The NZ2C system employs a Through The Mask (TTM) alignment system as shown in Figure 1. First order terms are passed through Moiré marks on the mask and wafer with a sensitivity on the order of 1nm. On device wafers, it is possible to enhance the align signal and avoid blooming by using multiple wavelengths, and controlling the intensity of each wavelength. The method aids in controlling signal variations, resulting in reduced measurement errors. The impact of this upgrade is discussed in more detail in Section 3d.

![Through The Mask (TTM) alignment system](image)

Figure 1. Through The Mask (TTM) alignment system

b. High Order Distortion Correction (HODC) System

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and lens during the exposure process. A different approach is required for the imprint tool in order to do high order distortion controls (HDOC). HDOC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis
Heat input on a field by field basis is realized through the use of DMD array which imparts heat through the mask onto a stepper field of a wafer. The basic operation of the system, along with initial results has been described in previous publications. The system is shown schematically in Figure 2.

Figure 2. a) Schematic drawing of the HODC system. b) Heat input needed to correct for existing distortion.

c. Test Wafer Results

The TTM and HODC systems were applied to test wafers and the results are reported in Figure 3 and 4. Figure 3 depicts Cross Matched Machine Overlay (XMMO) on an existing level patterned with an ASML 1950 ArF immersion tool. A total of 84 fields were measured, including twelve points per field. The results are an average across 23 wafers. XMMO of 2.9nm and 3.2nm mean plus three sigma was achieved in x and y, respectively.

**Cross Matched Machine OL : NIL to ArFi**

![Cross Matched Machine OL: NIL to ArFi](image)

Figure 3. XMMO using an FPA-1200 NZ2C imprint system. XMMO of 2.9nm and 3.2nm mean plus three sigma was achieved in x and y, respectively

Similarly, Figure 4 depicts Single Machine Overlay on an existing level patterned with the FPA-1200 NZ2C tool. A total of 84 fields were measured, including twelve points per field. The results are an average across three wafers. SMO of 2.2nm and 2.4nm mean plus three sigma was achieved in x and y, respectively. Residual distortions were 0.7nm, mean plus three sigma.
Figure 4. SMO using an FPA-1200 NZ2C imprint system. SMO of 2.2nm and 2.4nm mean plus three sigma was achieved in x and y, respectively.

It is important to note that distortions are greater nearer the edge for this SMO test. Figure 5 breaks out full field overlay and partial field overlay for one particular test wafer. The full field overlay errors are on the order of 2.1nm. The partial field errors are closer to 3.5nm, on average.

The reason for the difference is primarily due to the two chucks used in this experiment within a multi-station NZ2C system, as shown in Figure 6. The chuck used to pattern the zero level had greater flatness errors, and the errors were greatest near the wafer edge when compared to the chuck used to pattern the following level. The flatness error corresponds to a Chuck Flatness Induced Distortion (CFID) on the order of 3.0nm, consistent with the high overlay.
errors observed near the wafer edge. In the future, the newer chuck design will be applied to reduce overlay errors in all fields and also generate Dedicated Chuck Overlay (DCO) results.

Figure 6. Chuck flatness induced distortion explains the higher overlay errors observed near the wafer edge.

d. Device Wafer Results

Improvements to the alignment system were realized by moving to a dipole illumination system and optimizing the intensities of multiple wavelengths in the TTM system. The results are shown step by step in Figure 7. Plotted is alignment error for both a test wafer and a device wafer. After applying a dipole illumination scheme and a multi-wavelength strategy, the error signals are nearly equivalent between the test wafer and device wafer.

Figure 7. After applying a dipole illumination scheme and a multi-wavelength strategy, the error signals are nearly equivalent between the test wafer and device wafer.

Further verification of the improvements were observed by mapping the higher order distortion terms up to K30 as shown in Figure 8. Plotted are the errors for each term without any HODC correction, correction on a test wafer and a final correction on a device wafer. Very little difference is observed between the test wafer and the device wafer.
3. Throughput

Throughput is one of the key contributors to cost of ownership. In this section, we discuss how throughput was enhanced to 90 wafers per hour and how the optimization of a resist filling simulation package contributes to making drop pattern generation more automated. Following that, we discuss how improvements in the alignment system help meet throughput targets.

### a. Throughput and Resist Fill

Previous papers have discussed throughput breakdown in detail. Overheads to the imprint TAKT time have been reduced by applying a multi-field dispense strategy, as opposed to dispensing and imprinting in a sequential fashion. The reduction in overhead is on the order of .24 seconds, resulting in an increase in throughput to 90 wafers per hour. Figure 9 shows that non-fill defectivity to nominally the same for the multi-field approach.

Figure 9. Defect inspection result comparison. The multi-field dispense results are comparable in defectivity to the sequential imprinting method.
Newly developed is a resist drop fill simulator designed to minimize fill time and reduce non-fill defects. The model must account for the dissipation of trapped gas between drops that causes non-fill defects. An example is shown in Figures 10. In Figure 10, a filling simulation is compared to actual field inspection results after ~ 0.66 seconds. The red points in each image indicate a non-fill area. There is good agreement in the non-fill defect pattern for each case. Further simulations on an optimized resist drop pattern show non-fill defectivity trending to zero after a fill time of 1.1 seconds, in excellent agreement with actual fill time results.

![Filling Simulation vs Actual Fill Time Defectivity](image)

Figure 10. Comparison of non-fill defectivity for the drop simulation package and actual fill time results.

### b. Alignment Control

A final consideration for the alignment system is the time required for the align signal to converge for each field. This is important because alignment and resist fill are done in parallel. The budget assigned for alignment is 0.60 seconds. To minimize this budget the new TTM strategy was applied along with a feed forward scheme. On a test wafer align signal convergence is completed on 0.50 seconds, as shown in Figure 11a. When applied to a device wafer, convergence is done after 0.60 seconds, meeting the convergence budget.

![Test Wafer vs Device Wafer Alignment](image)

Figure 11. Alignment convergence for a test wafer and a device wafer. On the device wafer, convergence occurs within the 0.60 seconds allocated.
4. Conclusions

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In this work, improvements to the alignment system, together with the High Order Distortion Correction (HODC) system have enabled better distortion and overlay results on both test wafers and device wafers. On test wafers, XMMO of 2.9nm and 3.2nm in x and y respectively was demonstrated. SMO of 2.2nm and 2.4nm was achieved, with an opportunity to further improve results by applying wafer chucks with better flatness specifications. Comparable results were also achieved on device wafers by applying a multi-wavelength alignment strategy and a feed forward strategy to realize align signal convergence within the allocated 0.60 second budget.

Acknowledgments

The authors would like to thank their colleagues in the support of this work. In additional, the authors would like to acknowledge the efforts of DNP and TMC.

References