Topography and Flatness Induced Overlay Distortion Correction using Resist Drop Pattern Compensation in Nanoimprint Lithography Systems

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Abstract

Imprint lithography is a promising technology for replication of nano-scale features. For semiconductor device applications, Canon deposits a low viscosity resist on a field by field basis using jetting technology. A patterned mask is lowered into the resist fluid, which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Overlay budgets play a large role in defining production readiness. As an example, DRAM devices require overlay on the order of 20% of the half pitch. Canon uses a through the mask (TTM) alignment system to measure a Moiré image anywhere in the field. This system can also record alignment errors of all fields and all marks. The data collected by the TTM system correlates very closely with an Archer measurement tool. In addition, a High Order Distortion Correction (HODC) system, which applies a heat input on a field by field basis through the use of a DMD array has been combined with magnification actuators to correct high order distortion terms up to K30.

There is an additional distortion term that must also be addressed for the case of nanoimprint lithography. NIL drop patterns are typically designed to minimize resist fill time and create a uniform residual layer beneath the resist pattern. For device wafers, however, it is important to recognize that there are both long wavelength flatness errors coming from the wafer chuck and existing pattern topography from previously patterned levels that cause out of plane errors. When the mask comes in contact with the resist on the wafer, these out of plane errors can then induce mask bending, resulting in an additional distortion term.

To minimize this distortion, a Drop Pattern Compensation (DPC) Model has been implemented to minimize the added distortion terms. In this paper we describe the origins of the out of plane errors, and describe the model used to correct these errors along with some examples. Finally, results are presented for a device like wafer in which the overlay errors within a field are reduced from 5.4nm to 3.4nm, 3 sigma.

Keywords: nanoimprint lithography, NIL, overlay, HODC, drop pattern compensation, DPC

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features.1,2 Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.3-9 The patterned mask is lowered into the fluid, which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the
cost of the tool, when combined with simple single level processing and zero waste, leads to a cost model that is very compelling for semiconductor memory applications.

With respect to throughput, Hamaya et al. recently reported a multi-field dispense strategy to increase throughput to 90 wafers per hour for an NZ2C NIL four station tool. With respect to throughput, Hamaya et al. recently reported a multi-field dispense strategy to increase throughput to 90 wafers per hour for an NZ2C NIL four station tool.11

On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6” x 6” x 0.25” photo masks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6” x 6” x 0.25” fused silica was recently reported to have a defectivity of only 0.04/cm² as measured by a Lasertec tool with 50 nm sensitivity.12 Presently, Ichimura et al. have exceeded the targets for both CDU and IP. In addition, master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20nm have been fabricated.13

Overlay budgets play a large role in defining production readiness. As an example, DRAM devices require overlay on the order of 20% of the half pitch. Canon uses a through the mask (TTM) alignment system to measure a Moiré image anywhere in the field. This system can also record alignment errors of all fields and all marks. The data collected by the TTM system correlates very closely with an Archer measurement tool.

In addition, a High Order Distortion Correction (HODC) system, which applies a heat input on a field by field basis through the use of a DMD array has been combined with magnification actuators to correct high order distortion terms up to K30. A schematic of the HODC system is shown in Figure 1. Hiura et al. applied the system to demonstrate cross matched machine overlay (XMMO) and single machine overlay (SMO) of 3.4nm and 2.5nm respectively.14

![HODC Configuration](image)

**Figure 1.** a) Schematic drawing of the HODC system. b) Heat input needed to correct for existing distortion.

There is, however, an additional distortion term that must also be addressed for the case of nanoimprint lithography. NIL drop patterns are typically designed to minimize resist fill time and create a uniform residual layer beneath the resist pattern. For device wafers, however, it is important to recognize that there are both long wavelength flatness errors coming from the wafer chuck and existing pattern topography from previously patterned levels that cause out of plane errors. When the mask comes in contact with the resist on the wafer, these out of plane errors can then induce mask bending, resulting in an additional distortion term.

To minimize this distortion, a Drop Pattern Compensation (DPC) Model has been implemented to minimize the added distortion terms. In this paper we describe the origins of the out of plane errors, and describe the model used to correct these errors along with some examples. Finally, results are presented for a device like wafer in which the overlay errors within a field are reduced from 5.4nm to 3.4nm, 3 sigma.
2. Origin of Out of Plane Errors

The NIL process has five general steps to be completed. i) Dispense a low viscosity UV curable resist onto the wafer. ii) Align the mask to the dispensed drops to minimize overlay error. iii) Contact the mask with the wafer. iv) Wait for capillary fill and UV expose. v) Safely separate the mask without defects. During the NIL process, many technological efforts to minimize overlay errors are made, such as a through the mask (TTM) alignment system, a magnification/shape control system (MSCS), and a high order distortion correction system (HODC). These systems have demonstrated that in-plane overlay errors can be reduced significantly. However, there exists an additional distortion term which cannot be resolved by these systems. Although the NIL process requires a mask to remain perfectly flat in step 4, during the actual process, out-of-plane distortion is observed. One topographical cause of this distortion is wafer and wafer chuck flatness; another is existing patterned wafer topography.

Figure 2 illustrates the mask and wafer conforming process for each topographical mode. Since a resist layer thickness is uniform across a NIL stepper field, the mask inevitably follows wafer topography. Figure 2 (a) and (b) show the mask and wafer geometry before the mask comes into contact. In Figure 2 (c), flatness errors of the wafer and wafer chuck result in mask bending. This out-of-plane distortion results in bending strain mismatch at the mask-wafer interface, causing in-plane overlay (OL) error, as depicted by the direction of the arrows at the interface. Figure 2 (d) shows mask bending due to patterned wafer topography with half-wavelength on the order of 1 mm or larger, which also contributes to OL error.

An example due to topography induced OL distortion is shown in Figure 3. The OL distortion images represent two sets of data: on a flat wafer and a programmed topography wafer (~20nm deep trench) shown in the middle image. Compared to a flat wafer, the OL distortion vectors align normal to the boundary of the wafer trench, which causes a 3.5nm OL degradation in the y-direction.
3. Drop Pattern Compensation Model

In this study, resist drops are used to remove non-flatness and pattern induced distortions to minimize mask bending. To prevent additional distortion from mask bending, drop patterns are modified by adding or relocating drops to accommodate topography variation. Figure 4 illustrates how to prevent mask bending by using the modified drop patterns. The resist layer has a non-uniform thickness, depending on wafer topography, rather than a uniform thickness. Even though the mask remains flat by drop compensation, out of plane distortion may still exist due to wafer or wafer chuck non-flatness, resulting in uncompensated in-plane error at the wafer top surface. Further improvement can be realized with a favorable mask bending shape shown in Figure 5. In this case, mask bending compensates the non-flatness induced overlay errors to achieve a near-zero bending strain mismatch.
Figure 5. Drop Pattern for Favorable Mask Bending

a. Model Basics

A classic plate bending model is used to capture chucked wafer topography as shown in Figure 6. From a geometric perspective, in-plane distortions ($\Delta x$, $\Delta y$) are calculated from the out of plane displacement ($z(x,y)$) by relating them via the local slope:

$$\Delta x = \frac{t \cdot \partial z}{2 \cdot \partial x}, \quad \Delta y = \frac{t \cdot \partial z}{2 \cdot \partial y},$$

where $t$ is mask thickness.

Additionally, once in-plane distortions (i.e., OL distortions) are measured, out of plane displacement (i.e., the mask bending shape that follows the wafer topography) can be estimated from the equations. This model agrees well with finite element analysis and was also verified with interferometer (Zygo) flatness measurements.

Figure 6. Plate bending model.
To estimate the mask shape from OL data, out of plane distortion needs to be defined using basis functions. Since the NIL pattern is defined within a rectangular domain (~26mm x 33mm) and topography of the wafer is a mostly periodic pattern, 2D Fourier functions are used in this study. A linear combination of basis functions is used to estimate the mask bending shape.

\[
z(x, y) = \sum_{m,n=0}^{\infty} \left[ \left( a_{mn} \cos \frac{m\pi x}{L} \cdot \sin \frac{m\pi y}{H} \right) + \left( b_{mn} \cos \frac{m\pi x}{L} \cdot \cos \frac{m\pi y}{H} \right) \right] + \left[ \left( c_{mn} \sin \frac{m\pi x}{L} \cdot \sin \frac{m\pi y}{H} \right) + \left( d_{mn} \sin \frac{m\pi x}{L} \cdot \cos \frac{m\pi y}{H} \right) \right]
\]

Where;

- \(a, b, c, d\) are Fourier coefficients
- \(m, n\) are the number of basis modes
- \(L\) is half width of the imprint domain
- \(H\) is half height of the imprint domain

Figure 7 illustrates a NIL stepper field and selected two dimensional mode shapes for that field. The mode shapes in Figures 7 (b) – (f) were generated from the Fourier basis functions by varying \(m\) and \(n\).

Figure 7. (a) NIL stepper field and (b)-(f) examples of mode shapes of 2D Fourier function

b. Model Examples

Figure 8 (a) shows the OL distortion vectors of a whole wafer by stitching field by field OL data. 143 overlay errors (11x13 array) at each field are measured using a KLA-Tencor Archer metrology tool. After removing align correctible terms, the mask bending model can be applied to the residual distortion to estimate wafer chuck flatness as shown in Figure 8 (b). The model clearly shows a chuck flatness error signature ranging +/- 30nm on a field by field basis. The
wafer chuck induced OL error contribution is estimated from this model at 2.4nm in the x-direction and 3.0nm in the y-direction.

![Figure 8. Wafer Chuck Flatness Estimation](image)

4. Results: Device-like Wafer

The performance of drop pattern compensation (DPC) is evaluated using device-like wafers. First, a wafer is imprinted using an initial drop pattern which is created for a uniform resist layer. Next, the alignment and process signatures are removed from the OL data gathered from the initial imprint step. The mask bending model can then be applied to the residual distortion, which contains the topography induced distortion, to obtain the wafer topography map. Based on the wafer topography map, a new optimized drop pattern is generated using a drop generation algorithm developed by Canon, compensating for the topography induced OL distortion. Then the DPC process is repeated until the OL distortion target meets specification. Figure 9 shows the DPC process flow.

![Figure 9. DPC Process Flow](image)

To demonstrate DPC, simple basis modes are tested on a flat wafer. Each Fourier basis function has its unique shape, as shown in Figure 7 (b) - (f). The mode shape in Figure 7 (c) was selected as a test case. Figure 10 shows the target shape correction for this case, producing a range in resist layer thickness from 0nm to 25nm within the 26mm x 33mm field. A drop pattern is generated to produce the target shape, and a blank mask is then imprinted on a flat wafer to verify the drop pattern. An ellipsometer is used for confirmation of actual the resist layer thickness, as shown in Figure 10. The ideal OL distortion that is expected to result from this test case was calculated using the mask bending model. Figure 10 shows the ideal OL distortion, and the actual OL distortion obtained when imprinting the drop pattern using a mask and wafer with 143 overlay marks in the field. OL distortion vectors of the actual case agree well with the ideal case.
Figure 10. Mask Bending Induced Distortion

Figure 11 demonstrates how DPC improves OL distortion for a device-like wafer. In this example, mix and match overlay (MMO) was originally 5.4nm. When a first DPC model is used, overlay reduces the error down to 4.6nm. After applying HODC, the error was further reduced to 4.1nm. A final DPC process achieves 3.4nm MMO.
5. Conclusions

Drop pattern compensation (DPC) was developed to address out of plane distortion errors for NIL in order to obtain the best possible overlay results. DPC can correct for both pattern topography and flatness induced OL distortions and is complementary with HODC technology. Existing dispense technology developed by Canon is also leveraged by DPC. The model has demonstrated that HODC and DPC can address the challenges of mix and match overlay distortion signatures and be applied to device wafers in order to meet the overlay requirements of advanced device architectures.

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References