Progress in Nanoimprint Wafer and Mask Systems for High Volume Semiconductor Manufacturing

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ABSTRACT

Nanoimprint lithography manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

In this paper, we review the progress and status of the FPA-1200NZ2C wafer imprint system and FPA-1100NR2 mask replication system. To address high volume manufacturing concerns, an FPA-1200NZ2C four-station cluster tool is used in order to meet throughput and cost of ownership requirements (CoO). Throughputs of up to 90 wafers per hour were achieved by applying a multi-field dispense method. Mask life of up to 81 lots, using a contact test mask were demonstrated. A mix and match overlay of 3.4 nm has been demonstrated and a single machine overlay across the wafer was 2.5nm.

There is Mask Replication criteria that are crucial to the success of a replication platform include image placement (IP) accuracy and critical dimension uniformity (CDU). Data is presented on both of these subjects. With respect to image placement, an IP accuracy (after removing correctables) of 0.8nm in X, 1.0nm in Y has been demonstrated.

Keywords: Nanoimprint Lithography, NIL, CoO, defectivity, throughput, overlay, image placement accuracy, mask replication

1. INTRODUCTION

Imprint lithography is an effective and well known technique for replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both critical dimension uniformity (CDU) and line edge roughness

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meet the criteria of 2nm. A collaboration partner achieved overlay of 10nm (with a target of 8nm) and defect levels ~ 5/cm^2 across a lot of 25 wafers.[10] Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether CoO requirements can be met. Recently, Takeishi and Sreenivasan reported that a throughput of 40 wafers per hour was achieved on a four-station imprint tool.[11]

On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photo masks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was recently reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50 nm sensitivity.[12]

The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. In 2012, an MR-5000 mask replication tool was developed specifically to pattern 6" x 6" x 0.25" replica masks from an e-beam written master. Previous work by Ichimura et al. using this tool, demonstrated that a CDU of less than 1.5nm 3-sigma can be achieved on both the master and replica masks.[13]

As the most aggressive features in advanced memory designs continue to shrink below 15 or 16 nm (towards 1Z nm), the cost of fabricating these devices increases because of the large number of additional deposition, etch and lithographic steps necessary when using immersion lithography.[14] NIL offers a more attractive CoO than competing technologies. Cost benefits can be realized by:

- Enabling direct printing of the features of interest, without the need for multiple patterning techniques.
- Improved mask life that allows a replica mask to be used for more than 2000 wafers.
- By improving the throughput of the NIL tool

In this review paper, we focus on improvements to both the wafer imprint tool, and mask replication tool.

2. Wafer Nanoimprint Tool

2.1 Throughput

There are several parameters that can impact resist filling. Key parameters include resist drop volume (smaller is better), system controls (which address drop spreading after jetting), Design for Imprint or DFI (to accelerate drop spreading) and material engineering (to promote wetting between the resist and underlying adhesion layer). In addition, it is mandatory to maintain fast filling, even for edge field imprinting. Previously, we have demonstrated that it is feasible to fill dense line/space patterns in only one second.

The resist properties have a large impact on fill time and the engineering of the resist is critical for meeting performance criteria and properties such as surface tension, viscosity and wetting. Surface wetting has a strong influence on fill time. To enhance drop spreading after dispense and achieve a throughput of 80 wafers per hour, a two component resist system is used to create a surface tension gradient to drive resist flow. The approach is similar to Marangoni flow, which is driven by surface tension gradients. The process consists of three basic steps:

- In the first step, the first component of the imprint resist is spin coated with a pre-determined surface tension.
- In the second step, the second resist component is jetted and has a lower surface tension than that of the first component.
- In the final step, the second resist component quickly spreads along the surface while intermixing with the first component, thereby forming a new resist film.

An example of this effect is shown in Figure 1. For additional details on this process, the reader is referred to the paper by N. Khusnatdinov et al.[15]

Figure 1. Difference in drop diameter between the standard jetted resist, and the two component resist system.

To further increase throughput, a multi-field dispense (MFD) method has been developed in which resist is jetted onto several fields in order to decrease the overhead resulting from a sequential dispense and imprint process flow. The improvement to 90 wafers per hour is shown in a graph of throughput (for a four-station cluster tool) as a function of year. The next target is > 100 wafers per hour.

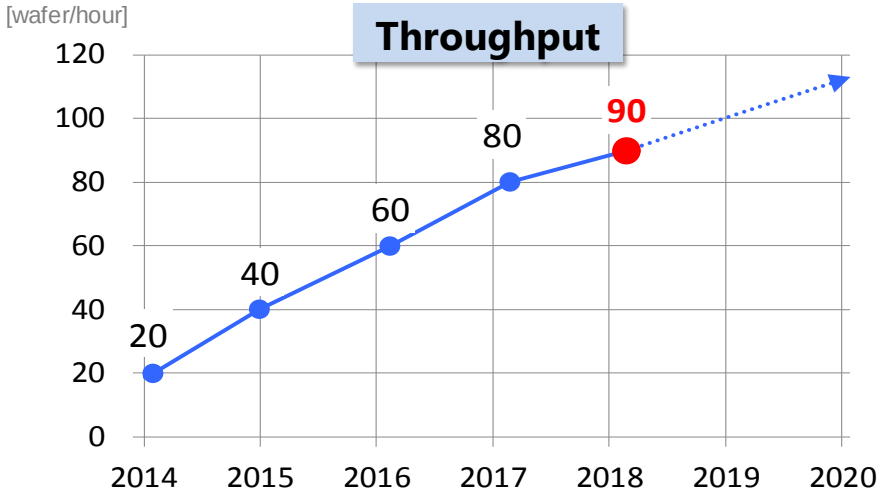


Figure 2. A two component resist system, which enhances resist spreading enabled throughputs up to 80 wph. Using a multi-field dispense method, throughputs of 90 wph have now been demonstrated.

2.2 Overlay

The alignment and overlay system consists of various factors, which can be categorized generally as alignment and distortion. Canon uses two key systems to address overlay (Figure 3):

- A through the mask (TTM) align system and a magnification actuator system which applies force through an array of piezo actuators to correct for magnification, skew and trap errors
- A High Order Distortion Control (HODC) system which locally varies the heat within a stepper field on the wafer to correct higher order distortions.

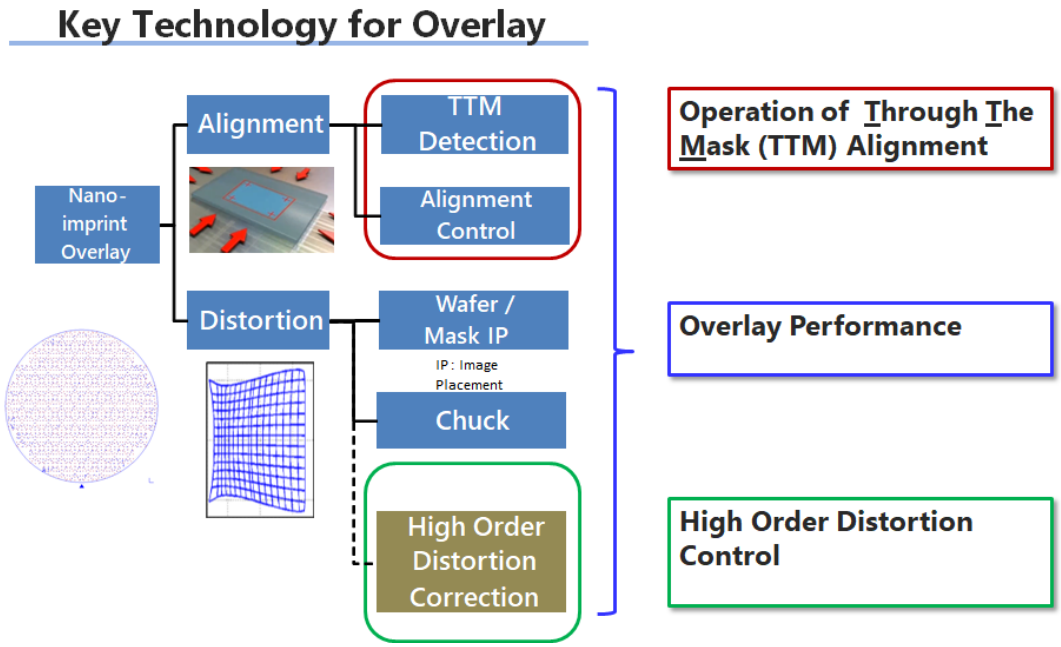


Figure 3. Schematic representation of the methodology for addressing overlay with a nanoimprint lithography tool. Key components include the TTM detection system and the HODC system.

The system has now been used to correct distortion terms up to K30 as shown in Figure 4.[16]

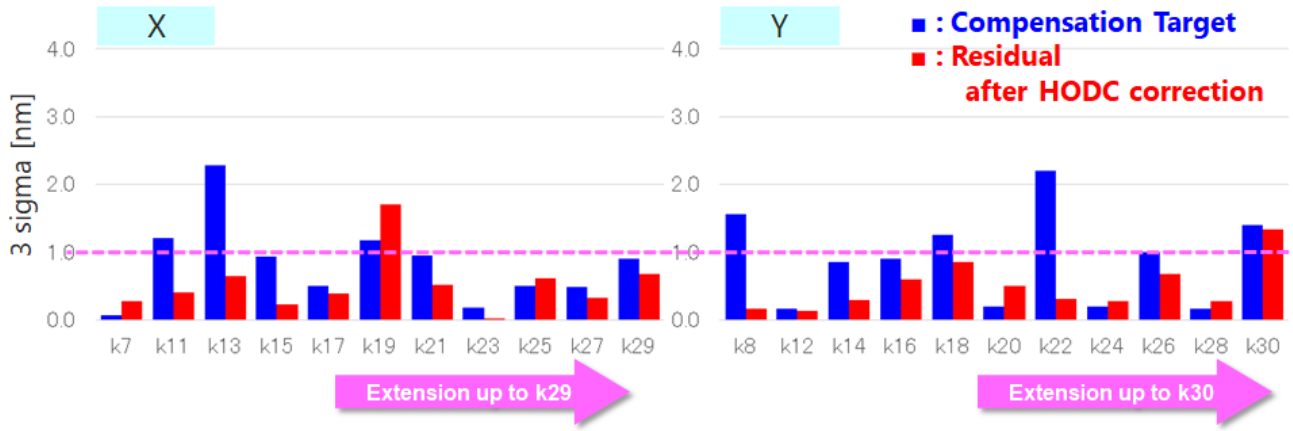


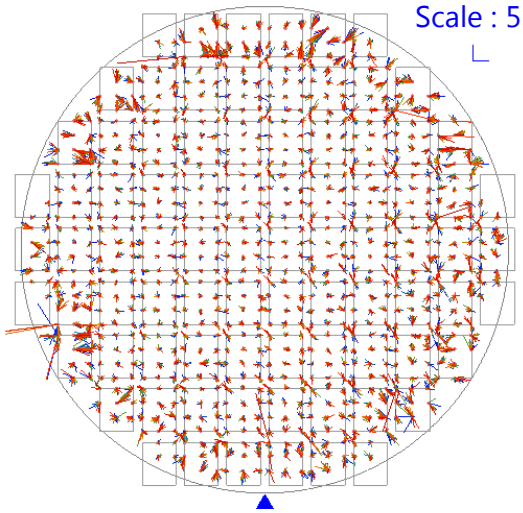
Figure 4. Correction of a field containing multiple higher order distortions. Residuals are reduced to less than ~1nm.

2.3 System Performance

As a final test, matched machine overlay (to an ASML ArFi scanner) and single machine overlay measurements (NZ2C to NZ2C) were done to characterize the NZ2C performance. Both tests were done by measuring the overlay of all 84 fields (including partial fields), 12 measurement points per field. The results are shown in Figures 5 and 6, respectively. For the MMO case, the average + 3 sigma was 3.4nm in both x and y. For the SMO case, the average + 3 sigma in x and y was 2.5nm and 2.4nm, respectively.

MMO : Mix and Match Machine Overlay

Wafer Map



MMO	X	Y
Average	0.0	0.0
3σ	3.4	3.4
Ave.+3σ	3.4	3.4

[nm]

Ideal case without correctable 1st layer wafer image placement by scanner tool

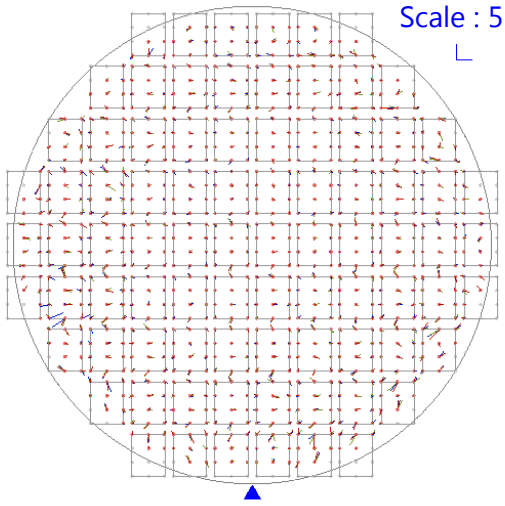
■ **Conditions**

- FPA-1200 NZ2C
- Device like Patterned Mask
- **NIL to ArF-IML 1st Layer**
- 12 measure points/field
  84 fields/wafer
- **23 wafers**

Figure 5. Matched machine overlay performance.

SMO : Single Machine Overlay

Wafer Map



SMO	X	Y
Average	0.0	0.0
3σ	2.5	2.4
Ave.+3σ	2.5	2.4

[nm]

Ideal case without correctable 1st layer wafer image placement by scanner tool

■ **Conditions**

- FPA-1200 NZ2C
- NIL-NIL Test Mask
- **NIL to NIL 1st Layer after Si etching process**
- 12 measure points/field
  84 fields/wafer
- **3 wafers**

Figure 6. Single machine overlay performance.

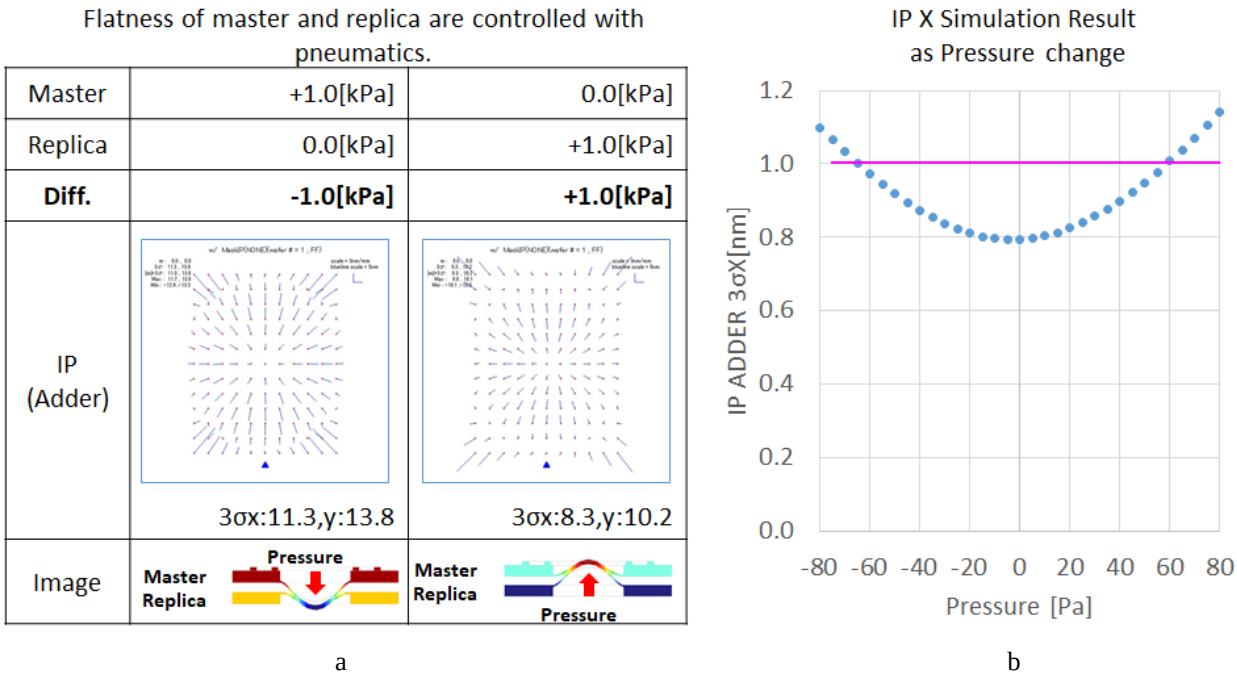
3. Mask Replication

In 2017, the new FPA-1100NR2 mask replication tool, which meets the target for the 1Z nm generation of devices, was shipped to a customer site. Target specifications are shown in Table 1.

Target Specifications		
Throughput	4	Mask/hour
CD Uniformity (3σ) (Adder)	0.8	nm
Image PlacemenAccuracy (3σ) (Adder)	1.0	nm
Particle	0.002	pcs/Mask

Table 1. Target specifications for the NR2 mask replication tool.

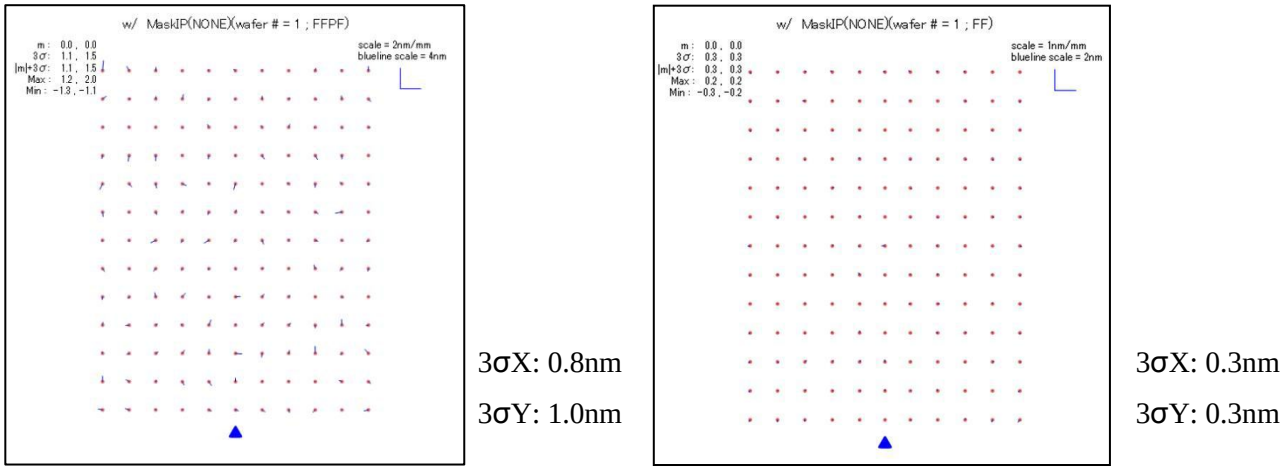
To optimize image placement accuracy, we improved the accuracy of the pneumatics controls, chuck flatness, tilt control of the Master and Replica plate, and also optimized the imprint sequence. The pneumatic controls influence mask flatness during the mask replication process, as shown in Figures 7a. We estimate that pressure accuracy needs to be around 10Pa for robust IP control, as shown in Figure 7b. In addition, the dynamic range at high speed needs around 50kPa.[17]



a b

Figure 7. a) Influence of mask flatness on image placement. b) Simulation showing the required pressure control.

We have been able to realize both of these conditions simultaneously with our high performance pneumatics, and the results are shown in Figure 8. The IP accuracy (after removing correctables) on the FPA-1100NR2 is 0.8nm in X, 1.0nm in Y, as shown in Figure 8a, and IP stability for 4 weeks is better than 0.3nm in X and Y, as shown in Figure 8b.[18]



a b

Figure 8. a) IP accuracy (after removing correctables). b) IP stability after 4 weeks.

The mask replication process also requires good control of the critical features. Residual layer thickness (or RLT) plays a role in CDU, since variations in RLT can impact CDU after pattern transfer. As a result, we have worked to minimize RLT variation. Currently we can achieve with an RLT uniformity of 3.3nm. From a simple geometrical estimation, the impact on CDU on a replica mask after etching is 0.6 nm, and this value meets the 0.80nm specification. A map of the residual layer thickness uniformity on a replica mask is shown in Figure 9.

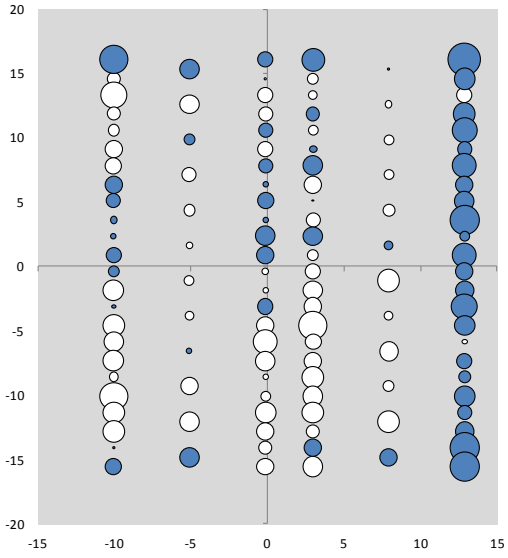


Figure 9. Residual layer variation across the 26mm x 33mm field of an imprinted replica mask. The RLT uniformity was 3.3nm, 3sigma.

4. CONCLUSIONS

Great progress has been made in the field of NIL over the last four years. In this paper, to meet CoO requirements and to address yield issues, the progress on overlay, throughput, and particle was shown. 90 wafers per hour on a four-station cluster tool was achieved by applying a multi-field dispense (MFD) method in which resist is jetted onto several fields in order to decrease the overhead resulting from a sequential dispense and imprint process flow.

Refinement of the HODC system has enabled correction of higher order terms up to K30. The system was applied for both mix and match and single machine overlay tests. A mix and match overlay of 3.4 nm has been demonstrated and SMO across the wafer was 2.5nm.

A new mask replication tool, the FPA-1100NR2 was also introduced and the means for improving the residual IP error in the tool to ~ 1 nm was presented. The combination of critical feature resolution and better IP will be used to address advanced devices with half pitch dimensions less than 15nm for the memory markets.

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