Performance of a Nanoimprint Mask Replication System

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Abstract

Nanoimprint lithography manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

In this paper, we review the progress and status of the FPA-1100NR2 mask replication system and also discuss the methods used on wafer imprint systems to extend the life of a replica mask. Criteria that are crucial to the success of a replication platform include image placement (IP) accuracy and critical dimension uniformity (CDU). Data is presented on both of these subjects. With respect to image placement, an IP accuracy (after removing correctables) of 0.8nm in X, 1.0nm in Y has been demonstrated. Particle adders were studied by cycling the tool for more than 16000 times and measuring particle adders. Additionally, new methods, including on-tool wafer inspection and in-situ mask cleaning are being studied to further extend the replica mask life.

Keywords: nanoimprint lithography, NIL, CoO, particle control, image placement accuracy, mask replication, mask life

1. Introduction

Imprint lithography is an effective and well known technique for replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-8] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both CDU and line edge roughness meet the criteria of 2nm. A collaboration partner has achieved overlay of 10nm (with a target of 8nm)[9] and defect levels ~ 5/cm^2 across a lot of 25 wafers.[10] Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether CoO requirements can be met. Recently, Ye reported on throughput methods designed to achieve 80 wafers per hour on a four-station NZC cluster tool[11].

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On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photo masks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was recently reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50 nm sensitivity.[12] Presently, Ichimura et al. have exceeded the targets for both CDU and IP. In addition, master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20 nm have been fabricated.[13]

The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. In 2012, an MR-5000 mask replication tool was developed specifically to pattern 6" x 6" x 0.25" replica masks from an e-beam written master. Previous work by Ichimura et al. using this tool, demonstrated that a CDU of less than 1.5nm 3-sigma can be achieved on both the master and replica masks.[14]

As the most aggressive features in advanced memory designs continue to shrink below 15 or 16 nm (towards 1Z nm), the cost of fabricating these devices increases because of the large number of additional deposition, etch and lithographic steps necessary when using immersion lithography.[15] NIL offers a more attractive CoO than competing technologies. Cost benefits can be realized by:

- Enabling direct printing of the features of interest, without the need for multiple patterning techniques.
- Improved mask life that allows a replica mask to be used for more than 2000 wafers.
- By improving the throughput of the NIL tool

It is important to recognize however that both the replica mask life and the mask specifications must be compatible with device manufacturing needs. With respect to CoO, it is anticipated that the lifetime of a single replica imprint mask will need to be on the order of 2x10^5 imprints, or approximately 2000 wafers. And for devices with half pitches compatible with 1Z nm memory, the replica mask must also meet strict criteria in IP in order to meet the overlay specifications of the device.

In this paper, we review the progress and status of the FPA-1100NR2 mask replication system and also discuss the methods used on wafer imprint systems to extend the life of a replica mask. Criteria that are crucial to the success of a replication platform include image placement (IP) accuracy and critical dimension uniformity (CDU). Data is presented on both of these subjects. With respect to image placement, an IP accuracy (after removing correctables) of 0.8nm in X, 1.0nm in Y has been demonstrated. Particle adders were studied by cycling the tool for more than 16000 times and measuring particle adders. Additionally, new methods, including on-tool wafer inspection and in-situ mask cleaning are being studied to further extend the replica mask life.

2. Mask Replication

In 2017, the new FPA-1100NR2 mask replication tool, which meets the target for the 1Z nm generation of devices, was shipped to a customer site. Target specifications are shown in Table 1. A schematic image of the tool is shown in Figure 2.

Target Specifications		
Throughput	4	Mask/hour
CD Uniformity (3σ) (Adder)	0.8	nm
Image PlacemenAccuracy (3σ) (Adder)	1.0	nm
Particle	0.002	pcs/Mask

Table 1. Target specifications for the NR2 mask replication tool.

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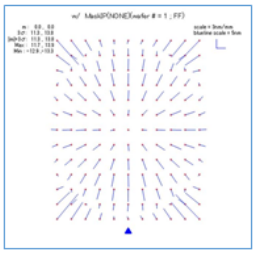
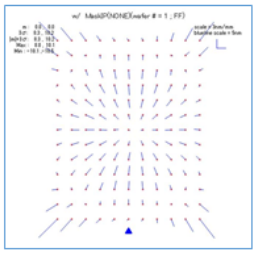
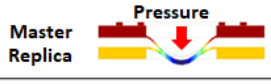
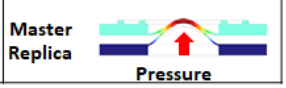
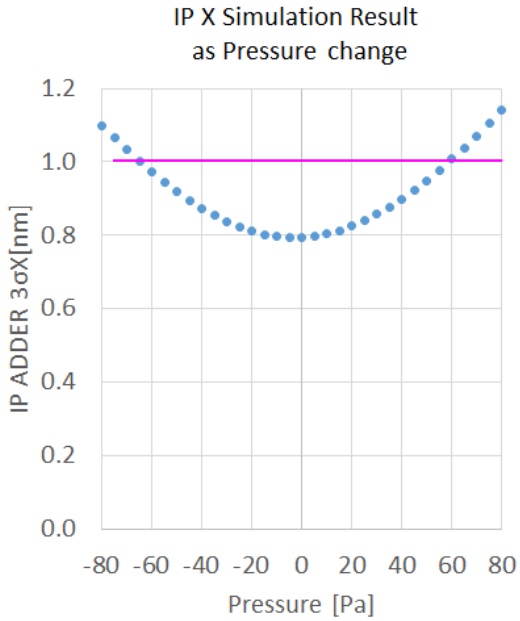
Figure 2. Schematic image of the FPA-1100NR2 replication system.

To optimize image placement accuracy, we improved the accuracy of the pneumatics controls, chuck flatness, tilt control of the Master and Replica plate, and also optimized the imprint sequence. The pneumatic controls influence mask flatness during the mask replication process, as shown in Figures 3a. We estimate that pressure accuracy needs to be around 10Pa for robust IP control, as shown in Figure 3b. In addition, the dynamic range at high speed needs around 50kPa.

Flatness of master and replica are controlled with pneumatics.

Master	+1.0[kPa]	0.0[kPa]
Replica	0.0[kPa]	+1.0[kPa]
Diff.	**-1.0[kPa]**	**+1.0[kPa]**
IP (Adder)	 3σx:11.3,y:13.8	 3σx:8.3,y:10.2
Image		

a



b

Figure 3. a) Influence of mask flatness on image placement. b) Simulation showing the required pressure control.

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We have been able to realize both of these conditions simultaneously with our high performance pneumatics, and the results are shown in Figure 4. The IP accuracy (after removing correctables) on the FPA-1100NR2 is 0.8nm in X, 1.0nm in Y, as shown in Figure 4a, and IP stability for 4 weeks is better than 0.3nm in X and Y, as shown in Figure 4b.

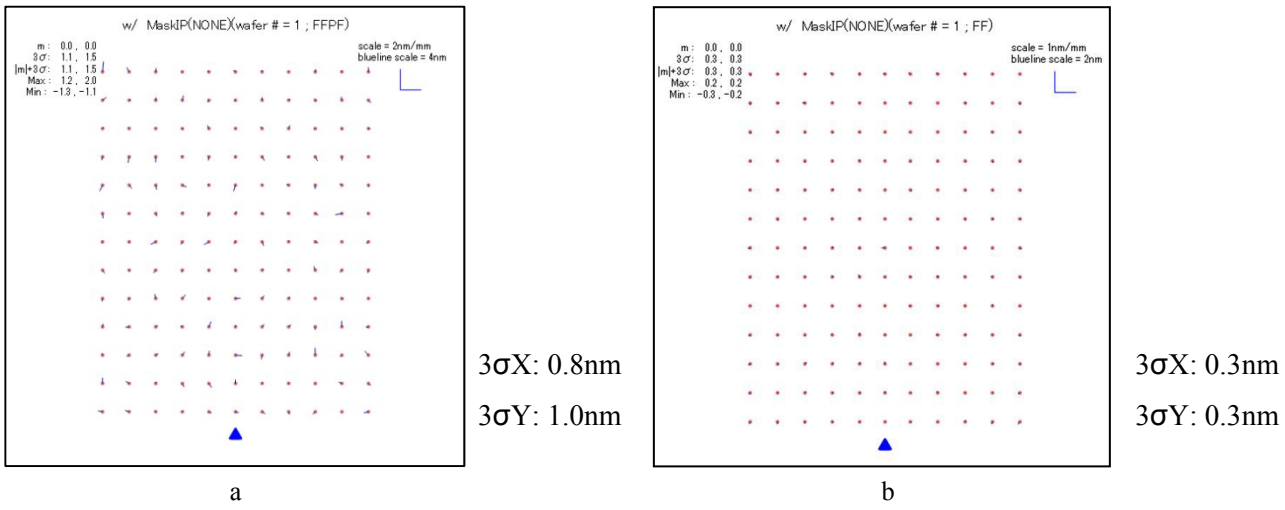

Figure 4. a) IP accuracy (after removing correctables). b) IP stability after 4 weeks.

The mask replication process also requires good control of the critical features. Residual layer thickness (or RLT) plays a role in CDU, since variations in RLT can impact CDU after pattern transfer. As a result, we have worked to minimize RLT variation. Currently we can achieve with an RLT uniformity of 3.3nm. From a simple geometrical estimation, the impact on CDU on a replica mask after etching is 0.6 nm, and this value meets the 0.80nm specification. A map of the residual layer thickness uniformity on a replica mask is shown in Figure 5.

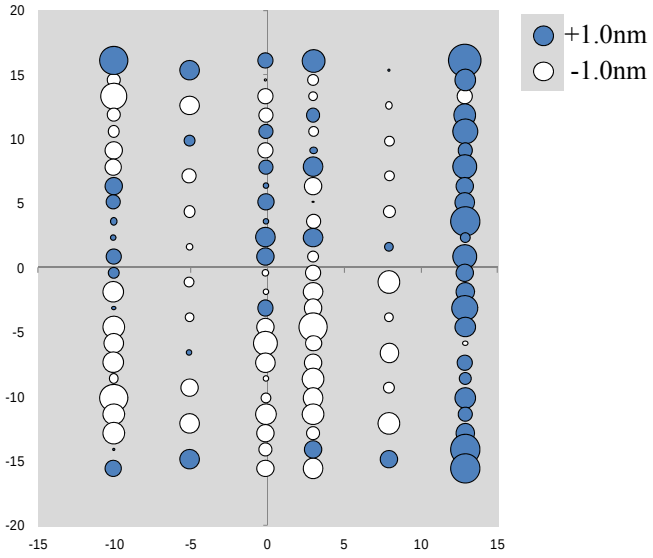

Figure 5. Residual layer variation across the 26mm x 33mm field of an imprinted replica mask. The RLT uniformity was 3.3nm, 3sigma.

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3. Mask Life and Particle Reduction

Mask life is critical in meeting cost of ownership targets for nanoimprint lithography. As mentioned previously, it is anticipated that the lifetime of a single replica imprint mask will need to be on the order of $2x10^5$ imprints, or approximately 2000 wafers.

Figure 6 reviews mask life history. Improvements were steadily made through the implementation of various particle countermeasure controls including an optimized air curtain, surface treatments of ceramics to minimize particle formation,
optimized tool cleaning methods, an electrostatic cleaning plate to draw particles away from the imprint area, and a mask neutralization system. As a result, mask life feasibility of 80 lots has been demonstrated.

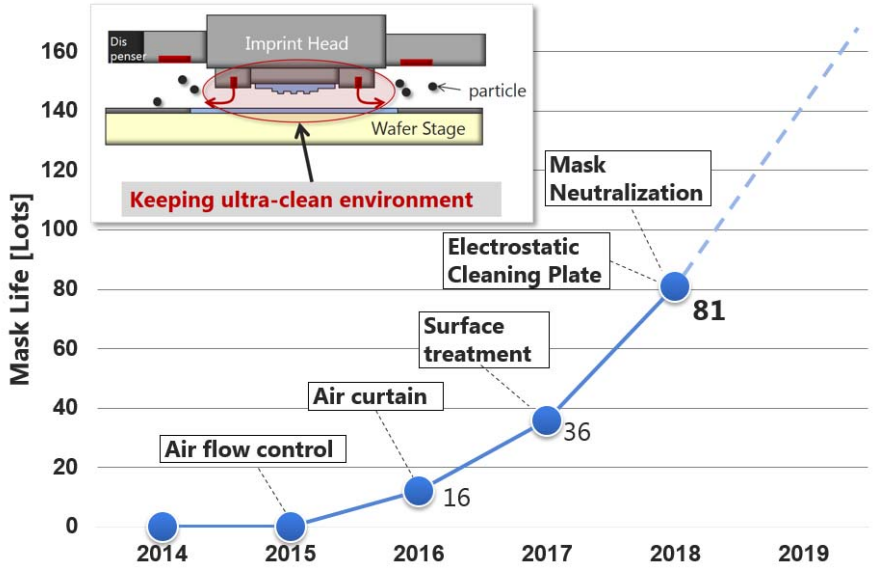

Figure 6. Mask life history since 2014.

The extended mask life is directly related to the reduction of tool particle adders, as shown in the graph of particle adder history in Figure 7. Each particle reduction method had a positive impact on particle adders. Since 2014, particle adders have been reduced from 0.1 pieces per wafer to 0.0005 pieces per wafer, which corresponds to one particle every 2000 wafers on the NZ2C tool.

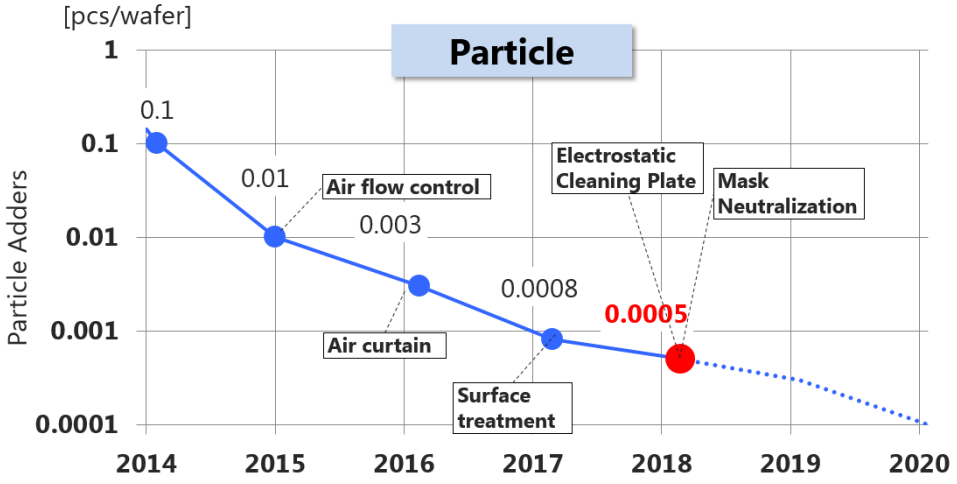

Figure 7. Particle adder history. Particles adders have been reduced to 0.0005 pieces per wafer.

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New methods are now being developed to further extend mask life beyond 100 lots (2500 wafers). New methods being developed include:

- A wafer particle checker
- An on-tool mask cleaning system
- Additional cleanliness improvements

The on-tool mask cleaning system can remove organic contamination from the mask. Testing has already started and we have confirmed that the system is capable of removing any remaining resist from the surface of the mask. Figure 8 shows the comparison of removal rate between on-tool cleaning system and offline mask cleaning machine. The process is still undergoing optimization to better understand the necessary cleaning times and frequency. The overall idea is to decrease the number of times where the mask needs to be removed from the tool for cleaning.

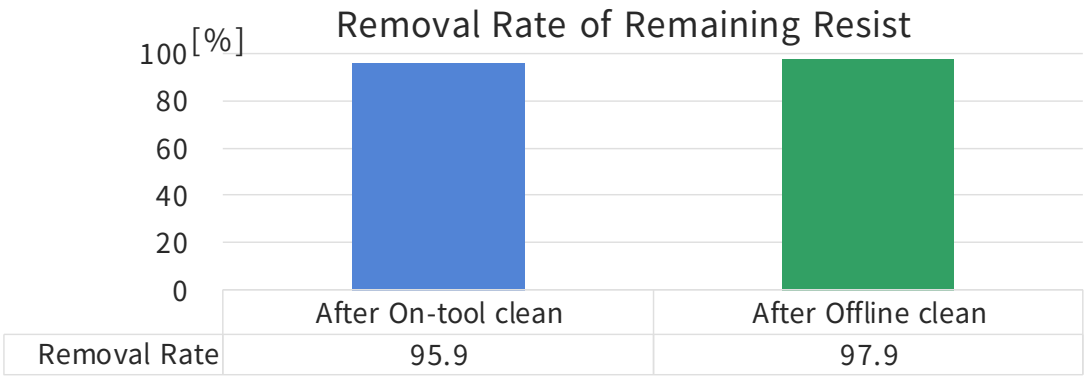

Figure 8. Comparison of removal rate between on-tool cleaning system and offline cleaning machine.

4. Conclusions

Great progress has been made in the field of NIL over the last two years. A new mask replication tool, the FPA-1100NR2 was also introduced and the means for improving the residual IP error in the tool to ~ 1 nm was presented. The combination of critical feature resolution and better IP will be used to address advanced devices with half pitch dimensions less than 15nm for the memory markets. Mask life and particle reduction were also addressed. An 80-lot mask life feasibility has been demonstrated, and new particle reduction methods were discussed, which will be used to extend mask life beyond 100 wafer lots.

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