

Improved Particle Control for High Volume Semiconductor Manufacturing for Nanoimprint Lithography

Tsuyoshi Arai, Yoichi Matsuoka, Hisanobu Azuma

Canon Inc., 20-2 Kiyohara-Kogyodanchi, Utsunomiya-shi, Tochigi 321-3292, Japan

ABSTRACT

Nanoimprint Lithography (NIL) has been shown to be an effective technique for replication of nano-scale features. The NIL process involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

There are many criteria that determine whether a particular technology is ready for high volume semiconductor manufacturing. Included on the list are overlay, throughput and defectivity.

Imprint lithography, like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL has defect mechanisms unique to the technology, and they include liquid phase defects, solid phase defects and particle related defects. Especially more troublesome are hard particles on either the mask or wafer surface. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process. If Cost of Ownership (CoO) requirements are to be met, it is critical to minimize particle formation and extend mask life.

In this work, methods including in-situ particle removal, mask neutralization and resist filtration are discussed in detail. As a result of these methods, along with already developed techniques, particle counts on a wafer were reduced to only 0.0005 pieces per wafer path or a single particle over 2000 wafers, with a next target of 0.0001 pieces per wafer path.

Particle adder reduction correlates directly with mask life, and a mask life of 81 lots (about 2000 wafers) is demonstrated. New methods are now under development to further extend mask and reduce cost of ownership. In this work on-tool wafer inspection and mask cleaning methods are also introduced.

Keywords: nanoimprint lithography, NIL, FPA-1200NZ2C, mask life, particle, defect

1. INTRODUCTION

Nanoimprint Lithography (NIL)¹⁻¹⁰, like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL does have defect mechanisms unique to the technology, and they include, liquid phase defects, solid phase defects and particle related defects.

Liquid phase defects can form, as an example, as the result of contamination to the underlying adhesion layer. The result of this contamination is incomplete filling in a small area, and is a type of non-fill defect. This defect type has been addressed in the past by applying the same sort of environmental filtering systems required, for example, for chemically amplified resists.

Solid phase defects can occur during the separation process. Shear forces imparted between the mask and wafer can tear features and potentially leave resist on the imprint mask. Another consequence of shear forces is line collapse and can be observed when the aspect ratio of sub-20nm features starts to grow well beyond 2:1. These defect types have also been overcome by careful attention to system controls during separation and are also no longer considered a priority.

More troublesome are particles that reside and adhere to either the mask or wafer surface. In the past we have described how the inkjet system can add to particle count and how liquid in-line filtrations systems addressed this issue.¹¹

These particles types were typically soft in nature and could be addressed by mask cleaning. Hard particles generated within the imprint tool are the biggest source of concern. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process. In summary,

- Liquid phase defects do not cause mask damage, do not require mask cleaning and can be addressed through environmental controls.
- Solid phase defects also do not damage the mask, but may require mask cleaning.
- Particles, break down into two categories: soft and hard. Soft defects rarely damage the mask. Hard particles, however impact mask life.

To put this point in perspective, consider that in order to meet the CoO specs, the replica mask life must be sustained for better than 1000 wafers. If we conservatively assume that:

- Every hard particle adds a defect to the mask, and
- The mask defectivity limit from hard particles is 0.1 pieces per square centimeter,

then the number of particle adders per wafer pass must be < 0.001 . As a result, if we are to achieve this particle specification, an aggressive strategy is needed to remove particles adders to the wafer and mask. The purpose of this paper is to review the measures being taken to reduce and control particles within the imprint tool and understand their impact to both particle adders and to mask life. Finally, we discuss additional methods that can further extend mask life and reduce NIL cost of ownership.

2. STRATEGY FOR PARTICLE MITIGATION

There are several countermeasures for particles that can be taken. In the past, countermeasures that have been discussed in detail include:¹²

1. Surface treatment: The minimization of particle generation from particle sources related to materials within the tool and the surface treatment of these materials.
2. Air curtain system: The reduction of particles that could potentially find their way onto the mask and wafer. These can be addressed by optimizing the airflow within the tool.
3. Optimize cleaning and polishing: Reduction of particles by using optimized cleaning and polishing of key parts.

In this paper we examine:

- In-situ particle removal
- Mask neutralization
- Resist filtration methods

By applying these techniques to a nanoimprint lithography system, as shown in Figure 1, it is possible to create an ultra-clean environment that is suitable for the nanoimprint process.

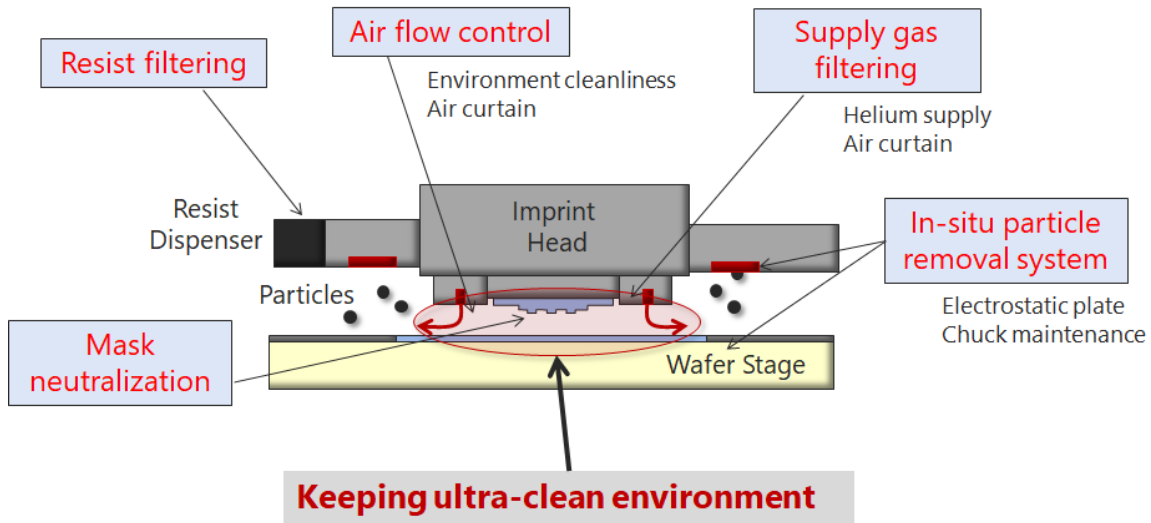


Figure 1. Canon's strategy for particle mitigation

a. In situ particle removal

Electrostatic charge can be generated on the surface of the imprint mask as a result of the separation of the mask and wafer after the exposure of the imprint resist. Charge can be addressed in two ways. One method is to create a charged environment away from the mask in order to preferentially attract charged particles to the charged environment. An Electrostatic Cleaning Plate (ESCP) has been designed which is placed adjacent to the mask and operated at a voltage greater than the voltage generated on the imprint mask. The ESCP system was initially tested on an off-tool set up as shown in Figure 2a. In the configuration shown, two tests were run. In the first test (Figure 2b), particles were collected on a 100mm wafer over a five minute time period, and measured using a KLA-Tencor SFS6420 Surface Inspection System, with a detection limit of 120nm. Three particles were collected. In the second test (Figure 2c), the plate was set to 1kV. In this case, 25 adders were detected, confirming the efficacy of the ESCP.

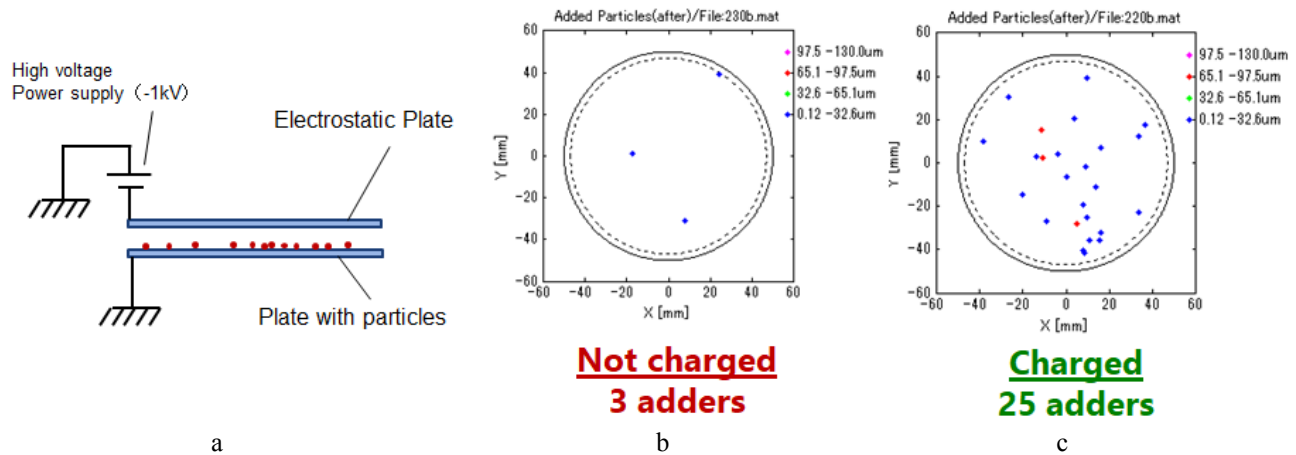


Figure 2. a. ESCP off-line test b. Particle adder test with no applied voltage c. Particle adder test with 1kV applied voltage

As a follow up experiment, the ESCP was applied to an NZ2C nanoimprint tool, and found to be effective in attracting weakly attached particles on the wafer stage.

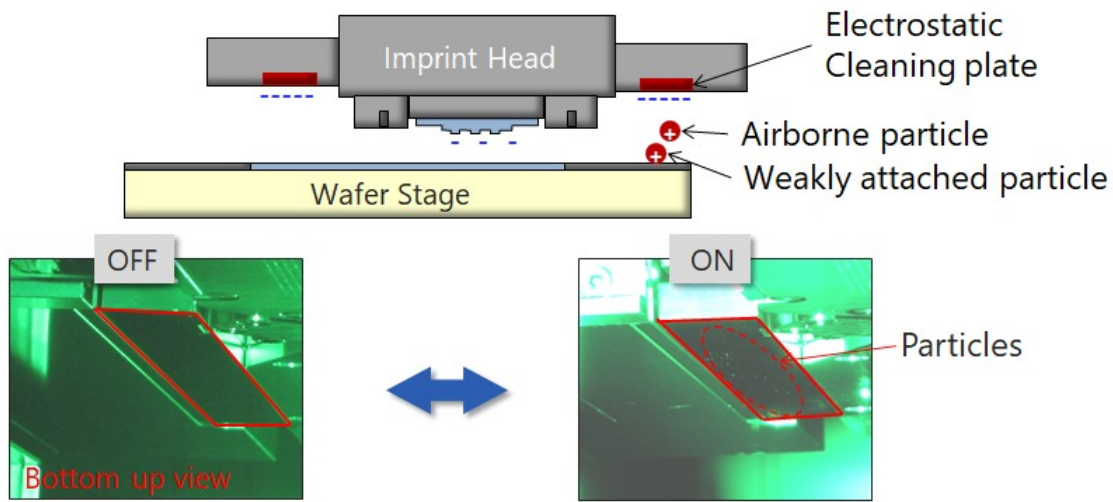


Figure 3. An ESCP was applied to an NZ2C nanoimprint tool and was effective in capturing weakly bound particles after applying a voltage to the plate.

b. Mask neutralization

A second method used to minimize particles on the mask surface works by the application of neutralization schemes. The mask and wafer separation step induces charging of the mask surface. We can take advantage of Paschen's law by introducing helium gas between the mask and wafer as illustrated in Figure 4. Neutralization tests were performed and were able to reduce the electrostatic voltage by more than a factor of four, as shown in the graph at the bottom of the figure.

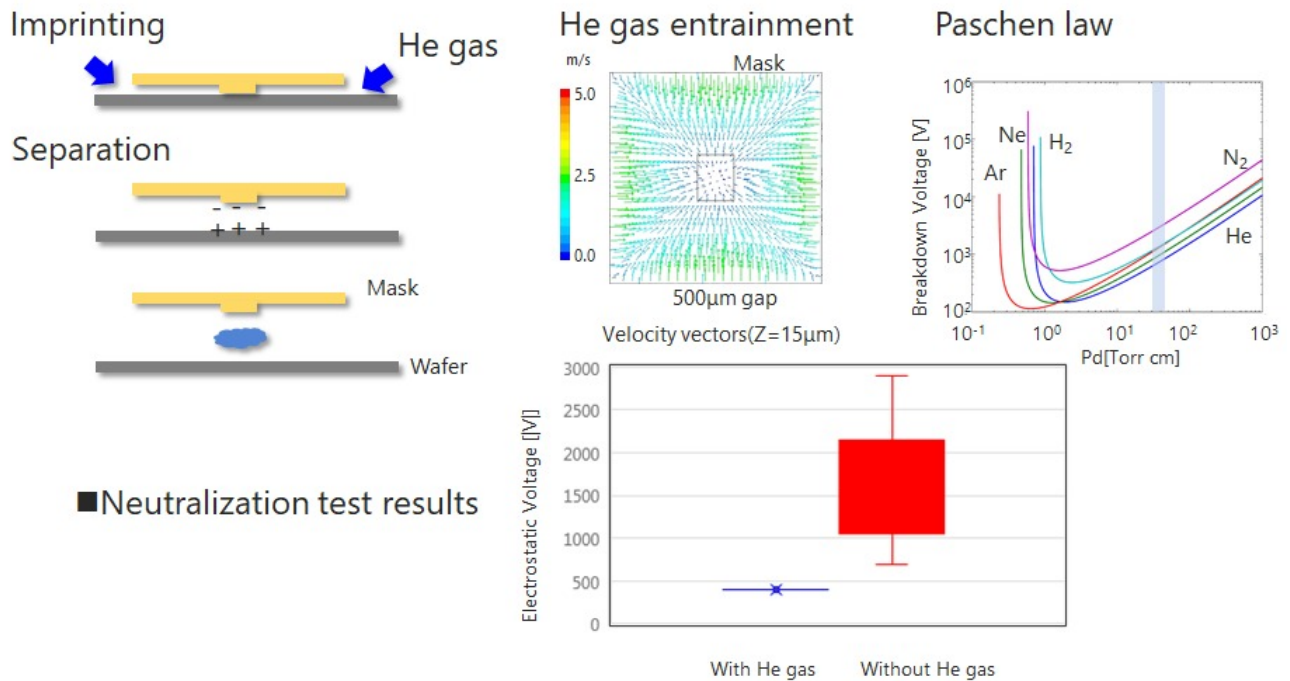


Figure 4. Mask charge can be neutralized through the introduction of helium gas. Testing confirmed that the electrostatic voltage could be reduced by 4x.

c. Resist filtration

Previous resist filtration discussions described the use of an off-line recirculation system to reduce particles within the system to 0.009 pcs/mL. In this study particle counts were taken on the tool with the accompanying resist jetting dispenser. The resist was kept in an ultra-clean state by adding additional in-line filtration and using smooth-flowing piping with reduced surface roughness.

Tests were then run with the system in idle mode and during the resist jetting process as shown in Figure 5. Particle counts were maintained at approximately 0.001 pcs/mL under both conditions, measured at a detection sensitivity of 300nm.

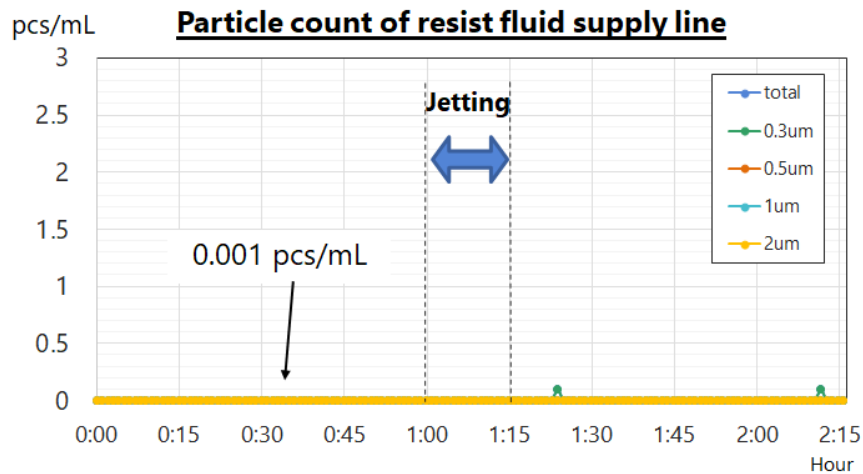


Figure 5. Particle count data verifying that particle counts are kept low when the resist filtration system is in idle mode and when it is dispensing.

3. MASK LIFE STATUS

Particle reduction results are shown in Figure 6, which plots particle adds as a function of year. Over the last year, the inclusion of the ESCP, in addition to improvements in surface treatments and supply gas filtering has reduced particle adds to 0.0005 pcs/wafer, or 1 particle every 2000 wafers.

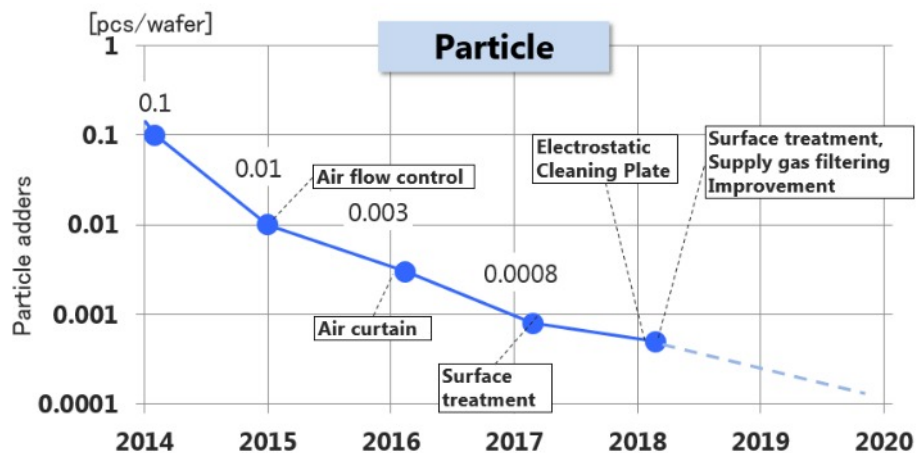


Figure 6. Progress and roadmap for particle reduction in the imprint tool

The correlation between particle adder reduction and mask life is apparent, as shown in Figure 7, which plots mask life as a function of year. Using the various methods described in this paper, a mask life of 81 lots (>2000 wafers) has been demonstrated.

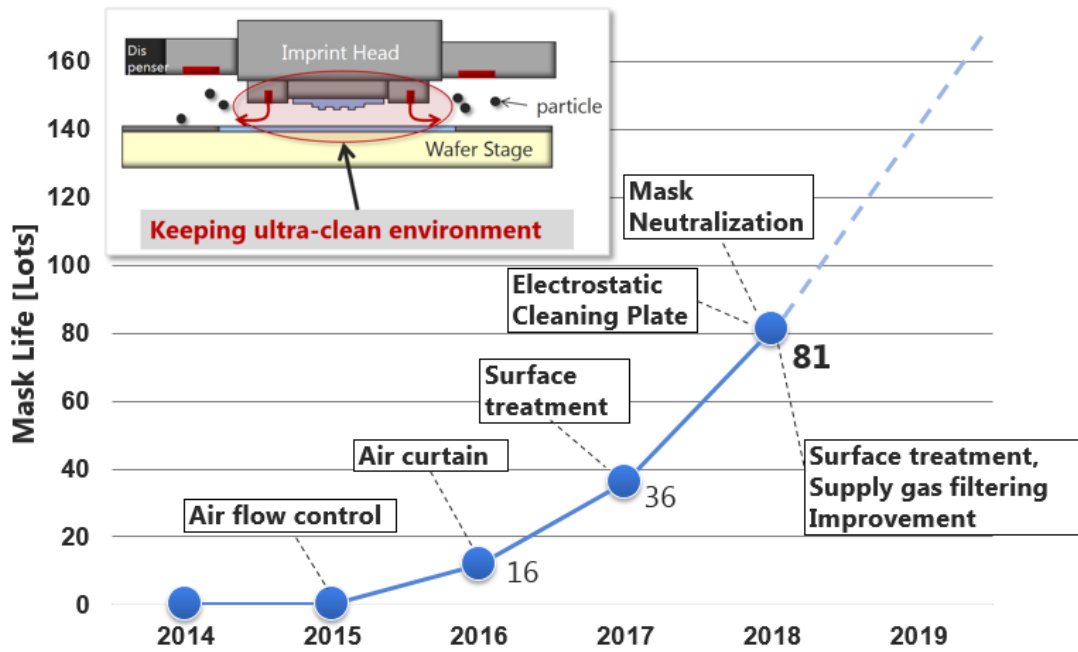


Figure 7. Mask life as a function of year. By applying a variety of particle reduction methods, a mask life of 81 lots has been demonstrated.

4. SOLUTIONS FOR MASK LIFE EXTENSION

Extended mask life reduces cost of ownership. Therefore additional methods are being investigated as means of extending mask life beyond 100 lots. Figure 8 depicts a simple schematic of an imprint tool equipped with both a wafer particle checker (WPC) and an on-tool mask cleaning unit.

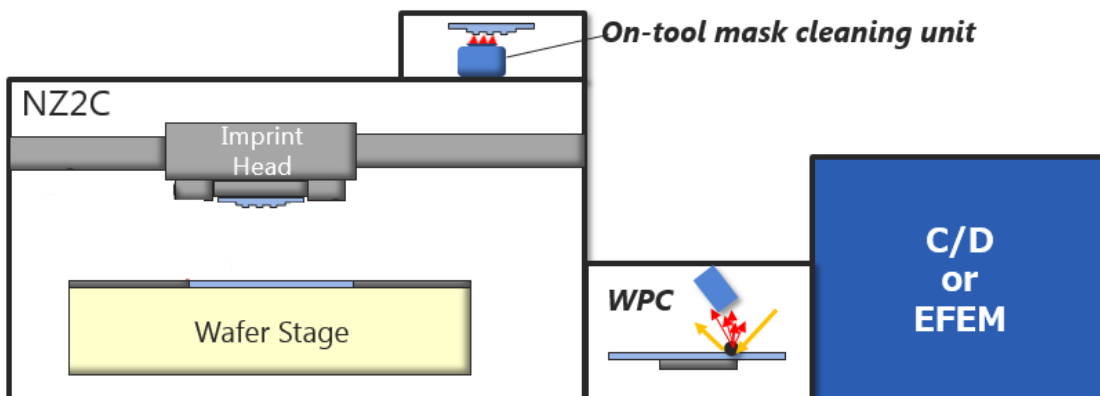


Figure 8. Schematic of an imprint tool equipped with both a wafer particle checker and an on-tool mask cleaning unit.

Development has already started on the WPC as a means for screening wafers before they enter a nanoimprint station. The system is a compact scattered light detection system with nominal resolution of about 100nm on bare wafers and 300nm on patterned wafers.

An on-tool mask cleaning is also being developed. The system uses dry clean technology and scans the mask surface, removing any residual resist on the mask, thereby eliminating a mechanism for potential mask damage. Initial studies confirm that the system's ability to remove resist is comparable to off-line tools currently used (Figure 9).

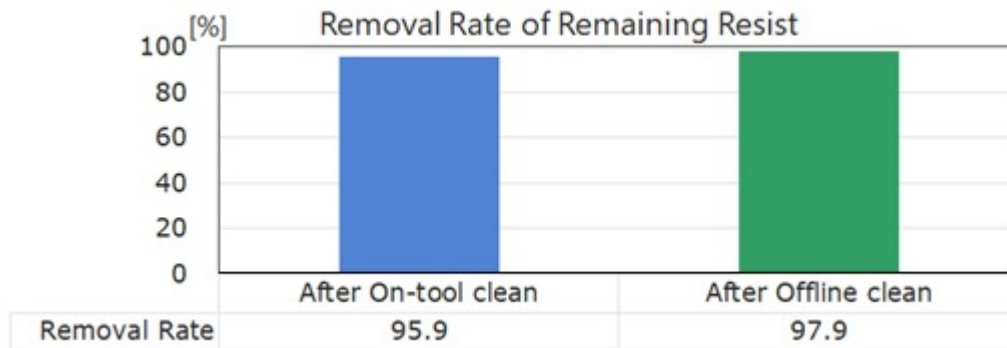


Figure 9. Resist removal rate for both online and offline resist removal systems.

CONCLUSIONS

Great progress has been made in the field of nanoimprint lithography over the last two years. A key factor for the insertion of nanoimprint lithography in a high volume manufacturing facility is mask life, which is influenced, in part, by the cleanliness of the nanoimprint tool. The continued reduction of particle adders extends both the life of the master mask and the replica mask. In this work, methods including in-situ particle removal, mask neutralization and resist filtration were discussed in detail. As a result of these methods, along with already developed techniques, particle counts on a wafer were reduced to only 0.0005 pieces per wafer path or a single particle over 2000 wafers, with a next target of 0.0001 pieces per wafer path.

Particle adder reduction correlates directly with mask life, and a mask life of 81 lots (about 2000 wafers) was demonstrated. New methods are now under development to further extend mask and reduce cost of ownership. In this work on-tool wafer inspection and mask cleaning methods were introduced.

ACKNOWLEDGEMENTS

The authors would like to thank their colleagues in the support of this work.

REFERENCES

- [1] S. Y. Chou, P. R. Kraus, P. J. Renstrom, "Nanoimprint Lithography", *J. Vac. Sci. Tech. B* 1996, 14(6), 4129 -4133.
- [2] T. K. Widden, D. K. Ferry, M. N. Kozicki, E. Kim, A. Kumar, J. Wilbur, G. M. Whitesides, *Nanotechnology*, 1996, 7, 447 - 451.
- [3] M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S. V. Sreenivasan, J. Ekerdt, and C. G. Willson, *Proc. SPIE, Emerging Lithographic Technologies III*, 379 (1999).
- [4] M. Colburn, T. Bailey, B. J. Choi, J. G. Ekerdt, S. V. Sreenivasan, *Solid State Technology*, 67, June 2001.
- [5] T. C. Bailey, D. J. Resnick, D. Mancini, K. J. Nordquist, W. J. Dauksher, E. Ainley, A. Talin, K. Gehoski, J. H. Baker, B. J. Choi, S. Johnson, M. Colburn, S. V. Sreenivasan, J. G. Ekerdt, and C. G. Willson, *Microelectronic Engineering* 61-62 (2002) 461-467.

- [6] S.V. Sreenivasan, P. Schumaker, B. Mokaber-Nezhad, J. Choi, J. Perez, V. Truskett, F. Xu, X. Lu, presented at the SPIE Advanced Lithography Symposium, Conference 7271, 2009.
- [7] K. Selenidis, J. Maltabes, I. McMackin, J. Perez, W. Martin, D. J. Resnick, S.V. Sreenivasan, Proc. SPIE Vol. 6730, 67300F-1, 2007.
- [8] I. McMackin, J. Choi, P. Schumaker, V. Nguyen, F. Xu, E. Thompson, D. Babbs, S. V. Sreenivasan, M. Watts, and N. Schumaker, Proc. SPIE **5374**, 222 (2004).
- [9] Hiroaki Takeishi, S.V. Sreenivasan, Proc. SPIE 9423, Alternative Lithographic Technologies VII, 94230C (March 19, 2015).
- [11] Keiji Emoto, et al, Proc. SPIE 9777, Alternative Lithographic Technologies VIII, 97770C (March 22, 2016).
- [11] Z. Ye, K. Luo, J. W. Irving, X. Lu, Wei Zhang, B. Fletcher, W. Liu, F. Xu, D. LaBrake, D. Resnick, S.V. Sreenivasan, Proc. SPIE. 8680, Alternative Lithographic Technologies V, 86800C. (March 26, 2013).
- [12] M. Yonekawa et al., Proc. SPIE. 10454, Photomask Japan 2017: XXIV Symposium on Photomask and Next-Generation Lithography Mask Technology.