Invited Paper

Nanoimprint Lithography and a Perspective on Cost of Ownership

Douglas J. Resnick[1], Junji Iwasa[2]

[1]Canon Nanotechnologies Inc., 1807 West Braker Lane, Bldg. C-300 Austin, TX 78758 USA
[2]Canon Inc., 20-2, Kiyohara-Kogyodanchi, Utsunomiya-shi, Tochigi 321-3292 Japan

ABSTRACT

Over the last several decades, several innovative lithographic approaches have been introduced in an effort to extend device roadmaps for both memory and logic devices. For many years, the emphasis was almost strictly on resolution, with the thought that at some point, conventional reduction optical lithography would be wavelength restricted.

The thought process changed around ten years ago however, with the introduction of pitch splitting techniques such as self-aligned patterning and multiple uses of litho/etch (LE) processes. For dense lines, Self-Aligned Double Patterning (SADP) methods extended resolution to about 20nm (half pitch) and was followed by quad patterning processes (SAQP) that could reduce the half pitch to 10nm. Multiple litho/etch processes have already been applied create 20nm half pitch dense contact arrays.

Although these pattern multiplication processes have enabled the industry to continue to aggressively scale devices, the methods come with a cost; both technical and financial. The technical price we pay for pitch splitting comes in the way of critical dimension control and additional overlay terms (pitch walking). Despite the precision of our newest deposition and etch processes, the additional process steps used to reduce pitch introduce these types of errors. Any technology (NIL and EUVL for example) that can deliver a single litho step process has the opportunity to deliver a simplified solution with better CD and overlay control.

In this work, we review the key elements that go into determining NIL CoO and compare it to existing technology. Two examples are described in detail; sub-19nm half pitch lines and dense 20nm contact arrays. The assumptions used in the model are described, and projections for further reducing CoO are discussed, based on tool throughput, mask life and other key factors.

Keywords: Nanoimprint Lithography, NIL, cost of ownership, CoO, SADP, SAQP, throughput, mask life

1. INTRODUCTION

Over the last several decades, several innovative lithographic approaches have been introduced in an effort to extend device roadmaps for both memory and logic devices. For many years, the emphasis was almost strictly on resolution, with the thought that at some point, conventional reduction optical lithography would be wavelength restricted.

The thought process changed around ten years ago however, with the introduction of pitch splitting techniques such as self-aligned patterning and multiple uses of litho/etch (LE) processes. For dense lines, Self-Aligned Double Patterning (SADP) methods extended resolution to about 20nm (half pitch) and was followed by quad patterning processes (SAQP) that could reduce the half pitch to 10nm. Multiple litho/etch processes have already been applied create 20nm half pitch dense contact arrays.

Although these pattern multiplication processes have enabled the industry to continue to aggressively scale devices, the methods come with a cost; both technical and financial. The technical price we pay for pitch splitting comes in the way of critical dimension control and additional overlay terms (pitch walking). Despite the precision of our newest deposition and etch processes, the additional process steps used to reduce pitch introduce these types of errors. Any

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technology (NIL and EUVL for example) that can deliver a single litho step process has the opportunity to deliver a simplified solution with better CD and overlay control.

Nanoimprint lithography (NIL) manufacturing equipment for the semiconductor industry utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[1-11] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity. Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask.

NIL's impact on cost of ownership (CoO) must be understood relative to the particular device level to be printed, along with an understanding of the current technology that is being used (LELE, SADP, SAQP (and with how many cut levels)) so that you can correctly compare NIL technology to the existing solution or future solutions.

In this work, we review the key elements that go into determining NIL CoO and compare it to existing technology. Two examples are described in detail; dense sub-19nm half pitch lines and dense 20nm contact arrays. The assumptions used in the model are described, and projections for further reducing CoO are discussed based on tool throughput, mask life and other key factors.

2. COST OF OWNERSHIP CONTRIBUTORS AND ASSUMPTIONS

a. Cost of Ownership Contributors

Contributors to cost of ownership (CoO) can be broken down into three groups: tool CoO, mask CoO, and peripheral process CoO, as shown in Table 1. Tool CoO includes tool fixed cost, running costs, the illumination source cost and the cost associated with resists (imprint resist for example). Mask CoO includes master mask price, replica mask price (which can be broken into two components: mask price and mask life) and mask cleaning cost (specifically the cost of cleaning the replica mask). Finally, the additional process steps must be taken into account. Possible contributors include deposition steps, track processes, wet and dry etching, wet cleans, and costs associated with other required lithography steps. As an example, for a NAND Flash gate level, a single optical litho step is required following a spacer based process used to decrease pitch by a factor of two.

Tool Cost of Ownership	Mask Cost of Ownership	Process Cost of Ownership
Tool fixed cost	Master mask price	Other process costs (dep, etch, etc.)
Running cost	Replica mask price	Additional litho cost (cut levels)
Illumination cost	Mask life	
Imprint chemical cost	Replica clean cost	

Table 1. CoO can be broken into tool CoO, mask CoO and costs associated with other process steps, including deposition, etch and additional lithography steps.

b. Cost of Ownership Assumptions

i. NIL Tool Cost Assumptions

Tool fixed cost was calculated using the equation:

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$$\text{Tool CoO} = (\text{Tool Price} + \text{Track Price})/(\text{Throughput}*24*365*(\text{Uptime})*\text{Depreciation Time}),$$

where,

Throughput: 80 (baseline condition), 96 and 200 wafers per hour
Uptime: 90%
Depreciation schedule: 5 years

Although throughputs as high as 90 wafers per hour (wph) have already been demonstrated, the baseline throughput for the model was set at 80 wph.[12] Running costs, which include labor, utilities and maintenance, are on the order of $4.00 per wafer level. Because i-line illumination is used to expose the nanoimprint resist, illumination costs are much lower than 193 immersion tools or EUVL tools, and are typically less than $1.00 per wafer. Imprint chemical costs include both an adhesion layer and the imprint resist, and add about $3.00 to the cost of ownership.

ii. NIL Mask Cost Assumptions

Mask contributors include the master mask, replica masks and replica clean costs. A master mask price of $400K was assumed for the model. It is a small contributor to CoO, since the master was assumed to have a lifetime of 1000 replica masks. As a result, the additional CoO is well under $1.00

The replica mask cost has two main inputs: mask price and mask lifetime. Assumptions for both mask price and mask lifetime are:

Replica mask price: $35K (baseline) and $25K
Replica mask lifetime: 80 lots (baseline), 120 lots

The replica mask price is low compared to a photomask because the masks are replicated using a NIL replication system, with throughputs significantly higher than conventional electron beam writers. With respect to mask lifetime, 80 lots and 120 lots were recently demonstrated.[13,14] Therefore a baseline condition of 80 lots (meaning 2000 wafers) was assumed.

In order to keep the replica mask as defect free as possible, we assumed that the replica mask would undergo a clean process after each wafer lot. This ends up adding less than $1.50 to the overall CoO. If fewer cleans are required, the clean CoO will drop accordingly.

iii. Process cost assumptions

To complete a wafer level, there are a variety a required process steps involved, including metal deposition, chemical vapor deposition, atomic layer deposition, track processes, directional dry etches and strip processes. The associated cost per wafer level was calculated using the equation:

$$\text{Tool CoO} = (\text{Tool Cost})/(\text{Throughput}*24*365*\text{Uptime}*\text{Depreciation Time}).$$

Again, uptime was set at 90%, and a five year depreciation cycle was assumed. As an example, a $6M dry etch tool running at 80 wph would add $1.90 to the overall cost of ownership.

As previously mentioned, some processes may require further lithographic steps, and in this model, and cut layers were assumed to be done with a KrF tool, with an associated CoO of $4.73.

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3. COST OF OWNERSHIP RESULTS

CoO should be modelled for a particular device level (or levels), since the process flow can vary significantly from level to level. In this work, two device levels were modeled:

- Sub-19nm half pitch lines
- Dense 20nm contacts

a. Sub-19nm half pitch lines

It was assumed that for a direct NIL process, all that was required was deposition, NIL, etching and stripping. The total number steps involved was eight. For the dense sub-19nm half pitch lines, NIL results were compared to a conventional ArF immersion process flow. Throughput for the ArF immersion tool was assumed to be 275 wph. A total of twenty-five steps are required to complete an SAQP based process, with the assumption that only one KrF cut step is required (for a NAND gate level, for example) The modeling results are shown in Figure 1.

Sub-19nm HP Line Cost Per Wafer Level

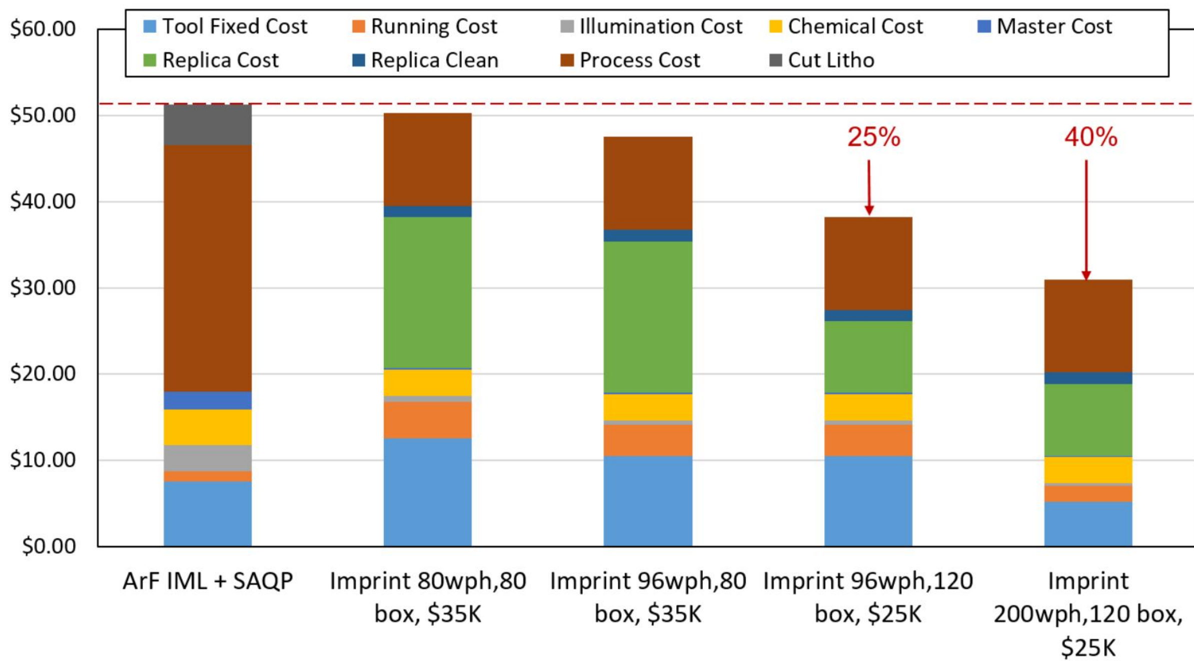

Figure 1. Cost per wafer level for a 19nm dense line process. NIL CoO is compared to an ArF immersion SAQP process, requiring a single KrF cut step. Even under the assumed baseline conditions, NIL has a cost advantage.

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The biggest contributor to the ArF immersion CoO are the additional processing steps. Using the NIL baseline conditions previously described, the cost per wafer level is lower than the ArF immersion case by about $2 per wafer level. If NIL throughput is increased to 96 wph, the NIL cost advantage is about $5.

It is worth noting that the biggest contributor to NIL CoO is mask cost. If mask life is improved to 120 lots and the mask price decreases to $25K, the total mask cost contribution drops by about half, and a 25% advantage is now realized with NIL. Finally, if a multifield imprint process is applied as a means to boost throughput to 200 wph, the NIL flow now is reduced to 40% over the ArF immersion case.

b. Dense 20nm contacts

The printing of dense 20nm contacts (needed for a DRAM device for example) using ArF immersion (ArFi) can be realized either by a LE^4 process flow or by applying a 2x SADP process flow. In this paper the 2x SADP process was modeled, again assuming the need for just a single cut step. Contacts are formed imaging dense lines in both the x and y directions and applying SADP technology to reduce the half lines from 40nm to 20nm. Because the flow requires two ArFi steps along with multiple deposition and etch steps, the cost per wafer level is higher than the sub-19 nm dense line case. For NIL, the process flow remains essentially the same. Results for the model are shown in Figure 2.

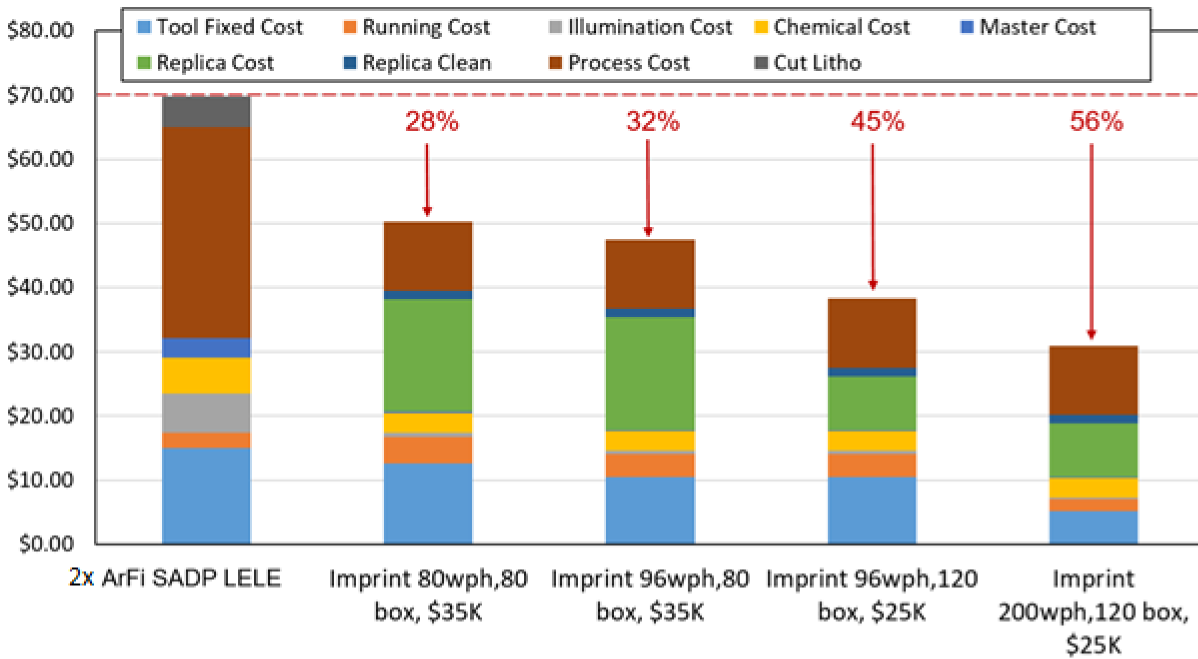

Figure 2. Cost per wafer level comparison for dense 20nm contacts. Even under baseline conditions, NIL has a 28% cost advantage over the ArFi process.

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For dense 20nm contacts, the biggest contributor to the ArF immersion CoO are the additional processing steps, followed by the ArFi steps. Using the NIL baseline conditions previously described, the cost per wafer level is lower than the ArF immersion case by about 28 percent. If NIL throughput is increased to 96 wph, the NIL cost advantage is now 32 percent.

Mask cost of ownership still has a big influence on NIL CoO, and as mask price and mask life improve, the cost advantage increases up to 45 percent. Finally, if a multifield imprint process is applied as a means to boost throughput to 200 wph, the NIL flow now is reduced by 56% over the ArF immersion case.

3. CONCLUSIONS

Great progress has been made in the field of NIL over the last four years. Throughput of up to 90 wph has been demonstrated. A mask life of 80 lots has also been realized. In this paper, NIL cost of ownership was compared to an ArF immersion process flow for two different cases: sub-19nm half pitch lines and dense 20nm contacts. For the dense line case, a simple NIL process flow provides a small reduction in CoO, which grows to as much as 40 percent as mask price, mask lifetime and tool throughput improve. For the dense contact case, NIL has an immediate advantage of 28% over the ArFi counterpart. The cost reduction doubles to 56 percent as NIL productivity, mask price and mask lifetime improve.

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