High Throughput Nanoimprint Lithography for Semiconductor Memory Applications

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Abstract

Imprint lithography is a promising technology for replication of nano-scale features. For semiconductor device applications, Canon deposits a low viscosity resist on a field by field basis using jetting technology. A patterned mask is lowered into the resist fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

There are two critical components to meeting throughput requirements for imprint lithography. Using a similar approach to what is already done for many deposition and etch processes, imprint stations can be clustered to enhance throughput. The FPA-1200NZ2C is a four station cluster system designed for high volume manufacturing.

For a single station, throughput includes overhead, resist dispense, resist fill time (or spread time), exposure and separation. Resist exposure time and mask/wafer separation are well understood processing steps with typical durations on the order of 0.10 to 0.20 seconds. To achieve a total process throughput of 17 wafers per hour (wph) for a single station, it is necessary to complete the fluid fill step in 1.2 seconds. For a throughput of 20 wph, fill time must be reduced to only one 1.1 seconds.

There are several parameters that can impact resist filling. Key parameters include resist drop volume (smaller is better), system controls (which address drop spreading after jetting), Design for Imprint or DFI (to accelerate drop spreading) and material engineering (to promote wetting between the resist and underlying adhesion layer). In addition, it is mandatory to maintain fast filling, even for edge field imprinting. In this paper, we address the improvements made in all of these parameters to first enable a 1.20 second filling process for a device like pattern and have demonstrated this capability for both full fields and edge fields. Non-fill defectivity is well under 1.0 defects/cm^2 for both field types. Next, by further reducing drop volume and optimizing drop patterns, a fill time of 1.1 seconds was demonstrated.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

Keywords: imprint lithography, nanoimprint lithography, NIL, throughput, defectivity, non-fill defects

1. Introduction

Imprint lithography is a promising technology for replication of nano-scale features.[1,2] For semiconductor device applications, Canon deposits a low viscosity resist on a field by field basis using jetting technology. A patterned mask is lowered into the resist fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.[3-8]

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was recently reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50 nm sensitivity.[9] Recently, Dai Nippon Printing (DNP) has exceeded the targets for

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both CDU and IP. DNP has fabricated master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20 nm.[10]

On the wafer side, an imprint tool must be capable of addressing defects and meeting device overlay specifications in order to provide high yielding results. With respect to cost of ownership, the technology must also provide sufficient throughput relative to both the cost of the tool and the floor space occupied by the tool.

There are two critical components to meeting throughput requirements for imprint lithography. Using a similar approach to what is already done for many deposition and etch processes, imprint stations can be clustered to enhance throughput. The FPA-1200NZ2C is a four station cluster system designed for high volume manufacturing.

For a single station, throughput includes overhead, resist dispense, resist fill time (or spread time), exposure and separation. Resist exposure time and mask/wafer separation are well understood processing steps with typical durations on the order of 0.10 to 0.20 seconds.[12] Previously, a single station throughput of 15 wafers per hour (wph) was demonstrated.[13] To achieve a total process throughput of 17 wph for a single station, it is necessary to complete the fluid fill step in 1.2 seconds. For a throughput of 20 wph, fill time must be reduced to only one 1.1 seconds.

There are several parameters that can impact resist filling. Key parameters include:

- Resist drop volume (smaller is better)
- Material engineering (to promote wetting between the resist and underlying adhesion layer)
- Design for Imprint or DFI (to accelerate drop spreading and address different pattern types)
- System controls which address drop spreading after jetting for both full fields and partial fields.
- Drop pattern optimization

In this paper, we address the improvements made in all of these parameters to first enable a 1.20 second filling process for a device like pattern and have demonstrated this capability for both full fields and edge fields. Non-fill defectivity is well under 1.0 defects/cm^2 for both field types. Next, by further reducing drop volume and optimizing drop patterns, a fill time of 1.1 seconds was demonstrated.

2. Experimental Details

To generate the inspection test masks, patterns were exposed using a shaped beam pattern generator and positive tone e-beam resist. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process were employed to create a master imprint mask for the imprint tool.

Several pattern types were evaluated. Included were line/space arrays down to 30nm, logic type patterns and dummy fill patterns. Several of the masks also included peripheral structures such as align marks and metrology marks.

Imprinting with the replica mask was performed on a single station imprint tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 300 mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process have previously been reported.[14]

Resist filling was visually observed with a large field of view camera that is capable of imaging the entire 26mm x 33mm field. Defectivity was measured with KLA−Tencor 2800 and 2905 wafer inspection tools. Inspections were performed in array mode for the line space patterns and in random mode for other patterns.

3. Throughput Results

Throughput measurements for an imprint process is always evaluated relative to areas of the pattern that do not get filled with resist and are typically referred to as non-fill defects. As a baseline, resist is allowed to fill over many seconds, and non-fill defects for a particular experiment are compared to this baseline. In the two following sections, we review the results of experiments targeting fill times and 1.2 and 1.1 seconds, respectively.

a. 1.2 Second Fill Time – 68 wph

Device levels often consist of unique regions, each having its own particular set of features. As an example, a memory level may have dense feature regions, peripheral circuitry regions, and kerf regions that may include larger features such as align and metrology marks. Table 1 shows the breakdown for the test mask used for this study.

Each region of the layer has its own specific filling characteristics. The second column describes the filling times achieved for the 1.5 second/60wph process demonstrated at the end of 2015. For this work (final column), fill times of 1.0 second were targeted in all regions with the exception of the kerf regions containing various metrology marks.

Filling Area	Fill Time (end of 2015)	Fill Time Targets (mid 2016)
FF: Core area 30nm L/S	1.2 sec	≤ 1.0sec
FF: Peripheral circuitry	1.5 sec	≤ 1.0sec
PF: Core area 30nm L/S	1.5 sec	≤ 1.0sec
FF & PF: Marks in Kerf	1.5 sec	≤ 1.2sec
Tput (wph)	**60***	**68***

FF: Full Field
PF: Partial Field

Inspection is based on KT2800 and KT2905
- Random mode inspection for full imprint field
- Array mode inspection for L/S.

* Based on a 4-station NZ2C imprint tool.

Figure 1. Test mask layout and targeted fill times for both a 60 wph and 68 wph process.

It is interesting to note that the longest fill times are often located in the kerf regions. Since resist typically fills from the center of a field out towards the edge, edge features are usually the last features to fill. In addition, larger features, such as metrology marks located in the kerf are the most difficult to fill. For the other regions, it was sufficient to achieve the faster filling times by applying new resist systems designed to promote faster resist spreading and to fine tune system controls.

For the kerf area, however, some marks needed to be redesigned (without impacting their functionality). This redesign represents one implementation of DFI. Quite often this meant segmenting the larger features as shown in Figure 2 below.

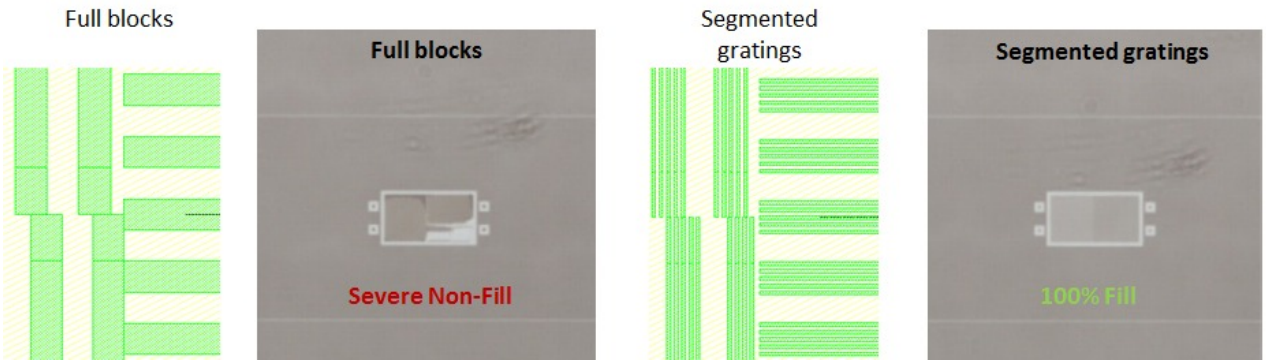

Figure 2. An example of DFI, in which large features are broken into segments to promote faster resist filling.

After performing the necessary optimization, a 25-wafer run was done at a filling time of 1.2sec on the FPA1200-NZ2C using a test mask with a minimum half pitch of 30nm. The results of this run are shown in Figure 3.

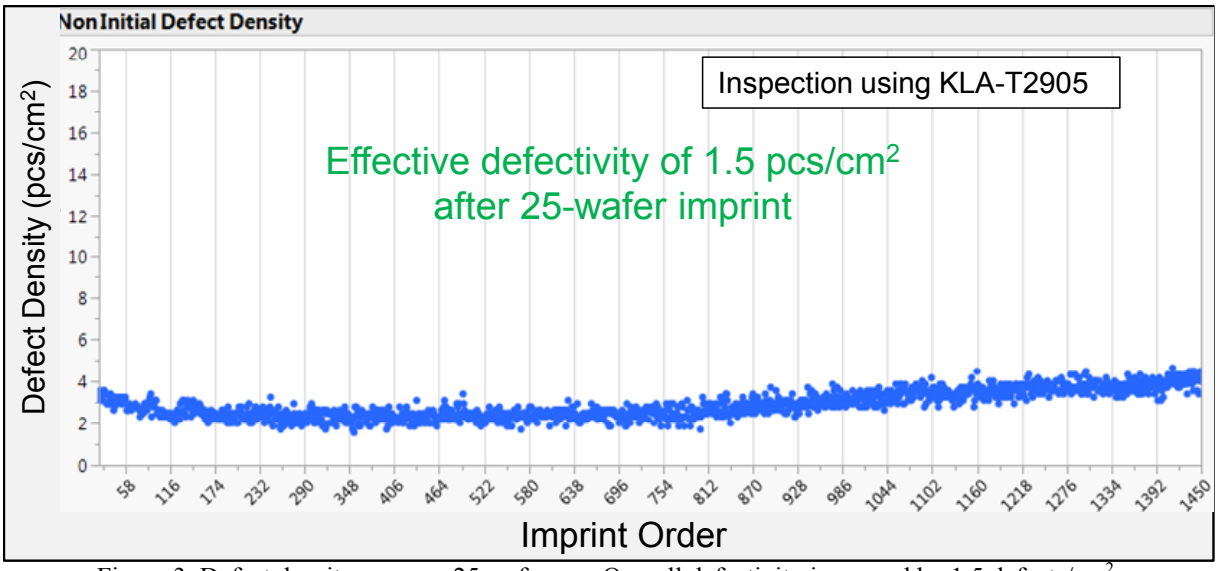

Figure 3. Defect density across a 25 wafer run. Overall defectivity increased by 1.5 defects/cm^2.

The test mask started with a baseline defectivity of ~ 3 defects/cm2. After the completion of the run, the defectivity increased by 1.5 defects/cm^2. This increase was anticipated, since wafers were prepared in one site and then shipped overseas for imprint testing. This was confirmed by inspecting all fields and performing a defect analysis. The analysis is shown in Figure 4 below. In the analysis, 61% of all defects were traceable to the previous layer on the wafer. Most importantly, however, was the confirmation of the fill time process. Only 0.8% of the defects were non-fill defects that can be attributed to resist filling issues.

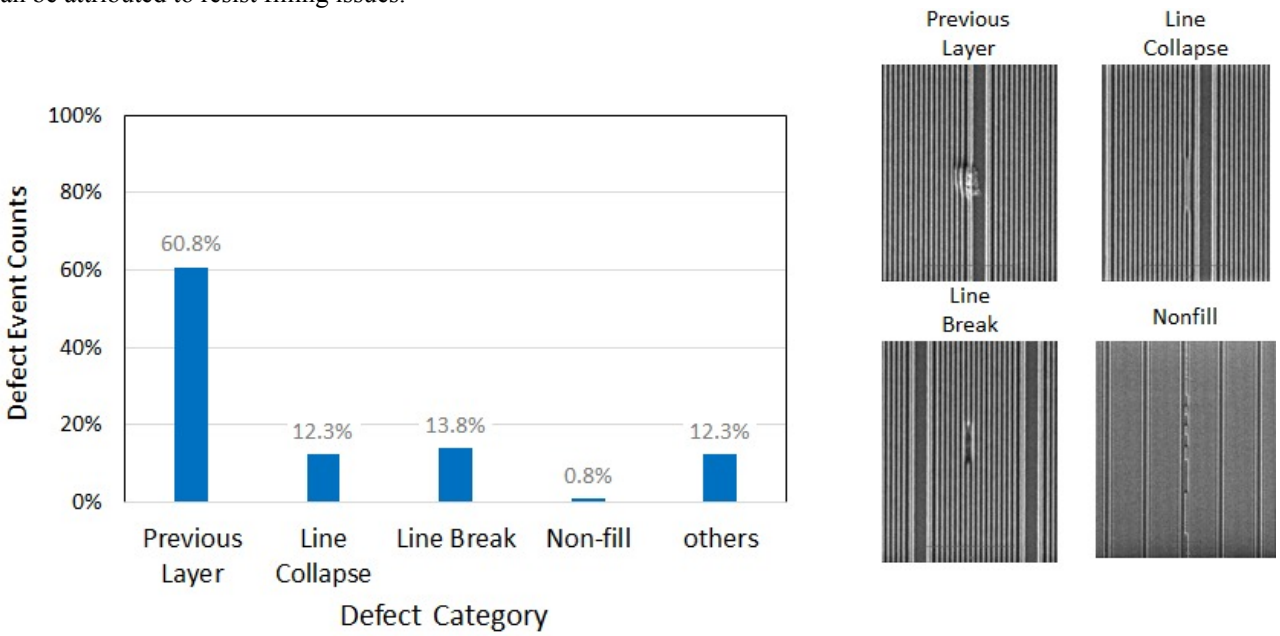

Figure 4. Defect breakdown across a 25 wafer run. Only 0.8% of the defects were fill time related.

a. 1.1 Second Fill Time – 80 wph

To achieve an 80 wph throughput, both fill time and overhead needed to be reduced. Targeted fill time for this work was 1.1 seconds. Again, the greatest challenges were in the kerf regions and were addressed with the following methods[13]:

1) Resist drop volume: sub-1.0pL
   - Smaller drops means decreased distances between drops
2) Drop pattern optimization based on imprint feature type:
   - Dense lines, contact holes, peripheral circuity, metrology marks
3) System hardware and controls
   - To address mask/wafer initial contact after jetting and drop spreading after contact

Fill time was tested by patterning both full fields and partial fields and the results are shown in Figures 5 and 6, respectively. Figure 5 describes full field non-fill defect density as a function of fill time. The non-fill defectivity remains constant until the fill time decreases to 1.0 seconds.

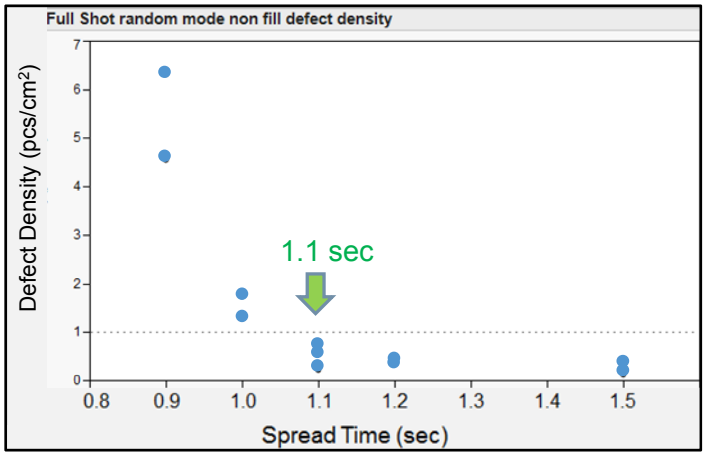

Figure 5. Full field non-fill defect density as a function of fill time. The non-fill defectivity remains constant until the fill time decreases to 1.0 seconds.

In Figure 6, non-fill defectivity is tracked for both the full fields and partial fields. It is important to note that several partial field locations require testing since the system controls need to be adjusted depending on the size of the partial field area.

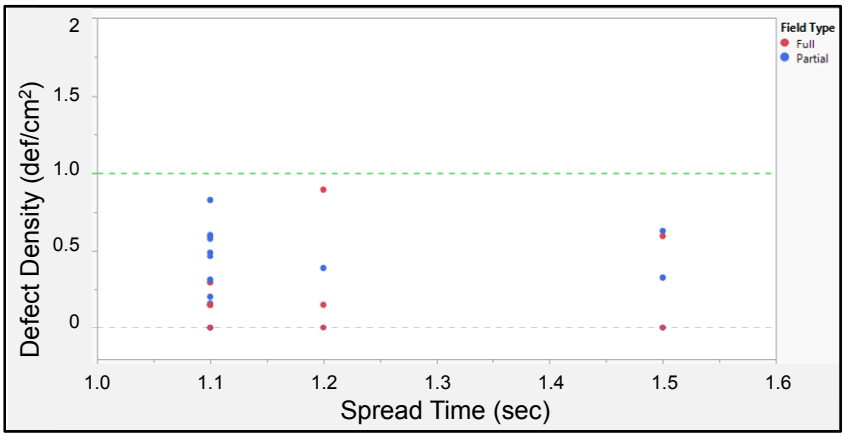

Figure 6. Full field and partial field non-fill defectivity. Defectivity is comparable for both field types.

Figure 7 summarizes progress for 60, 68 and 80 wph throughput testing. The 68 wafer per hour process has been verified on the NZ2C, and the initial 80 wph process are now being transferred to the production platform.

Filling Area	Fill Time (end of 2015)	Fill Time (mid 2016)	Fill Time (end of 2016)
FF: Core area 30nm L/S	1.2 sec	≤ 1.0sec	≤ 1.0sec
FF: Peripheral circuit	1.5 sec	≤ 1.0sec	≤ 1.0sec
PF: 30nm L/S	1.5 sec	≤ 1.0sec	≤ 1.0sec
FF: Marks in Kerf	1.5 sec	≤ 1.2sec	≤ 1.1sec
Tput (wph)	**60***	**68***	**80***

* Based on a 4-station NZ2C imprint tool.

Figure 7. Fill time and throughput summary

Conclusions

To achieve a total process throughput of 20 wafers per hour for a single station tool, it is necessary to complete the resist fluid fill step in 1.1 seconds. This work has demonstrated that by minimizing resist drop size, enhancing resist wetting, utilizing Design For Imprint and improving system controls it is possible to meet the fill time target necessary for 20 wafers per hour on a device like pattern. When applied to a four station cluster tool, the resulting throughput is 80 wafers per hour. The 1.1 second fill time work is now being ported to the production tool and additional testing will be done to verify overall throughput performance.

The next target is a 90 wafers per hour, which will require further fill time reductions in addition to addressing other overhead components.

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