Improved Defectivity and Particle Control for Nanoimprint Lithography High-Volume Semiconductor Manufacturing

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Abstract

Imprint lithography has been shown to be an effective technique for replication of nano-scale features. Jet and Flash* Imprint Lithography (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Criteria specific to any lithographic process for the semiconductor industry include overlay, throughput and defectivity. The purpose of this paper is to describe the technology advancements made in the reduction of particle adders in an imprint tool.

Hard particles on a wafer or mask create the possibility of creating a permanent defect on the mask that can impact device yield and mask life. By using material methods to reduce particle shedding and by introducing an air curtain system, test stand results demonstrate the potential for extending mask life to better than 1000 wafers.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

Keywords: Jet and Flash Imprint Lithography, J-FIL, nanoimprint lithography, NIL, defectivity, particles, mask life

1. Introduction

Imprint lithography is an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography* (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both CDU and line edge roughness meet the criteria of 2nm. A collaboration partner has achieved overlay of 10nm (with a target of 8nm) and defect levels ~ 5/cm² across a lot of 25 wafers. Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether Cost of Ownership requirements can be met. Recently, Takeishi and Sreenivasan reported that a throughput of 40 wafers per hour was achieved on a four station imprint tool.

On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6” x 6” x 0.25” photomasks. Complying with this standard provides the necessary tooling...
needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (<10nm) layer of chromium on the 6” x 6” x 0.25” fused silica was recently reported to have a defectivity of only 0.04/cm² as measured by a Lasertec tool with 50 nm sensitivity. Presently, Ichimura et al. have exceeded the targets for both CDU and IP. In addition, master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20 nm have been fabricated.

The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. In 2012, an MR-5000 mask replication tool was developed specifically to pattern replica masks from an e-beam written master. Previous work by Ichimura et al. using this tool, demonstrated that a CDU of less than 1.5nm 3σ can be achieved on both the master and replica masks. In 2012, an MR-5000 mask replication tool was developed specifically to pattern 6” x 6” x 0.25” replica masks from an e-beam written master.

As the most aggressive features in advanced memory designs continue to shrink below 15 or 16 nm (towards 1Z nm), the cost of fabricating these devices increases because of the large number of additional deposition, etch and lithographic steps necessary when using immersion lithography. Nanoimprint lithography (NIL) offers a more attractive Cost of Ownership (CoO) than competing technologies. Cost benefits can be realized by:

- Enabling direct printing of the features of interest, without the need for multiple patterning techniques.
- Improved mask life that allows a replica mask to be used for more than 1000 wafers.
- By improving the throughput of the NIL tool

The cost benefits are outlined in Figure 1, which describes CoO for a variety of lithographic methods to make both contact and dense line patterns with a 15nm half pitch. CoO is broken into three parts: the critical litho cost, mask cost and additional processing, indicated by the blue, red and green bars, respectively.

For contact holes, a 64% reduction in cost can be realized over an immersion lithography 2x SADP process. For dense lines, the cost reduction over immersion SAQP is 48%.

![Figure 1. Cost of Ownership comparison for various lithographic processes.](http://proceedings.spiedigitallibrary.org/ on 06/08/2017 Terms of Use: http://spiedigitallibrary.org/ss/termsofuse.aspx)

It is important to recognize however that both the replica mask life and the mask specifications must be compatible with device manufacturing needs. With respect to Cost of Ownership (CoO), it is anticipated that the lifetime of a single replica imprint mask will need to be on the order of 10^5 imprints, or approximately 1000 wafers. And for devices with half pitches compatible with 1Z nm memory, the replica mask must also meet strict criteria in image placement in order to meet the overlay specifications of the device.
In this paper, we will focus on the extension of mask life by reducing particle counts within the imprint tool, specifically focusing on air flow control, particle reduction methods and in-situ cleaning methods.

2. Background Information

Nanoimprint Lithography (NIL), like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL does have defect mechanisms unique to the technology, and they include, liquid phase defects, solid phase defects and particle related defects.

Liquid phase defects can form as the result of contamination to the underlying adhesion layer. The result of this contamination is incomplete filling in a small area, and is typically referred to as a non-fill defect. This defect type has been addressed in the past by applying the same sort of environmental filtering systems required, for example, for chemically amplified resists.

Solid phase defects can occur during the separation process. Shear forces imparted between the mask and wafer can tear features and potentially leave resist on the imprint mask. Another consequence of shear forces is line collapse and can be observed when the aspect ratio of sub-20nm features starts to grow well beyond 2:1. These defect types have also been overcome by careful attention to system controls during separation and are also no longer considered a priority. Examples of liquid and solid phase defects are shown in Figures 2a and 2b, respectively.

![Figure 2](http://proceedings.spiedigitallibrary.org/proceedingsgraphic.png)

Figure 2. Major defect types of Nanoimprint Lithography: a) non-fill defect in liquid phase, b) Separation defect in solid phase, c) particle defect.

More troublesome are particles that reside and adhere to either the mask or wafer surface. In the past we have described how the inkjet system can add to particle count and how liquid in-line filtration systems addressed this issue. These particle types were typically soft in nature and could be addressed by mask cleaning. Hard particles generated within the imprint tool are the biggest source of concern. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process. An example of a hard particle defect is shown in Figure 2c.

In summary,

- Liquid phase defects do not cause mask damage, do not require mask cleaning and can be addressed through environmental controls.
- Solid phase defects also do not damage the mask, but may require mask cleaning.
- Particles, break down into two categories: soft and hard. Soft defects rarely damage the mask. Hard particles, however impact mask life.
To put this point in perspective, consider that in order to meet the CoO specs shown in Figure 1, the replica mask life must be sustained for better than 1000 wafers. If we conservatively assume that:

- Every hard particle adds a defect to the mask, and
- The mask defectivity limit from hard particles is 0.1 pieces per square centimeter,

then the number of particle adders per wafer pass must be < 0.001. As a result, if we are to achieve this particle specification, an aggressive strategy is needed to remove particles adders to the wafer and mask. There are several countermeasures for particles that can be taken. Included on the list are:

- The minimization of particle generation from particle sources related to materials within the tool and the surface treatment of these materials.
- The reduction of particles that could potentially find their way onto the mask and wafer. These can be addressed by optimizing the airflow within the tool.
- Providing a means to control electrostatic charge within the imprint tool

In the next section, we review the previous approaches taken and present the status of this effort from the previous year.

3. Prior Work on Particle Reduction

a) Ceramic Treatment and Primary Air Curtain

In general, lithography tool manufacturers rely on the use of ceramic materials to reduce particle generation. What isn’t generally appreciated however, is that even ceramic materials continuously generate particles. As a result, several surface treatment methods have been developed to minimize particle generation. The upper left graph in Figure 3 shows an example of a ceramic that generates many particles over the course of several hours. By applying correct polishing, coating and heating methods, however, particle generation is significantly reduced. As an example, the graph on the bottom left shows particle generation after a special heating process. In this case, the relative particle generation is reduced to only 0.3% after the heat treatment. This type of strategy is applied for all relevant materials within the tool.

![Figure 3. Surface treatment methods for ceramic based materials. Special heat treatment methods can be effective in reducing particle generation from these surfaces to 0.3%.](http://proceedings.spiedigitallibrary.org/ss/termsofuse.aspx)
b. The Application of a Primary Air Curtain

A key point to be made is that even when particles are shed, that they don’t find their way to the mask and wafer surfaces. This is accomplished by applying air flow optimization methods to the tool, and in particular to the area of the mask and wafer. Figure 4 depicts a simulation of particles tracked in the wafer plane. Figure 4a shows a schematic of the tool. Incoming particles can initially be managed through the choice of material and material treatment, as well as ultrafine filtration systems. But these steps alone are not sufficient to meet defectivity goals, and additional countermeasures must be adopted to further reduce particles near the wafer. Figure 4b shows a simulation of particles tracked within the tool. Note that particles located above the wafer are substantially reduced relative to the rest of the tool. How this is accomplished is discussed below.

![Figure 4. a) Schematic of the imprint tool. b) A simulation of particles tracked within the imprint tool.](image)

An environmental test stand was developed specifically to study particle control. This test stand is capable of adjusting the starting environment within the tool. An example of how the system operates is shown in Figure 5. Particle counts were performed at two unique particle settings. The graph below shows the difference between an ISO Class 7 environment, where almost ten to the seventh particles are generated within a cubic meter and an ISO Class 0 environment.

![Figure 5. a) Environmental test stand operating at two different conditions: ISO Class 7 and ISO Class 0. b) Primary air curtain designed to reduce particulates at the plane of the mask and wafer.](image)

To address particles at the wafer plane, a primary air curtain system was introduced into the test stand, as shown in the schematic image in Figure 5b. This air curtain has already been applied to our NIL tools. To predict the effects of an optimized air flow system, an accelerated experiment was performed by setting the test stand for ISO Class 7 conditions.

The accelerated test was done by:

- Moving the stage equivalent to a full wafer run, and
- Operating the air curtain system in an ISO Class 7 environment
- Measuring wafer particle counts,
• And then extrapolating the equivalent ISO Class 2 values that are applied to the NIL tool.

The smallest particles measured had a diameter of 80nm and were measured using a KLA-Tencor Surfscan SP3.

In this experiment, we operated the test stand under two different conditions:

1. Without any air curtain, and
2. With the primary curtain

As shown in Figure 6, without any curtain, almost 3000 particles are generated on the wafer, with an equivalent ISO Class 2 count of 0.03 pieces per wafer pass. By applying the air curtain, we can reduce this number to 0.006 pieces, and under optimal conditions further reduce the particle adders to less than 0.003. Clearly, the air curtain operation was confirmed to have great potential for meeting the particle adder specification.

Figure 6. Particle adders per wafer based on two different operating conditions in the test stand. A primary air curtain was very effective in reducing particles at the wafer plane.

Figure 7 reviews imprint tool particle adder history up through February of 2016. Air flow control in the tool was established in 2014, and the air curtain system was introduced in the following year. The combination of improved ceramics and the optimized primary air curtain enabled a particle reduction down to 0.003 pcs/wafer, or 1 particle every 333 wafers. As a result of this work, the next established target was 0.001 pcs/wafer, or 1 particle every 1000 wafers.

Figure 7. History and roadmap for particle reduction in the imprint tool.
3. Recent Particle Reduction Work

Three additional modifications are being studied to further reduce particles within the imprint tool:

- An optimized air curtain that covers a larger area within the tool
- Further reduction of particles generated from other sources
- Electrostatic charge control.

Each topic is discussed in the sections below.

a. Air Curtain extension and optimization

The operation of the primary curtain was combined with optimized cleaning methods for both tool parts and the imprint tool itself, and was effective in further reducing particle counts to 0.0008 pcs/wafer, or approximately 1 particle every 1250 wafers, as shown in Figure 8.

![Figure 8. Recent history and roadmap for particle reduction in the imprint tool.](image)

While successful in reducing particulates, the previous version of the primary air curtain was restricted in its coverage within the imprint tool as shown in Figure 9a. The primary air curtain captured the entire area of the mask chuck, but did not include the wafer pick up area. Additionally, when the wafer stage moved beyond the borders of the primary air curtain, the particle environment was not as well controlled.

![Figure 9. a) Primary air curtain. b) Optimized air curtain providing extended coverage as the stage is moved.](image)

A redesign and configuration of the air curtain created a more optimized curtain that covered both the mask chuck and wafer as the stage is moved, as shown in Figure 9b. The result of this optimized design is shown in Figure 10,
which pictures particles captured on a wafer during accelerated testing. In this experiment, no particles were detected when the optimized air curtain equipped with extended coverage was applied. Plans are in place to start on-tool testing and results will be reported in the future.

![W/o Air Curtain](image1.png) ![Primary Air Curtain](image2.png) ![Optimized Air Curtain](image3.png)

Figure 10. The extended air curtain was effective in further reducing particle counts in a test stand under accelerated test conditions. Plans are in place to start on-tool testing in the future.

b. Particle Reduction

Materials other than ceramics also have the potential to generate particles. As an example, gas nozzles within the system often have rough surfaces that allow particles to shed during the operation of the nozzle. Mechanical and chemical polishing can reduce the roughness. Figure 11 shows the nozzle surfaces before and after polishing.

![Before](image4.png) ![After](image5.png)

Figure 11. Gas nozzle roughness before and after polishing.

To understand the efficacy of the process, airborne particulates generated from the nozzle surfaces were measured using a TSI AeroTrak® Model 9110 Portable Particle Counter. The results of particle studies are shown below in Figure 12. Airborne particle counts were reduced by more than a factor of 100 as a result of the polishing processes.
Airborne particle counts were reduced by more than a factor of 100 as a result of the polishing processes. 

**a. Electrostatic Charge Control**

Electrostatic charge can be generated on the surface of the imprint mask as a result of the separation of the mask and wafer after the exposure of the imprint resist. Charge can be addressed in two ways: One method is to attempt to remove the charge using various neutralization schemes. As second method is to create a charged environment away from the mask in order to preferentially attract charged particles to the charged environment. The basic concept is shown in Figure 13. An Electrostatic Cleaning Plate (ESCP) is placed adjacent to the mask and operated at a voltage greater than the voltage generated on the imprint mask. Initial on-tool results are very promising and will be reported in future symposiums.

![Figure 13. A schematic drawing of an Electrostatic Cleaning Plate (ESCP) designed to draw charge particles away from the mask surface.](image)

**Conclusions**

Great progress has been made in the field of nanoimprint lithography over the last two years. A key factor for the insertion of nanoimprint lithography in a high volume manufacturing facility is mask life, which is influenced, in part, by the cleanliness of the nanoimprint tool. The continued reduction of particle adders extends both the life of the master mask and the replica mask. In this work, methods for reducing particles generated from material surfaces were introduced, and an optimized air curtain
system was tested. Particle counts on a wafer were reduced to only 0.0008 pieces per wafer, or a single particle over 1250 wafers, with a next target of 0.0001 pieces per wafer.

Other particle sources within the tool have also been identified and minimized. Finally a potential method for minimizing mask charging and the resultant attraction of particles to the mask surface was also introduced.

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