Nanoimprint system development for high-volume semiconductor manufacturing and the status of overlay performance

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ABSTRACT

Imprint lithography has been shown to be a promising technique for replication of nano-scale features. Jet and Flash Imprint Lithography* (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

There are many criteria that determine whether a particular technology is ready for wafer manufacturing. Included on the list are overlay, throughput and defectivity. The most demanding devices now require overlay of better than 4nm, 3 sigma. Throughput for an imprint tool is generally targeted at 80 wafers per hour. Defectivity and mask life play a significant role relative to meeting the cost of ownership (CoO) requirements in the production of semiconductor devices.

The purpose of this paper is to report the status of throughput and defectivity work and to describe the progress made in addressing overlay for advanced devices. In order to address high order corrections, a high order distortion correction (HODC) system is introduced. The combination of applying magnification actuation to the mask, and temperature correction to the wafer is described in detail and examples are presented for the correction of K7, K11 and K17 distortions as well as distortions on actual device wafers.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

Keywords: Jet and Flash Imprint Lithography, J-FIL, defectivity, throughput, overlay, high order distortion correction

1. INTRODUCTION

Imprint lithography is a promising method for replication of nano-scale features and has been used to fabricated advanced memory devices.[1-3] Jet and Flash Imprint Lithography* (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate.[4-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both CDU and line edge roughness meet the criteria of 2nm. A

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collaboration partner has achieved overlay of 10nm (with a target of 8nm)[10] and defect levels ~ 5/cm^2 across a lot of 25 wafers.[11] In 2015, mix and match overlay results of less than 5nm were achieved. Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether CoO requirements can be met. Recently, Takeishi and Sreenivasan reported that a throughput of 40 wafers per hour was achieved on a four station imprint tool.[12] Further improvements, defining a path towards 60 wafers per hour were reported by Zhang et al.[13]

As the most aggressive features in advanced memory designs continue to shrink below 15 or 16 nm (towards 1Z nm), the cost of fabricating these devices increases because of the large number of additional deposition, etch and lithographic steps necessary when using immersion lithography.[14] Nanoimprint Lithography (NIL) offers a more attractive CoO than competing technologies. Cost benefits can be realized by:

- Enabling direct printing of the features of interest, without the need for multiple patterning techniques.
- Improved mask life that allows a replica mask to be used for more than 1000 wafers.
- By improving the throughput of the NIL tool
- By improving the overlay performance so that the technology can address both NAND Flash and DRAM devices

In this review paper, we focus on the wafer imprint tool, and briefly summarize the status of defectivity and throughput and then discuss the progress made in overlay performance. In order to address high order corrections, a high order distortion correction (HODC) system is introduced. The combination of applying magnification actuation to the mask, and temperature correction to the wafer is described in detail and examples are presented for the correction of K7, K11 and K17 distortions as well as distortions on actual device wafers.

2. Defectivity

NIL, like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL has defect mechanisms unique to the technology, and they include, liquid phase defects, solid phase defects and particle related defects. Examples of these types of defects have been discussed previously.[15]

Especially, more troublesome are hard particles on either the mask or wafer surface. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process. Because of this, hard particle is a primary factor to decide the mask life time. The methodology for removing particles can be broken down into categories:

- Reduction: The minimization of particle generation from particle sources related to materials within the tool and the surface treatment of these materials
- Removal: The reduction of particles that could potentially find their way onto the mask and wafer. These can be addressed by optimizing the airflow within the tool and by providing an ionizer source to address charge build up on the mask
- Rejection: The elimination of particles through an inspection and mask cleaning process flow.
- Tool preparation: Meaning the measures taken to insure tool cleanliness

Particle reduction and removal has been accomplished through a combination of applying air curtains to direct particles away from the mask and wafer, the treatment of ceramics to inhibit particulation and a combination of charge reductions methods. The results of these efforts are shown in Figure 1 below. A simulated run on the NZ2C yielded a single particle event for more than 1200 wafers, which is equivalent to a particle adder specification of 0.0008, surpassing the target of a 1000 wafer mask life. Further details on this work can be found in the paper by Nakayama et al. in this proceedings, and cover the additional topics of mechanical and chemical polishing to reduce particles generated from gas nozzles and the implementation of an electrostatic cleaning plate to direct particles away from the mask surface.

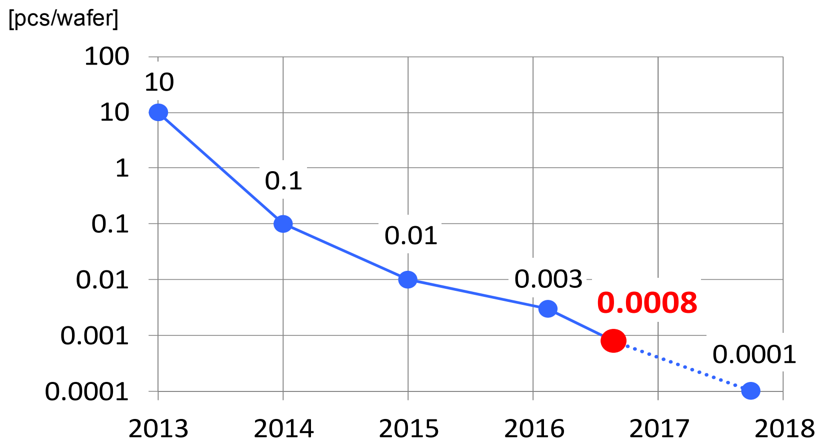


Figure 1. Historical improvements on tool particle adders

3. Throughput

There are several parameters that can impact resist filling. Key parameters include resist drop volume (smaller is better), system controls (which address drop spreading after jetting), Design for Imprint or DFI (to accelerate drop spreading) and material engineering (to promote wetting between the resist and underlying adhesion layer). In addition, it is mandatory to maintain fast filling, even for edge field imprinting. Previously, we have demonstrated that it is feasible to fill dense line/space patterns in only one second.

The resist properties have a large impact on fill time and the engineering of the resist is critical for meeting performance criteria and properties such as surface tension, viscosity and wetting. Surface wetting has a strong influence on fill time as shown in Figure 2. In this work, resist spreading was addressed in order to accelerate drop spreading on the surface of the wafer prior to imprinting. Resist fill time was tracked as a function of resist drop diameter. A 3x increase in drop diameter resulted in a reduction in fill time of approximately 0.6 seconds.

As a rule of thumb, a 1.1 second fill time is necessary to achieve a throughput of 20 wafers per hour per imprint station, or 80 wafers per hour for a fully configured four station cluster tool. Last year, we reported throughputs of 15 wafers per hour, with a 1.5 second fill time. Figure 3 shows the various methods employed to reach a throughput of 15 wafers per hour.[13] Presently, we are achieving throughputs of about 17 wafers per hour with a fill time of 1.2 seconds, and have demonstrated 1.1 second filling on device-like layouts. A detailed report on throughput by Ye et al. can also be found in this proceedings.

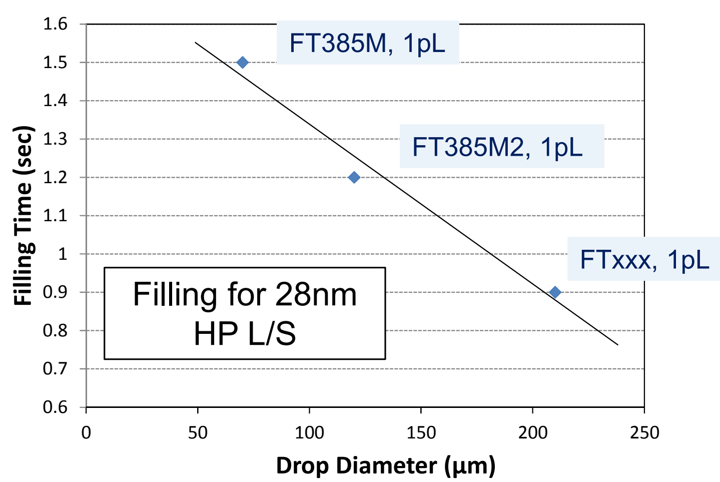


Figure 2. Resist fill time as a function of resist drop diameter for three different resist formulations. Improved resist spreading had a significant impact on fill time.

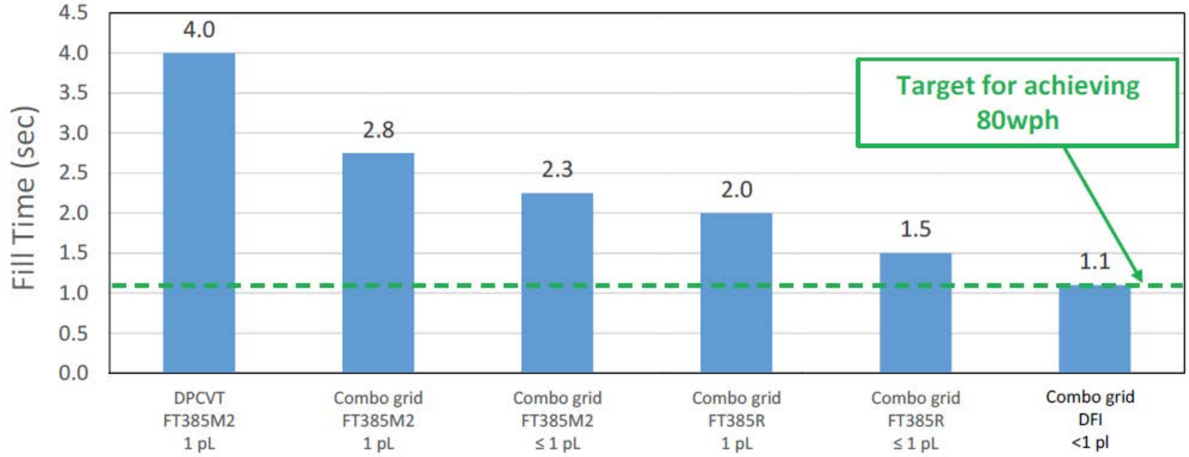


Figure 3. Fill time for five different conditions, demonstrating feasibility for printing 15 wafers per hour.

4. Overlay

The alignment and overlay system consists of various factors, which can be categorized generally as alignment and distortion. In a multi-station system, such as the NZ2C, it is important to recognize that overlay and distortion must be controlled within a station and from station to station. Additionally, the magnification actuator system initially employed for overlay is limited in its ability to correct for high order distortion signatures present on previously pattern levels of a device. Thus a method for correcting these distortions is required. In the following sections, we address all three subjects.

a. Through The Mask Alignment System

Using a through the mask (TTM) alignment system, 1nm repeatability has been demonstrated and the data collected by the TTM system correlates very closely with an Archer measurement tool. Canon has studied both Single Machine Overlay (SMO) and Mix and Match Overlay (MMO), and the results are reported below.

SMO measurements are not done in the same way as an optical projection system, since it is not possible to print a second time over the existing resist. As a result, the wafer must be removed after a first imprint, etched and then placed back in the tool for the subsequent imprint and overlay. Shown in Figure 4 are the SMO results across a full wafer and within a single field. Within a single field, an SMO of less than 1.2nm, 3sigma was observed. Across wafer, SMO was less than 2.2nm.

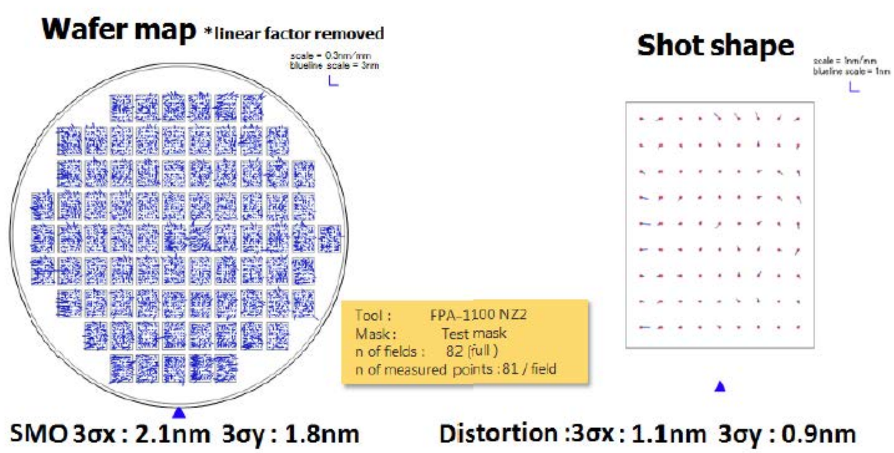
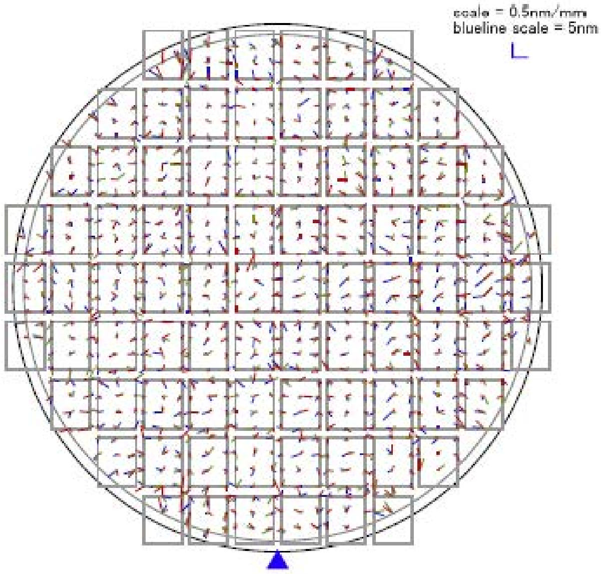


Figure 4. Single Machine Overlay measurements using the NZ2C imprint system. Within a single field, an SMO of less than 1.2nm was observed. Across wafer, SMO was less than 2.2nm.

The best mix and match overlay data is presented in Figure 5. Across the wafer, 4.0nm, 3sigma was observed.



Tool : FPA-1200 NZ2C
Mask : Test mask with 1x nm features
Substrate : ArF IML
n of fields : 84 (full and partial)
n of measured points : 12 / field

3wafers total [nm]

	X	Y
|m|	0.1	0.0
3σ	3.9	4.0
|m|+3σ	**4.0**	**4.0**

Figure 5. Mix and match overlay to an ArF immersion scanner. The three wafer average and 3 sigma values in x and y were 4.0 nm and 4.0 nm, respectively.

In a follow-up experiment, system stability was examined over a three day period. The average + 3 sigma mix and match overlay achieved over the three day period was 4.0nm in x and 4.2nm in y, as shown in Figure 6.

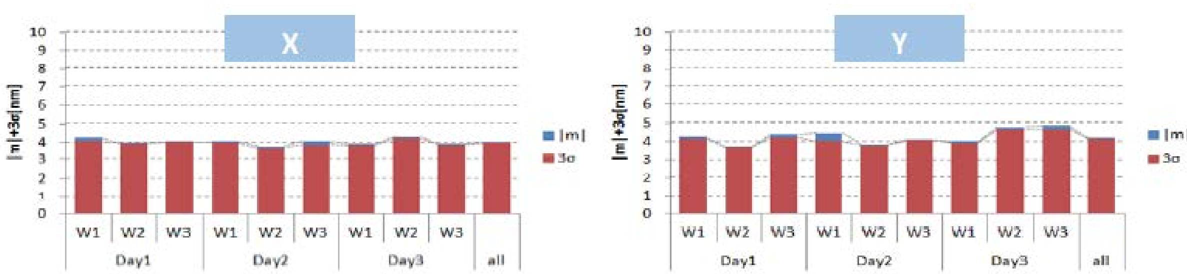


Figure 6. Mix and match overlay stability over a three day period. The mean + 3 sigma values in x and y were 4.0nm and 4.2nm, respectively.

b. Station to station variability

Initial tests have also been performed to understand the variability between stations in the NZ2C cluster tool. The first experiment examined variability between two stations across an eighteen wafer run. Measured were the translation, magnification and rotation residuals. As shown in Figure 7, the translation variability is well under 1nm and the magnification and rotation residuals were less than 0.10 ppm.

Figure 8 reports the average distortion residuals between two stations using two different masks. Data was collected across 58 fields of a wafer and the residual value was calculated by subtracting out the average distortion. The difference between stations and masks is less than 0.70nm.

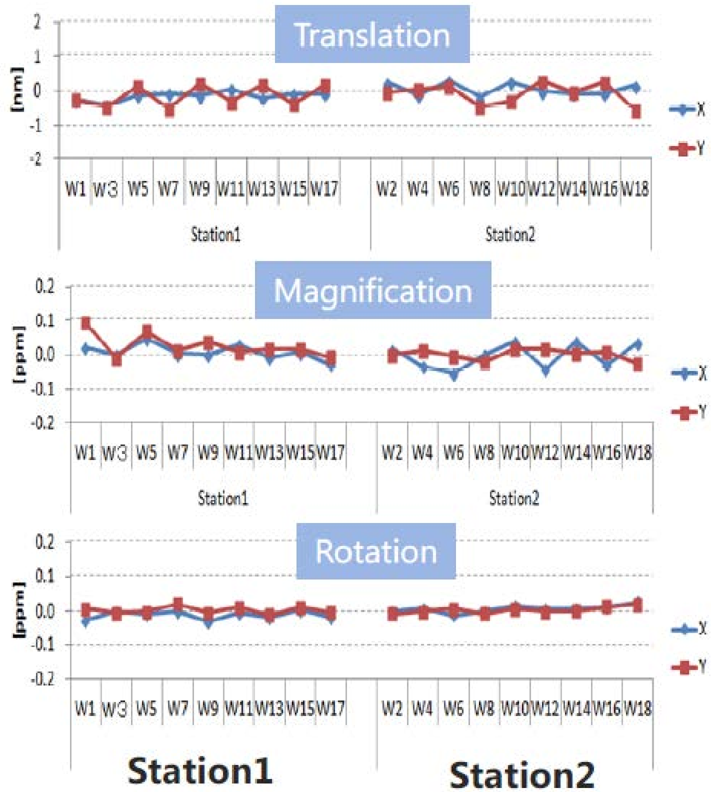


Figure 7. Translation, magnification and rotation variability between two imprint stations in the NZ2C.

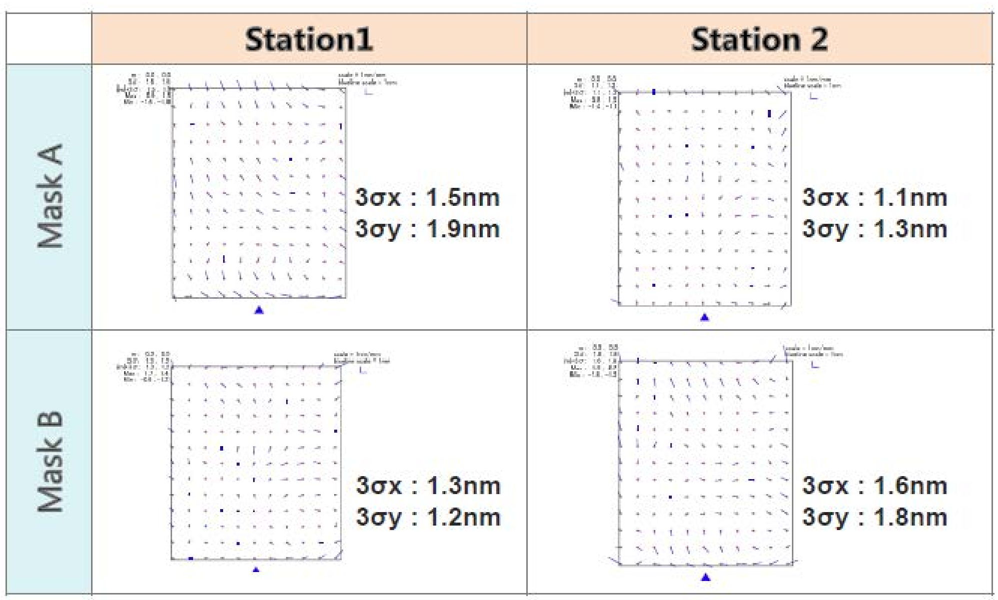


Figure 8. Residual distortion errors between two imprint stations using two different masks.

c. High Order Distortion Correction

It is important to note the difference in overlay approaches between an optical scanner and an imprint step and repeat tool. In an optical scanner, Shot Shape High Order Compensation (SSHOC) is done by manipulating both the stage and lens during the exposure process. A different approach is required for the imprint tool in order to do high order distortion controls (HDOC). HDOC for NIL can be enabled by combining two approaches:

1. Mag actuator, which applies force using an array of piezo actuators
2. Heat input to correct distortion on a field by field basis

Both approaches are described below.

With respect to the mag actuator, a larger array of piezo based actuators can be applied to do linear corrections. A simple schematic is shown in Figure 9.

Heat input on a field by field basis is also possible, and defines a potential path for achieving overlay results of better than 3nm. An example of this method is depicted in Figure 10. Figure 10a describes the heat input, temperature and initial shot distortion at time T = 0. Figure 10b shows the final heat input, temperature and distortion after 500 msec, which is well within the resist fill time budget of 1000 msec to achieve throughputs of 20 wafers per hour per imprint station.

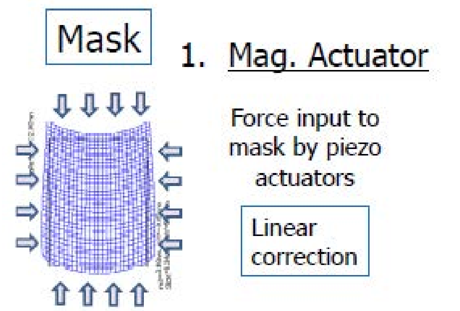


Figure 9. HOC correction using an array of piezo actuators.

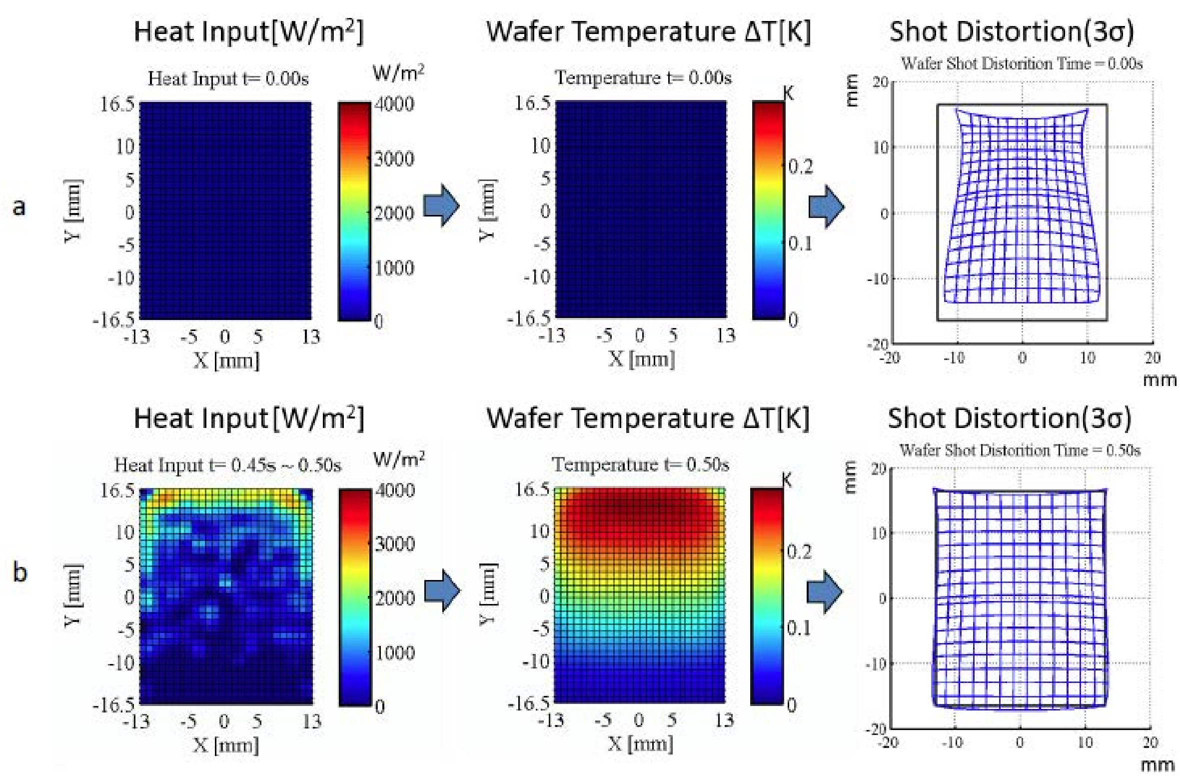


Figure 10. a) Shot distortion at time T = 0. B) Distortion after a heat input of 500 msec.

Initial heat input experiments have now been performed and the results are very promising. Simulation and experimental results are in excellent agreement, and a reproducibility across a four wafer set of ~1nm was demonstrated. Testing has now started on the NZ2C tool first looking at the ability to correct known high order terms such as K7 (2nd Magnifications), K11(Bow) and K17 (Pincushion).

Figure 11 describes the results of the experiment designed to address bow within a field. In the experiment, bow was targeted at 0.02 ppm/mm. To obtain the data, a first reference wafer was patterned by imprinting 58 full field shots with a -2 ppm mag offset. A second wafer was then patterned by imprinting 58 full field shots with the same mag offset and the heat input required to generate the desired bow. Average placement across each wafer was then calculated and the two field maps were subtracted. The results in Figure 11a show the difference between the targeted shape (in blue) versus the shape obtained experimentally (in red). The residuals are shown in Figure 11a for each of 143 measurement points. Very good agreement was observed, with maximum residual errors less than 1.3nm.

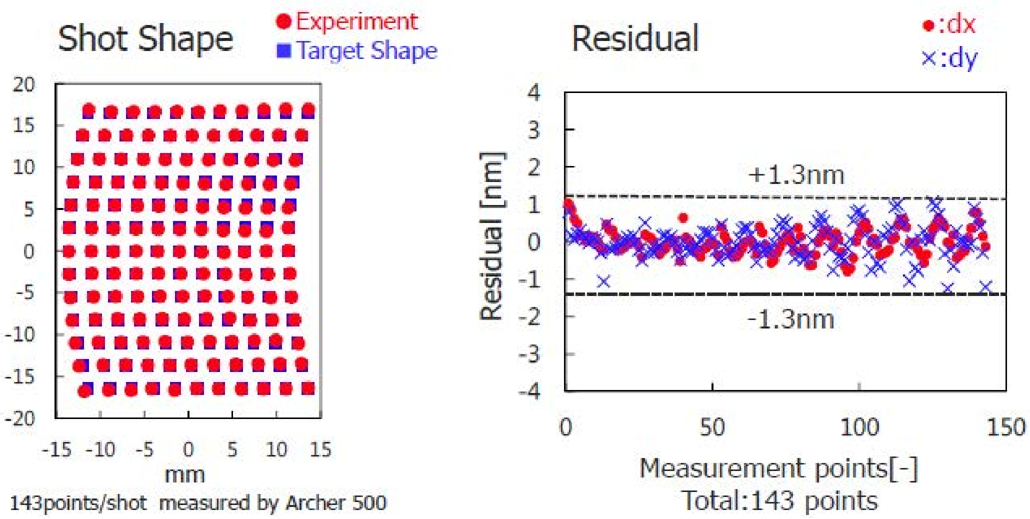


Figure 11. a)Targeted and experimental results for a K11 high order correction. b) Residual errors were less than 3nm.

Similar experiments were also done to look at K7 and K17 high order corrections. Again, the targeted and experimental values are in good agreement.

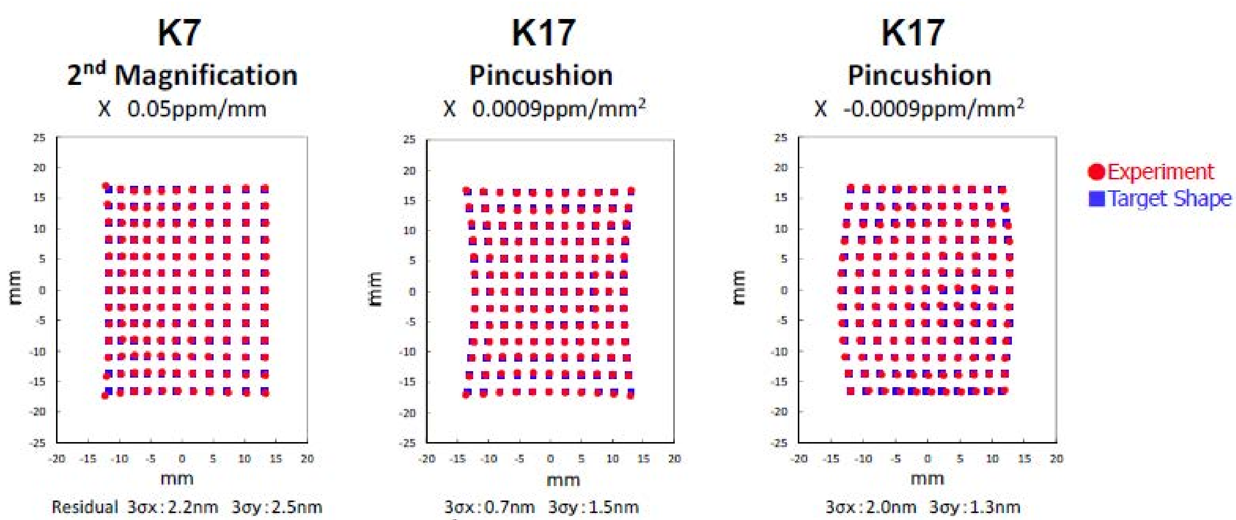


Figure 12. Good HODC obtained for K7 (2nd Magnification) and K17 (positive and negative Pincushion).

HODC was next applied to a device wafer which required a bow correction. The results are reported in Figure 13. Again excellent correction was confirmed, with residual errors less than 1.3nm as measured using an Archer 500 tool. Other high order terms can be corrected as well, but the thrust going forward will be targeted at device wafers.

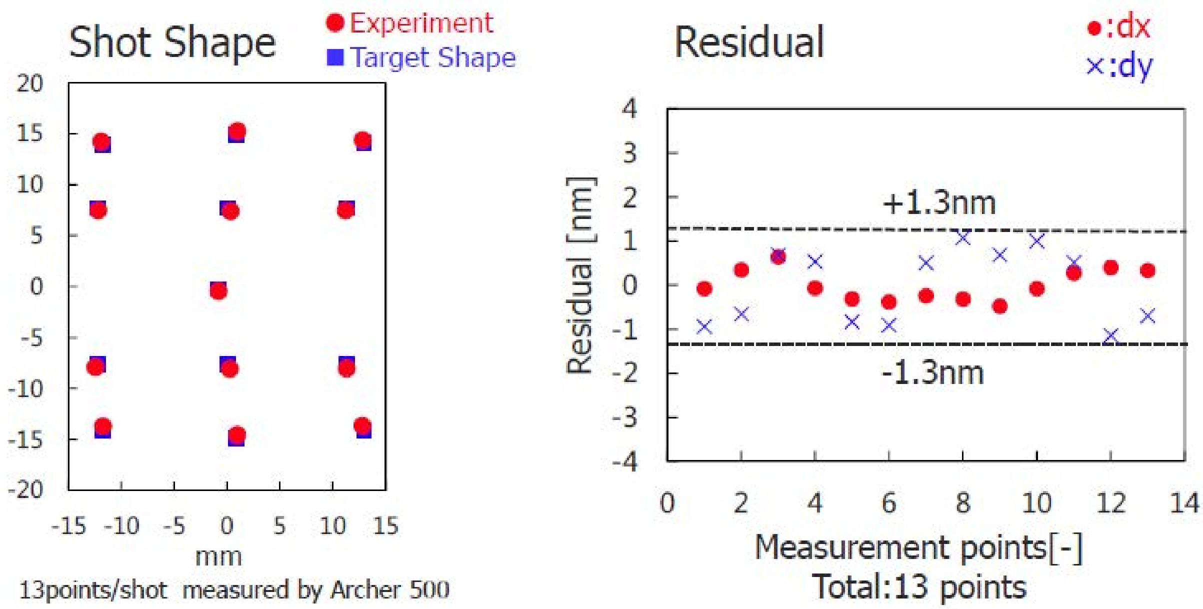


Figure 13. Corrected bow on a device wafer using the HODC system. Residual errors were again less than 1.3nm.

5. CONCLUSIONS

Great progress has been made in the field of NIL over the last three years. In this paper, to meet CoO requirements and to address yield issues, the progress on overlay, throughput, particle reduction and mask replication tool was shown. A mix and match overlay of 4.0 nm has been demonstrated and methods for reducing overlay error using heat input through a High Order Distortion Correction (HODC) system were introduced. The HODC system has successfully corrected bow, pincushion and 2nd magnification distortions and was also successful in doing corrections on device wafers. Throughputs of up to 20 wafers per hour per imprint station have also been achieved. The continued reduction of particle adders extends both the life of the master mask and the replica mask. In this work, an air curtain system was tested both on a test stand and on the imprint tool. In an optimized configuration in a test stand, the air curtain showed potential for enabling a particle adder count greater than 1000 wafers. Optimization of this new scheme as well as enhancements to the existing particle control systems, will aid in the further reduction of imprint defectivity, in order to meet the levels required for device manufacturing.

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REFERENCES

[1] S. Y. Chou, P. R. Kraus, P. J. Renstrom, “Nanoimprint Lithography”, J. Vac. Sci. Technol. B, 14(6), 4129 -4133 (1996).

[2] T. K. Widden, D. K. Ferry, M. N. Kozicki, E. Kim, A. Kumar, J. Wilbur, G. M. Whitesides, Nanotechnology, 7, 447 – 451 (1996).

[3] M. Hatano, K. Kobayashi, H. Kashiwagi, H. Tokue, T. Kono, T. Nakasugi, E. H. Choi, W. Jung, Proc. SPIE. 9777, Alternative Lithographic Technologies VIII, 97770B. (March 22, 2016).

[4] M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S. V. Sreenivasan, J. Ekerdt, and C. G. Willson, Proc. SPIE, Emerging Lithographic Technologies III, 379 (1999).

[5] M. Colburn, T. Bailey, B. J. Choi, J. G. Ekerdt, S. V. Sreenivasan, Solid State Technology, 67, (June 2001).

[6] T. C. Bailey, D. J. Resnick, D. Mancini, K. J. Nordquist, W. J. Dauksher, E. Ainley, A. Talin, K. Gehoski, J. H. Baker, B. J. Choi, S. Johnson, M. Colburn, S. V. Sreenivasan, J. G. Ekerdt, and C. G. Willson, Microelectronic Engineering 61-62 461-467 (2002).

[7] S.V. Sreenivasan, P. Schumaker, B. Mokaberi-Nezhad, J. Choi, J. Perez, V. Truskett, F. Xu, X, Lu, presented at the SPIE Advanced Lithography Symposium, Conference 7271 (2009).

[8] K. Selenidis, J. Maltabes, I. McMackin, J. Perez, W. Martin, D. J. Resnick, S.V. Sreenivasan, Proc. SPIE Vol. 6730, 67300F-1, (2007).

[9] I. McMackin, J. Choi, P. Schumaker, V. Nguyen, F. Xu, E. Thompson, D. Babbs, S. V. Sreenivasan, M. Watts, and N. Schumaker, Proc. SPIE **5374**, 222 (2004).

[10] T. Higashiki, T. Nakasugi, I. Yoneda, Proc. SPIE 7970 (2011).

[11] Z. Ye, K. Luo, J. W. Irving, X. Lu, W. Zhang, B. Fletcher, W. Liu, M. Shafran, S. Lee, W. Longsine, V. Truskett, F. Xu, D. LaBrake, Douglas Resnick, S. V. Sreenivasan, Proc. SPIE. 8680, Alternative Lithographic Technologies V, 86800C. (March 26, 2013).

[12] H. Takeishi and S. V. Sreenivasan, *Proc. SPIE*. 9423, Alternative Lithographic Technologies VII, 94230C. (March 19, 2015).

[13] W.Zhang, B. Fletcher, E. Thompson, W. Liu, T. Stachowiak, N. Khusnatdinov, J. W. Irving, W. Longsine, M. Traub, V. Truskett, D. LaBrake, Z. Ye, Proc. SPIE 9777, Alternative Lithographic Technologies VIII, 97770A (March 22, 2016).

[14] Ping Xu, Yongmei Chen, Yijian Chen, Liyan Miao, Shiyu Sun, Sung-Woo Kim, Ami Berger, Daxin Mao, Chris Bencher, Raymond Hung, Chris Ngai, Proc. of SPIE Vol. 7973 79731Q-1.

[15] Hiroaki Takeishi, S. V. Sreenivasan, Proc. of SPIE Vol. 9423, 94230C, 2015.