

NIL defect performance toward High volume mass production

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ABSTRACT

A low cost alternative lithographic technology is desired to meet with the decreasing feature size of semiconductor devices. Nanoimprint lithography (NIL) is one of the candidates for alternative lithographic technologies. NIL has advantages such as good resolution, critical dimension (CD) uniformity and smaller line edge roughness (LER). On the other hand, NIL involves some risks. Defectivity is the most critical issue in NIL. The progress in the defect reduction on templates shows great improvement recently. In other words, the defect reduction of the NIL process is a key to apply NIL to mass production. In this paper, we describe the evaluation results of the defect performance of NIL using an up-to-date tool, Canon FPA-1100 NZ2, and discuss the future potential of NIL in terms of defectivity. The impact of various kinds defects, such as the non-filling defect, plug defect, line collapse, and defects on replica templates are discussed. We found that non-fill defects under the resist pattern cause line collapse. It is important to prevent line collapse. From these analyses based on actual NIL defect data on long-run stability, we will show the way to reduce defects and the possibility of NIL in device high volume mass production. For the past one year, we have been collaborating with SK Hynix to bring this promising technology into mainstream manufacturing. This work is the result of this collaboration.

Keywords: Nanoimprint, Lithography, Template, Defect classification, Defect control

1. INTRODUCTION

In the CMOS semiconductor device (memory and logic) industry, there is a growing need to shrink the pattern size. Thus, a great deal of work has been conducted on the development of next generation lithography (NGL) technology. However, several major barriers in NGL have been encountered, including rising tool cost, delay in the development of a high performance tool, and poor performance of resist. The EUVL can be a candidate of the NGL to be capable of finer technology than hp20nm. In addition, further pattern shrinking is possible with the high NA EUVL and EUVL extendable technology. However, there are big challenges to EUVL realization like optical source power, mask infrastructure and resist performance. The light source maker's development road map is shown clearly about light source output performance improvement, and it is expected that further development for the improvement will proceed as planned based on the requirement. NIL also can be one of candidates of the NGL. Researchers have suggested NIL is a cost-effective technique for the replication of nano-scale features.^{1,2} It had been demonstrated that NIL has finer resolution capability with excellent CD uniformity and LWR as a low cost lithography technology.³ NIL is one of the candidates for NGL. NIL is a simple technology and is capable of forming critical patterns easily. On the other hand, its defectivity control is difficult, since the fine feature patterns on the template directly contact and transfer to the resist 1 to 1. There are unique defectivity types which are peculiar to the NIL process.⁶ It is a big challenge to achieve low defectivity desirable for semiconductor device fabrication. Authors address current NIL defectivity performances for semiconductor device fabrication, especially with the discussion about mass production from the defectivity control point of view. There has also been discussion about future work for mass production such as defectivity on replica templates, and the necessity of infrastructure in mass production.

2. EXPERIMENTAL RESULTS

2-1, Apparatus of experiment

a. Exposure tool

Imprinting was performed using the Canon FPA-1100 NZ2 system in Figure 1. FPA-1100 is processed based on Jet and Flush Imprint Lithography (J-FIL) which is shown schematically in Figure 2. The process starts with a template made from a standard 6025 photo mask blank, and then the patterns will be etched into the glass using the same technology for phase shift mask fabrication. An array of pico-liter sized drops of a low viscosity imprint resist is spread across the field being imprinted as the template is lowered onto the drops. When the surface tension of the liquid phase imprint resist has been broken, capillary action draws the resist into the template features. Once the filling is complete, ultraviolet (UV) light, passing through the glass template, is used to cross-link the resist and convert it to a solid. The template then is withdrawn and leaves a patterned resist on the substrate. The process is repeated on the next field to populate the substrate completely.

b. Templates

Replica templates made with commercial photo mask materials were used in this experiment. Since NIL is a 1 to 1 transfer system, the resolution, CDU, image placement and defectivity of the replica templates are important. Master templates were written with high quality Variable Shape Beam (VSB) mask writers with 50keV. Replica templates are made by duplicating the master template by using the NIL technique in DNP. 5 For the replica imprint, the same J-FIL technology is used using MR-5000. Imprint templates are already being written; we can imprint down to hp1x-nm dense line and space patterns, 2x-nm contact hole patterns, diagonal patterns, and 1x-nm pillar patterns with very high quality of feature fidelity (Figure 3).



Fig.1. Canon FPA-1100 NZ2 (Left)

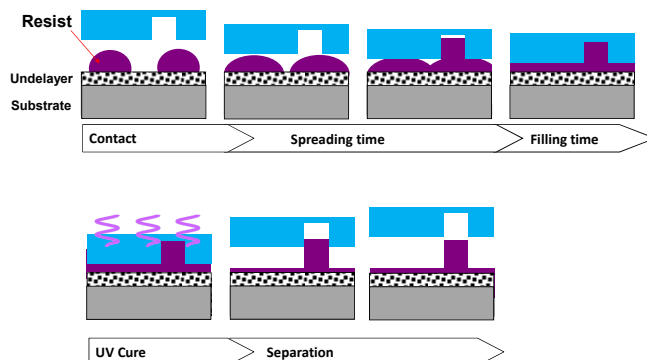


Fig.2. Schematic of J-FIL. (Right)

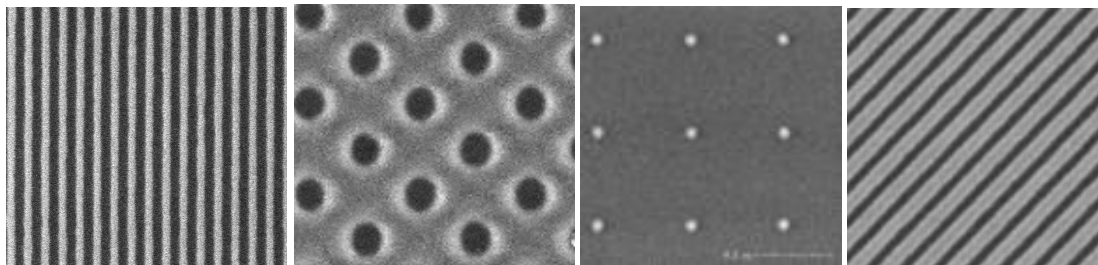


Fig.3. Example of resist patterns formed by NIL (1x-nm hp dense line and space, 2x-nm hole, 1x-nm pillar, diagonal pattern)

2-2, NIL defect classification

Based on the defect data collected using the process described in 2-1, the defects encountered in the NIL process can be classified as shown in Figure 4. There are four primary types of defects: (i) Defects on the template; (ii) Non-fill defects; (iii) Line collapse, and (iv) Plug defects. The nature of these four types is presented in the next subsections.

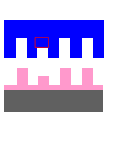
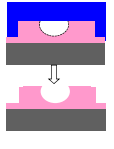
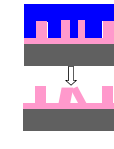
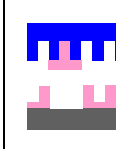
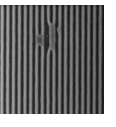
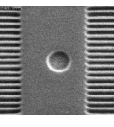
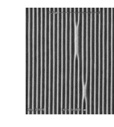
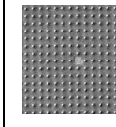
	<i>Template</i>	<i>Non-fill</i>	<i>Collapse</i>	<i>Plug</i>
Model of defect				
Defect image				
	<i>Repeater</i>	<i>Random (NIL Process defect)</i>		

Fig.4. Classification of NIL defects and SEM images

a. Defects on the template

Defects on the template print repeatedly on the wafer. The defectivity performance on the templates is important to reduce the total defect number of NIL. Defects on replica templates are classified three types. (i) Defects transferred from the master template (Master defects), (ii) defects generated in the fabrication of replica templates. (Replica defects) (iii) pattern damage by particles. Defects on master templates can be eliminated by repair technique, currently (ii) replica template defects are dominant in the performance of template defects. Figure 5 suggests the recent progress in the performance of replica defects. Defect performances of less than 0.1 [pcs/cm²] were achieved on 2x-nm replica templates. For a further improvement in defectivity on 1x nm template, a high sensitive defect inspection tool is a must.

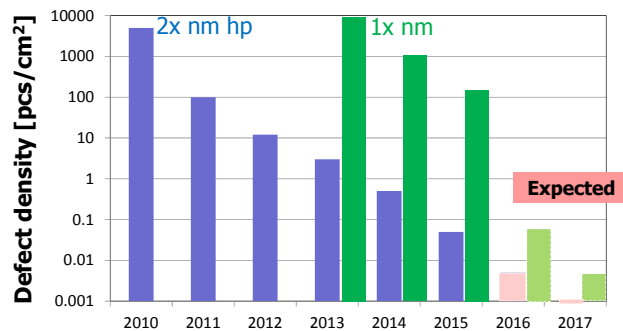


Fig.5. Defectivity obtained on replica templates.

b. Non-fill defects

Non-fill defects are trapped bubbles in the resist and do not form a pattern. Non-fill is generated when there is not enough time for the spreading and filling process. Insufficient surface energy control of the template and underlayers also cause non-fill defects. Non-fill defects determine the process time of each shot. In order to enhance the throughput of NIL, it is important to develop a method for the quick dissipation of residual bubbles from the ambience between the template and the wafer. 7,8

c. Line collapse

Line collapse defects are the feature pattern collapse of the resist, which is caused by its poor stiffness and too high shear stress when a template is separated from the patterns on a wafer. In order to reduce line collapse, higher stiffness of the resist is required and a lower shear force in the separation process.

d. Plug defects

Plug defects occur when the resist is attached on the template instead of staying on the substrate. Plug defects are also caused by the poor stiffness of the resist, insufficient adhesion on the underlayer and the poor release property of the template surface as well as high shear stress during the separation process. To avoid a higher separation force when the template is withdrawn from the resist, the design of the template is important.⁹ It is also known that small soft particles cause plug defects.¹³ Particle control in the resist supply system and resist material which has higher stiffness are important in reducing plug defects.

2-3, Defect results

In the early stage, NIL defects increase shot to shot (Figure 6). The primary defects were plug and non-fill ones. The linear increase in defects is mainly caused by plug ones. The non-linear term of defect increase is related with surface contamination from the environment. Plug defects were reduced by resist material improvement and the filtration of the resist supply system in the NIL tool. Environmental chemical control was effective in avoiding non-fill defects. After implementing these controls and by several process optimizations further, a drastic reduction in NIL defectivity was obtained on the wafer. NIL defect density was down to less than 2 [pcs/cm²] and no obvious increase in defect density was found (Figure 7). The defect density fluctuates around 0 to 2 [pcs/cm²]. We have captured hundreds of SEM images and inspected them for residual defects. The primary residual defects are line collapse (Figure 8). These line collapses are compound defects of non-fill and line collapse. Non-fill defects under the feature pattern cause line collapses. We found two mechanisms for these compound defects. Firstly, the template surface has higher surface energy and capillary force because of the fine feature pattern on the template. Better wettability of the template surface makes it easy to trap bubbles. Secondly, contamination in the resist material and contaminant adsorbed on the underlayer stabilize nanobubbles and extend the length of life. Surface energy control of the surface and the development of higher gas dissolution rate material as well as environmental chemical control will result in an improved defectivity down to 0.01[pcs/cm²]. The overall trend in the total defectivity over the last eight years is presented in Figure 9. All of these data were obtained using a KLA28xx wafer inspection tool. The trend is clearly improved year by year as a log scale. Figure 10 shows the key five components of NIL defects. We call this the mandala of NIL defects. In this paper, I described NIL process defects, which are mainly caused by the resist, the wafer, and the NIL tool system. The NIL defect density toward HVM will be accomplished by an improvement in each key area, such as the design of the template and its quality. Especially, low defectivity templates at least less than 0.1[pcs/cm²] are inevitable toward HVM.

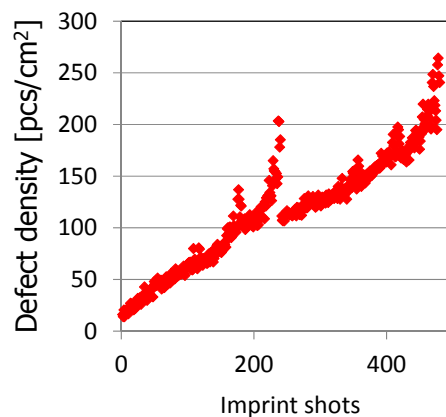


Fig. 6. Defectivity trend of NIL process in the early stage (obtained by α -tool)

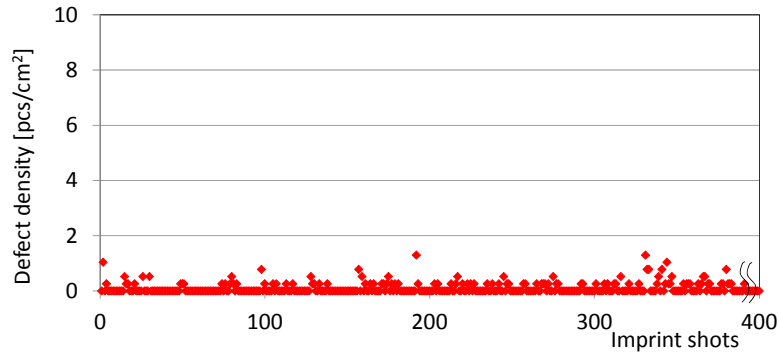


Fig. 7. Up-to-date defectivity trend of the NIL process (obtained by FPA-1100 NZ2)

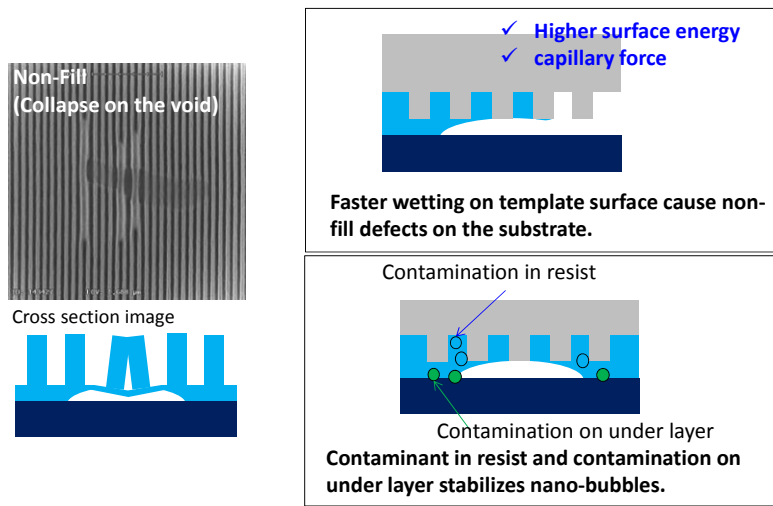


Fig. 8. Defect mechanisms of line collapse.

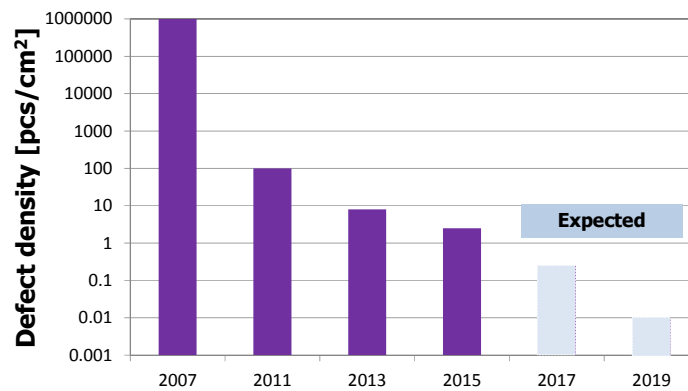


Fig. 9. Defectivity trend obtained on the wafer and expected.

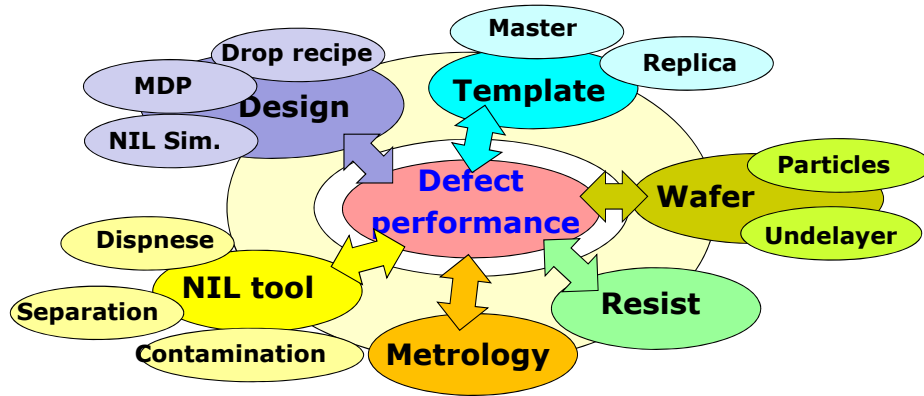


Fig. 10. NIL defect mandala

3. CONCLUSION

In this paper, we studied the defectivity of 2x nm hp performed by NIL. Recent progresses in the NIL tool, process and replica templates have brought a dramatic improvement in the defectivity performance. We have investigated the mechanism of residual defects and have found that the development of higher gas dissolubility material and environmental control will allow a further improvement in the stability of NIL defects. The results of our experiment clearly showed the following, i) NIL can cost-effectively fabricate sub 2x-nm structures with arbitrary patterns, such as dense lines and spaces, diagonal lines, holes and pillar patterns. ii) Defectivity of NIL process for 2x nm hp is getting close to the target of HVM. Lithography technology has been evolved and screened for the last 40 years and needs to continue to evolve for the growth of the semiconductor industry. NIL is promising technology for HVM in 2xnm hp and beyond.

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REFERENCES

- [1] S. Y. Chou, P. R. Kraus, P. J. Renstrom, "Nanoimprint Lithography", J. Vac. Sci. Technol. B 1996, 14(6), 4129 - 4133.
- [2] T. K. Widden, D. K. Ferry, M. N. Kozicki, E. Kim, A. Kumar, J. Wilbur, G. M. Whitesides, Nanotechnology, 1996,7, 447 - 451.
- [3] I. Yoneda, S. Mikami, T. Ota, T. Koshiba, M. Ito, T. Nakasugi, T. Higashiki, Proc. SPIE vol.6521-03 (2008).
- [4] Tatsuhiko Higashiki, Tetsuro Nakasugi, Ikuo Yoneda : " Nanoimprint lithography and future patterning for semiconductor devices," J. Micro/Nanolith. MEMS MOEMS 10(4), 043008 (Oct-Dec 2011)
- [5] K. Ichimura, et al, Proc. of SPIE 9423(2015)
- [6] J. Perez, et al, , Proc. of SPIE 6517 (2007)
- [7] Ikuo Yoneda, et al, Proc. of SPIE Vol. 7271 (2009)
- [8] Xiaogan Liang, Hua Tan, Zengli Fu, Stephen Y Chou, *Nanotechnology* 18 (2007) 025303 (7pp)
- [9] S. Kobayashi, et al, Proc. of SPIE Vol. 9049 (2015)
- [10] Zhengmao Ye, et al, Proc. of SPIE Vol. 8680(2013)
- [11] H. Takeishi, S. V. Sreenivasan, SPIE Advanced Lithography 2015