Design for nanoimprint lithography: Total layout refinement utilizing NIL process simulation

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ABSTRACT

Technologies for pattern fabrication using Nanoimprint lithography (NIL) process are being developed for various devices. NIL is an attractive and promising candidate for its pattern fidelity toward 1z device fabrication without additional usage of double patterning process. Layout dependent hotspots become a significant issue for application in small pattern size device, and design for manufacturing (DFM) flow for imprint process becomes significantly important. In this paper, simulation of resist spread in fine pattern of various scales are demonstrated and the fluid models depending on the scale are proposed. DFM flow to prepare imprint friendly design, issues for sub-20 nm NIL are proposed.

Keywords: nanoimprint lithography, resist fluid, alignment, shear stress, design for imprint

1. INTRODUCTION

Nanoimprint lithography (NIL) has been developed targeting various devices, and its extensions into fine devices such as NAND Flash memories is being expected. An example of famous ancient imprint seal, The King of Na gold seal of 2000 years ago, has five Chinese characters on it, and it represents ten byte of information. After 2000 years, amount of storage information has been increased by more than 20-th power of 10 and is increasing in many field, to manufacture various devices.[1-6)]

Conventionally, computational lithography has been developed based on optics, as means of improving CD uniformity (CDU), optical proximity correction (OPC), overlay (OL), and defects performance (Figure 1 a). On the other hand, the NIL, that is consisting of contact process, completely different from optical lithography. So new model of nano-mechanics, fluid engineering are necessary (Figute 1 b). Furthermore, understanding and building of an innovative physical model is indispensable. In this paper, examples of computational lithography for NIL is described to construct design for manufacturing (DFM) for NIL. As the pattern size on the substrate continuously shrink, mold longevity, CD uniformity and residual layer thickness (RLT) uniformity becomes more and more critical. Hence, DFM for NIL becomes absolutely necessary.

2. COMPUTATIONAL LITHOGRAPHY FOR NIL

2.1 Nanoimprint lithography simulation model

In figure 2, process simulators corresponding to each NIL steps are illustrated. Figures at the top, middle and bottom row represent NIL process steps, CDU issues, and defect density issue respectively. Various kind of simulators such as, structural simulator[7-8)], fluid simulator, stress simulator are necessary in order to identify critical controlling factors and predict prevention method beforehand. For simulation of imprinting process, we think that small sized resist flow between mold and substrate is essential. In figure 3, resist fluid simulations are mapped according to the process representative size. Vertical axis represents calculation amount. In the resist drop spreading process, the spreading

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distance is around a few hundreds micron, and general fluid simulation based on Navier-Stokes equations and RLT simulator is usable. The filling size is around tens of microns for simulation of resist spreading and filling behavior during imprinting process, and thus, the effect of surface tension is very significant. To simulate this process, viscoelastic fluid simulator is usable, although careful calibration is necessary. To simulate resist behavior of thin RLT below 20nm, local friction and molecular behavior has to be considered, due to the shear stress during the alignment process. In this case, advanced fluid simulator is necessary. For simulation of resist behavior of further smaller size, such as NIL process with thinner RLT or mold with smaller pattern size, molecular behavior has to be taken into consideration, and thus molecular dynamics simulator may be usable[9,10)]. In this case, calculation amount is expected to be enormous. So, to predict resist behavior in the process, novel and simple physical becomes increasingly necessary.

In the following section, several examples of resist flow simulation is shown.

2.2 RLTU improvement utilizing RLT simulator

In figure 4 a, RLT Uniformity (RLTU) improvement flow utilizing RLT simulator is illustrated. RLTU significantly affects CD uniformity after etching, and hence the RLTU improvement in NIL process is one of the most critical issues. Major control knob to improve RLTU is considered to be resist droplet placement recipe. Although iterative RLT measurement and droplet placement calibration takes time and effort, RLT simulator is helpful. An example of droplet placement recipe refinement is shown in figure 4 b-d. Figure 4 b indicates color chart of density map in test chip used in this experiment. Before correction, droplet placement recipe figure 4 c-1 is used for NIL, and the corresponding RLTU is that shown in figure 4 d-1. After correction, droplet placement recipe (Figure 4 c-2) is used, and the corresponding refined RLTU is that shown in figure d-2. RLTU is slightly improved, but still some variation is remained. For further improvement, we think that droplet placement grid, droplet volume, and algorithm has to be refined.

2.3 Dependency of Resist Flow on Layout

An example of Resist flow dependency on layout is shown in figure 5. Resist flow simulation result is shown in figure 5 a and b. In the case of blank template (figure 5 a) i.e., template with flat non-patterned surface, resist droplets spread isotropically on substrate. On the other hand, resist spreads along the direction of lines and spaces in the case of patterned template (figure 5 b). Experimental result is shown in figure 5 c, d and e. Resist is placed on the substrate as shown in the blue area in figure 5d and imprinted using patterned template (figure 5 c) with 28 nm lines and spaces, The resist is then cured after one second, four seconds and ten seconds as shown in figure 5 e. Spread resist shapes are similar to the results of the simulation. This resist flow pattern dependency is considered to be derived from the effect of surface tension.

2.4 Bubble trap caused by resist flow

Figure 6 illustrates various classed of NIL process defect. Among these, the non-fill defect that is, derived from helium bubble trap, is one of the significant issues in NIL. To analyze this defect, resist flow simulation considering surface tension is performed as shown in figure 7. Resist spread on template and substrate due to surface tension. At the flow front of the resist, the length of the contact-periphery between resist and template is longer than that of resist and the substrate. Thus, resist proceeds faster on template due to the larger surface tension on template. As a result, helium bubbles remained on the substrate. This mechanism is considered to be one of the causes of non-fill defect. To prevent the defect, layout modification to prevent bubble trap is necessary. Furthermore, calibration of properties of resist and substrate is indispensable.

2.5 Stagnant behavior of resist at thin residual layer thickness

It is known that alignment shear stress increases at thin RLT. An example is shown in figure 8. Max shear stress between template and wafer increases significantly with RLT below 10 nm. Figure 9 demonstrates plausible mechanism. Resist monomers flow freely in the region apart from the substrate during alignment sequence. In the region neighboring the substrate, rearrangement of resist monomers increases the apparent viscosity. The pseudo and simple simulation, based on this assumption, is shown in figure 10. At each figures, the bottom side is the resist contact region with the substrate. Apparent viscosity is set higher in this region of stagnant layers. Under such condition, resist proceeds more rapidly in the region apart from substrate whereas, it proceeds slowly in the region of stagnant layer (Figure 10 a - h). In order to analyze more detailed mechanism, more advanced simulation, such as molecular dynamics is necessary.

3. ISSUES FOR MODEL OF SUB-20 NM NIL AND BEYOND

In this section, issues for sub-20nm NIL and beyond is indicated. At first, as the pattern size nears molecular size, pattern roughness consideration becomes increasingly necessary. As thinner RLT is necessary for smaller sized patterning, adhesion force during alignment is further increased. New resist with superior frictional property is useful even with thinner RLT. For ultra-thin RLT, roughness on template and substrate affects separation force. Separation force is increased for the high Meniscus force of resist between template and substrate. Therefore, further RLTU improvement is important. Considering these models, NIL friendly design, such as the design that enhances the escape of bubble out of resist, is be prepared beforehand.

4. SUMMARY

In this paper, examples of computational lithography for NIL is demonstrated. NIL is a kind of contact process, and new models including mechanics, fluid engineering are necessary. Furthermore, understanding and building of an innovative physical model is indispensable. Nano-scale resist flow simulations are performed for RLTU improvement utilizing RLT simulator, understanding the dependency of resist flow on template layout, bubble defect derived from surface tension difference on template and substrate, and shear stress against RLT. For sub-20 nm pattering with NIL, new physical models are necessary such as monomer/polymer rearrangement, and model of nano-scale bubble generation. Toward NIL application for mass production, building of precise NIL models and implementation to electronic design automation (EDA) is indispensable.

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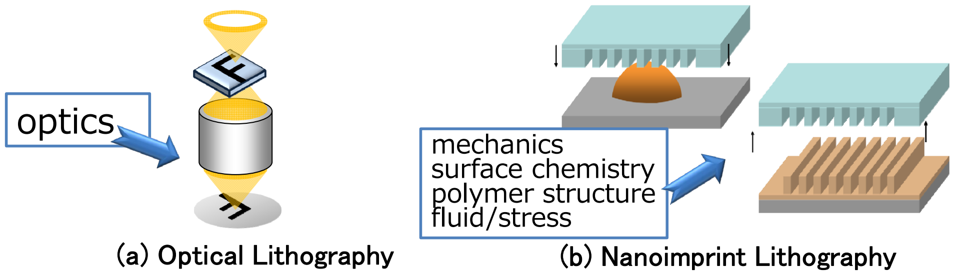

Figure 1: Comparison of computational lithography model for optical lithography (a) and Nanoimprint lithography (b).

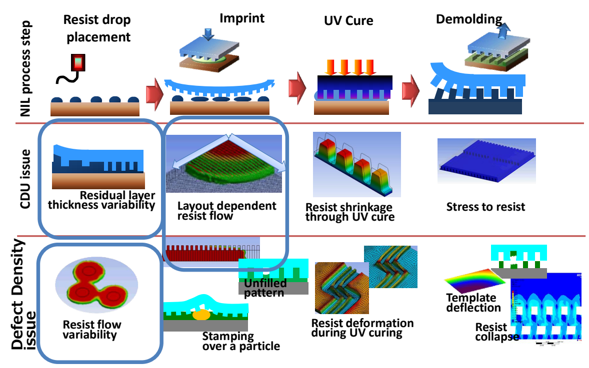

Figure 2: Computational NIL model corresponding to the each NIL process steps

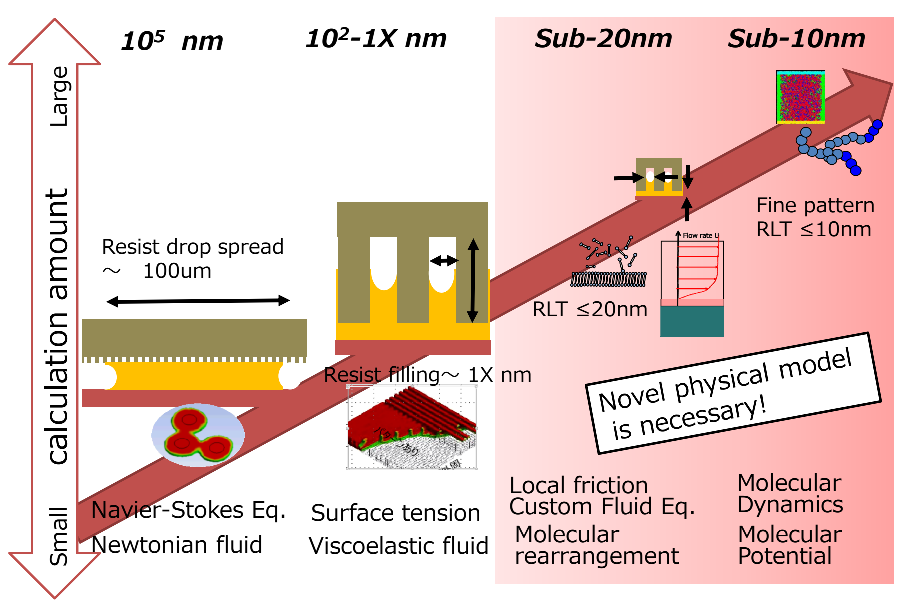

Figure 3: Resist behavior models against the size scale.

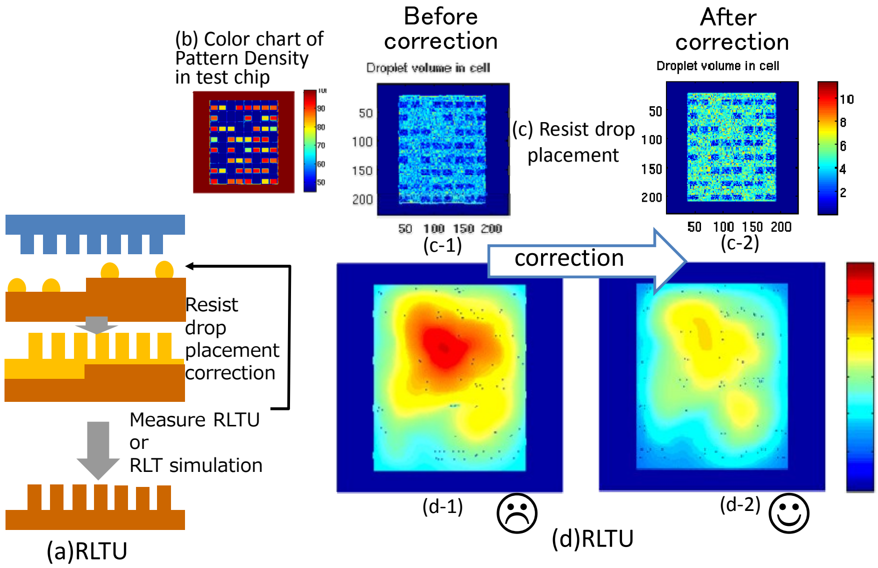

Figure 4: RLT Uniformity (RLTU) improvement utilizing RLT simulator.

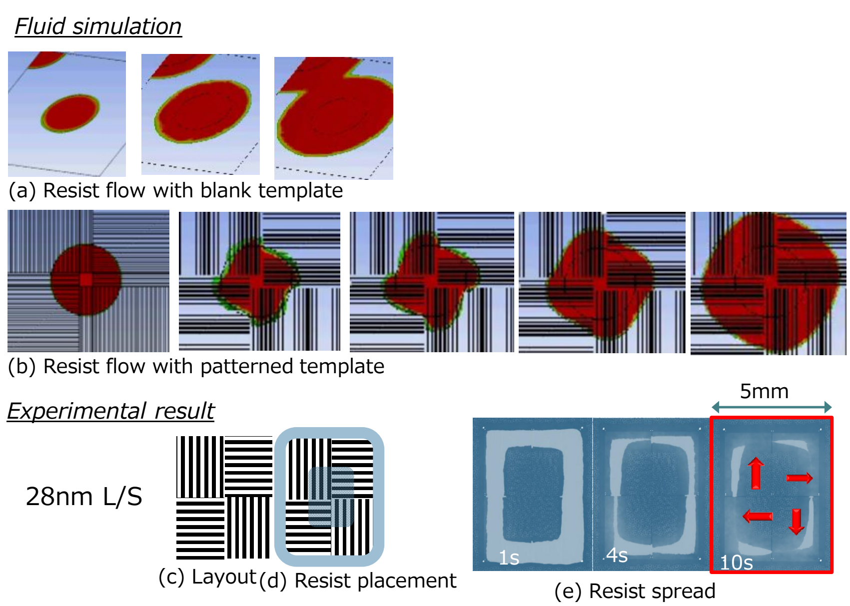

Figure 5: Dependency of Resist Flow on Layout in NIL process.

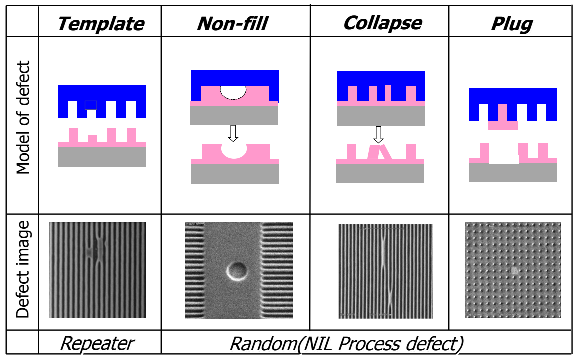

Figure 6: NIL process defect classification.

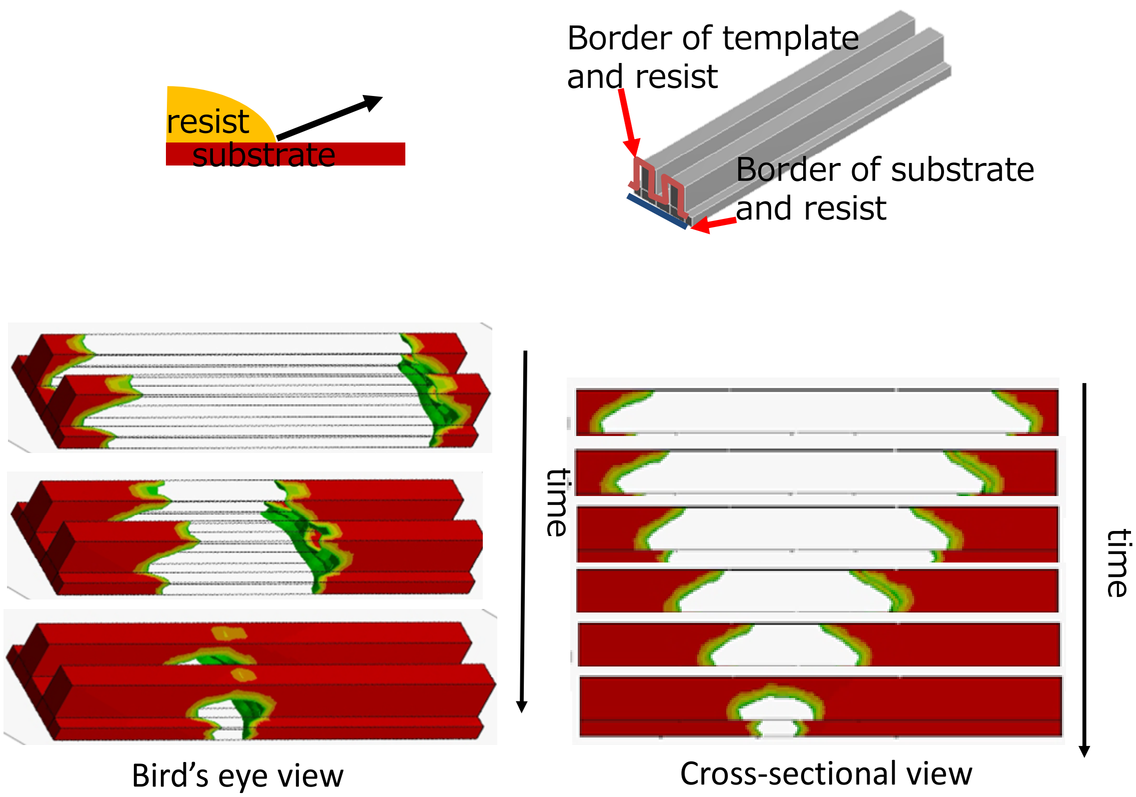

Figure 7: Simulation of bubble trap caused by resist flow.

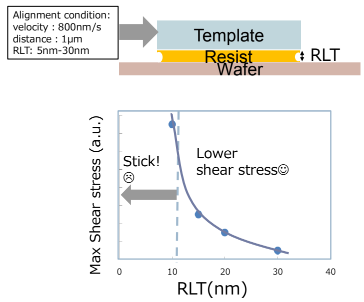

Figure 8: Result of RLT dependence on alignment shear stress.

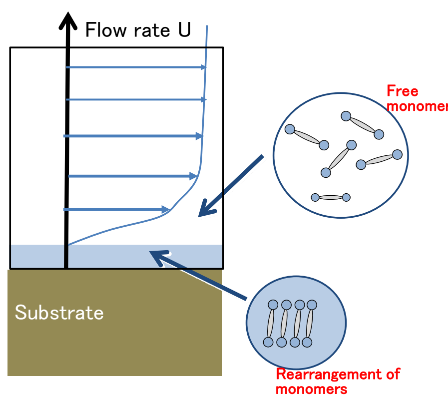

Figure 9: Schematic figure of the effect monomer molecular rearrangemen .

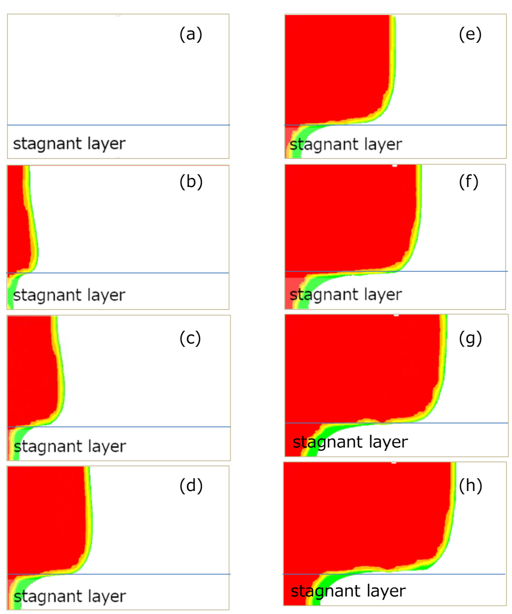

Figure 10: Pseudo resist flow simulation neighboring stagnant layer.