

# Defectivity and Particle Reduction For Mask Life Extension, and Imprint Mask Replication For High Volume Semiconductor Manufacturing

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## Abstract

Imprint lithography has been shown to be an effective technique for replication of nano-scale features. Jet and Flash\* Imprint Lithography (J-FIL\*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Criteria specific to any lithographic process for the semiconductor industry include overlay, throughput and defectivity. The purpose of this paper is to describe the technology advancements made in the reduction of particle adds in an imprint tool and introduce the new mask replication tool that will enable the fabrication of replica masks with added residual image placement errors suitable for memory devices with half pitches smaller than 15nm.

Hard particles on a wafer or mask create the possibility of creating a permanent defect on the mask that can impact device yield and mask life. By using material methods to reduce particle shedding and by introducing an air curtain system, test stand results demonstrate the potential for extending mask life to better than 1000 wafers. Additionally, a new replication tool, the FPA-1100 NR2 is introduced. Mask chuck flatness simulation results were also performed and demonstrate that residual image placement errors can be reduced to as little as 1nm.

\*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

**Keywords:** Jet and Flash Imprint Lithography, J-FIL, nanoimprint lithography, NIL, defectivity, particles, mask life

## 1. Introduction

Imprint lithography is an effective technique for replication of nano-scale features.<sup>1,2</sup> Jet and Flash Imprint Lithography\* (J-FIL\*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate.<sup>3-8</sup> The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. With respect to the imprint stepper, both CDU and line edge roughness meet the criteria of 2nm. A collaboration partner has achieved overlay of 10nm (with a target of 8nm)<sup>9</sup> and defect levels  $\sim 5/\text{cm}^2$  across a lot of 25 wafers.<sup>10</sup> Other criteria specific to any lithographic process include throughput, which plays a strong role in determining whether Cost of Ownership requirements can be met. Recently, Takeishi and Sreenivasan reported that a throughput of 40 wafers per hour was achieved on a four station imprint tool.<sup>11</sup>

On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. Semiconductor requirements dictate the need for a well-defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photomasks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was recently reported to have a defectivity of only 0.04/cm<sup>2</sup> as measured by a Lasertec tool with 50 nm sensitivity.<sup>12</sup> Presently, Ichimura et al. have exceeded the targets for both CDU and IP. In addition, master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20 nm have been fabricated.<sup>13</sup>

The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. In 2012, an MR-5000 mask replication tool was developed specifically to pattern replica masks from an e-beam written master. Previous work by Ichimura et al. using this tool, demonstrated that a CDU of less than 1.5nm 3σ can be achieved on both the master and replica masks.<sup>14</sup> In 2012, an MR-5000 mask replication tool was developed specifically to pattern 6" x 6" x 0.25" replica masks from an e-beam written master.

As the most aggressive features in advanced memory designs continue to shrink below 15 or 16 nm (towards 1Z nm), the cost of fabricating these devices increases because of the large number of additional deposition, etch and lithographic steps necessary when using immersion lithography.<sup>15</sup> Nanoimprint lithography (NIL) offers a more attractive Cost of Ownership (CoO) than competing technologies. Cost benefits can be realized by:

- Enabling direct printing of the features of interest, without the need for multiple patterning techniques.
- Improved mask life that allows a replica mask to be used for more than 1000 wafers.
- By improving the throughput of the NIL tool

The cost benefits are outlined in Figure 1, which describes CoO for a variety of lithographic methods. When compared to an immersion based Self Aligned Quadruple Patterning (SAQP), approach, CoO for NIL is reduced by approximately 40%.

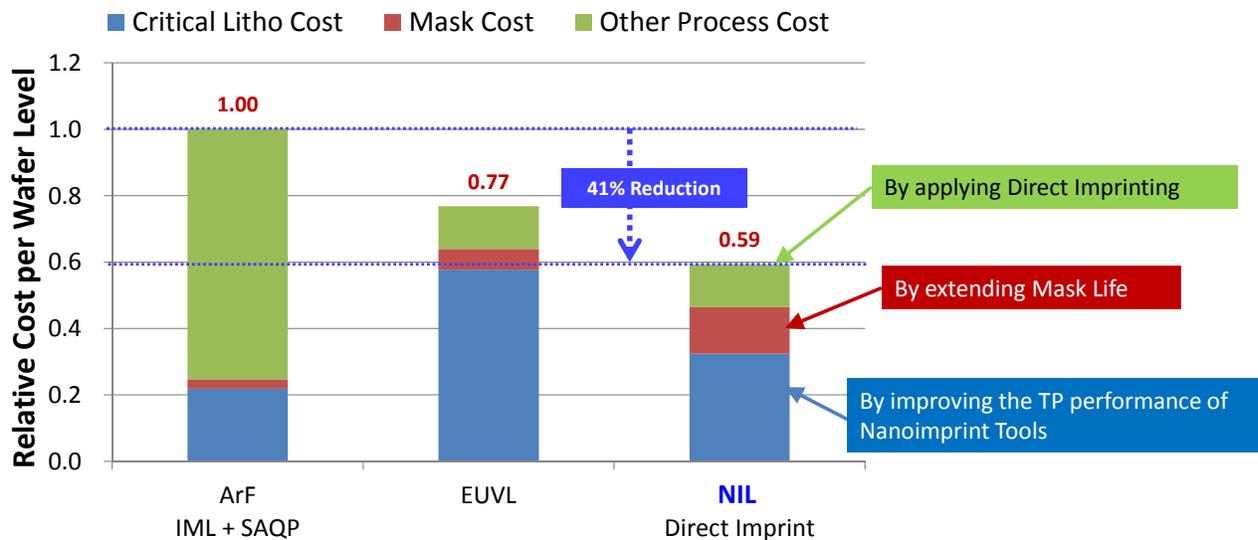


Figure 1. Cost of Ownership comparison for various lithographic processes.

It is important to recognize however that both the replica mask life and the mask specifications must be compatible with device manufacturing needs. With respect to Cost of Ownership (CoO), it is anticipated that the lifetime of a single replica imprint mask will need to be on the order of 10<sup>5</sup> imprints, or approximately 1000 wafers. And for devices with half pitches compatible with 1Z nm memory, the replica mask must also meet strict criteria in image placement in order to meet the overlay specifications of the device.

In this paper, we will focus on the extension of mask by reducing particle counts within the imprint tool and then discuss mask replications and the methods that will be applied to meeting image placement specifications on a replica mask.

## 2. Mask Life

Nanoimprint Lithography (NIL), like any lithographic approach requires that defect mechanisms be identified and eliminated in order to consistently yield a device. NIL does have defect mechanisms unique to the technology, and they include, liquid phase defects, solid phase defects and particle related defects.

Liquid phase defects can form as the result of contamination to the underlying adhesion layer. The result of this contamination is incomplete filling in a small area, and is typically referred to as a non-fill defect. This defect type has been addressed in the past by applying the same sort of environmental filtering systems required, for example, for chemically amplified resists.

Solid phase defects can occur during the separation process. Shear forces imparted between the mask and wafer can tear features and potentially leave resist on the imprint mask. Another consequence of shear forces is line collapse and can be observed when the aspect ratio of sub-20nm features starts to grow well beyond 2:1. These defect types have also been overcome by careful attention to system controls during separation and are also no longer considered a priority. Examples of liquid and solid phase defects are shown in Figures 2a and 2b, respectively.

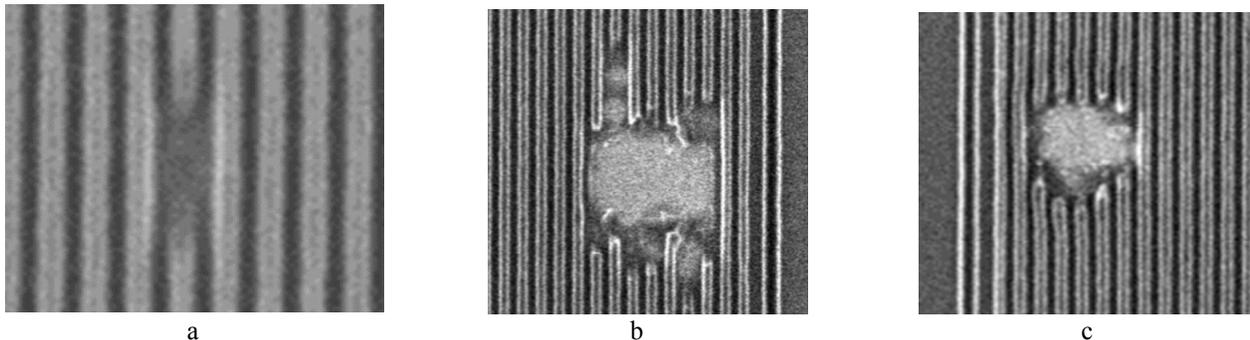


Figure 5. Major defect types of Nanoimprint Lithography: a) non-fill defect in liquid phase, b) Separation defect in solid phase, c) particle defect.

More troublesome are particles that reside and adhere to either the mask or wafer surface. In the past we have described how the inkjet system can add to particle count and how liquid in-line filtration systems addressed this issue.<sup>16</sup> These particle types were typically soft in nature and could be addressed by mask cleaning. Hard particles generated within the imprint tool are the biggest source of concern. Hard particles run the chance of creating a permanent defect in the mask, which cannot be corrected through a mask cleaning process. An example of a hard particle defect is shown in Figure 2c.

In summary,

- Liquid phase defects do not cause mask damage, do not require mask cleaning and can be addressed through environmental controls.
- Solid phase defects also do not damage the mask, but may require mask cleaning.
- Particles, break down into two categories: soft and hard. Soft defects rarely damage the mask. Hard particles, however impact mask life.

To put this point in perspective, consider that in order to meet the CoO specs in shown in Figure 1, the replica mask life must be sustained for better than 1000 wafers. If we conservatively assume that:

- Every hard particle adds a defect to the mask, and
- The mask defectivity limit from hard particles is 0.1 pieces per square centimeter,

then the number of particle adders per wafer pass must be  $< 0.001$ . As a result, if we are to achieve this particle specification, an aggressive strategy is needed to remove particles adders to the wafer and mask. There are several countermeasures for particles that can be taken. Included on the list are:

- The minimization of particle generation from particle sources related to materials within the tool and the surface treatment of these materials
- The reduction of particles that could potentially find their way onto the mask and wafer. These can be addressed by optimizing the airflow within the tool and by providing an ionizer source to address charge build up on the mask
- The elimination of particles through an inspection and mask cleaning process flow.

This last item adds cost to the imprint process however, and needs to be minimized. Therefore, we will discuss the means for treating surfaces and optimizing airflow within the tool. We will start first with a discussion on surface treatment.

### a) Material Surface Treatments

In general, lithography tool manufacturers rely on the use of ceramic materials to reduce particle generation. What isn't generally appreciated however, is that even ceramic materials continuously generate particles. As a result, several surface treatment methods have been developed to minimize particle generation. The upper left graph in Figure 3 shows an example of a ceramic that generates many particles over the course of several hours. By applying correct polishing, coating and heating methods, however, particle generation is significantly reduced. As an example, the graph on the bottom left shows particle generation after a special heating process. In this case, the relative particle generation is reduced to only 0.3% after the heat treatment. This type of strategy is applied for all relevant materials within the tool.

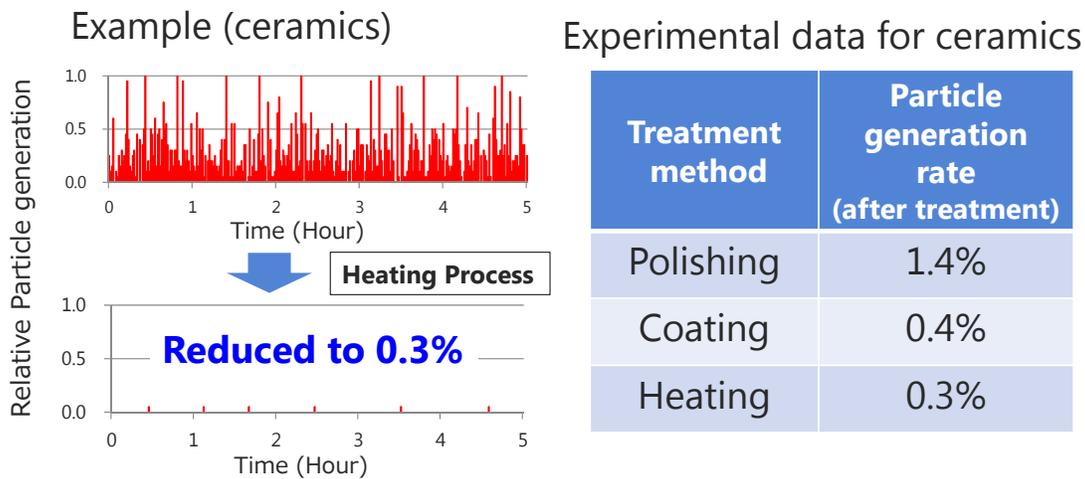


Figure 3. Surface treatment methods for ceramic based materials. Special heat treatment methods can be effective in reducing particle generation from these surfaces to 0.3%.

## b. Air Flow Optimization

A key point to be made is that that even when particles are shed, that they don't find their way to the mask and wafer surfaces. This is accomplished by applying air flow optimization methods to the tool, and in particular to the area of the mask and wafer. Figure 4 depicts a simulation of particles tracked in the wafer plane. Figure 4a shows a schematic of the tool. Incoming particles can initially be managed through the choice of material and material treatment, as well as ultrafine filtration systems. But these steps alone are not sufficient to meet defectivity goals, and additional measures must be adopted to further reduce particles near the wafer. Figure 4b shows a simulation of particles tracked within the tool. Note that particles located above the wafer are substantially reduced relative to the rest of the tool. How this is accomplished is discussed below.

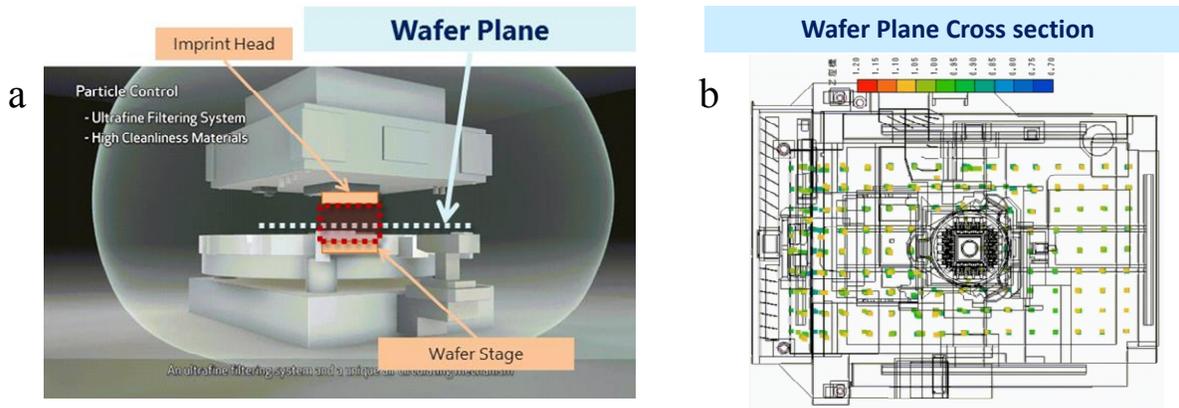


Figure 4. a) Schematic of the imprint tool. b) A simulation of particles tracked within the imprint tool

An environmental test stand was developed specifically to study particle control. This test stand is capable of adjusting the starting environment within the tool. An example of how the system operates is shown in Figure 5. Particle counts were performed at two unique particle settings. The graph below shows the difference between an ISO Class 7 environment, where almost ten to the seventh particles are generated within a cubic meter and an ISO Class 0 environment.

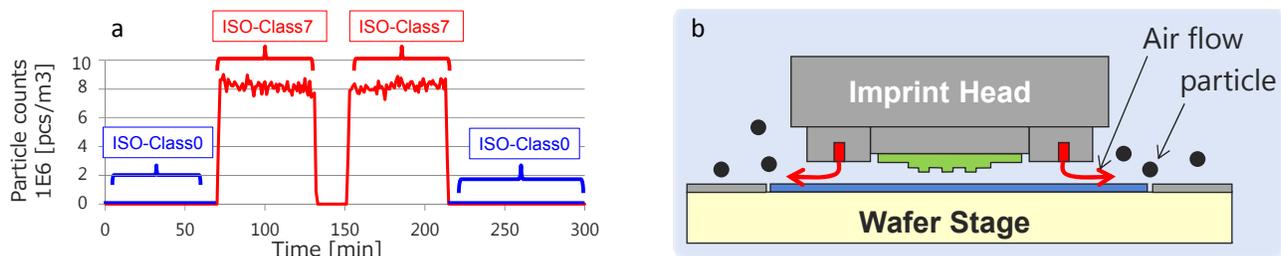


Figure 5. a) Environmental test stand operating at two different conditions: ISO Class 7 and ISO Class 0. b) Primary air curtain designed to reduce particulates at the plane of the mask and wafer.

To address particles at the wafer plane, a primary air curtain system was introduced into the test stand, as shown in the schematic image in Figure 5b. This air curtain has already been applied to our NIL tools. To predict the effects of an optimized air flow system, an accelerated experiment was performed by setting the test stand for ISO Class 7 conditions.

The accelerated test was done by:

- Moving the stage equivalent to a full wafer run, and

- Operating the air curtain system in an ISO Class 7 environment
- Measuring wafer particle counts,
- And then extrapolating the equivalent ISO Class 2 values that are applied to the NIL tool.

In this experiment, we operated the test stand under three different conditions:

1. Without any air curtain
2. With the primary curtain, and
3. With the primary air curtain, run with an optimized condition

As shown in Figure 6, without any curtain, almost 3000 particles are generated on the wafer, with an equivalent ISO Class 2 count of 0.03 pieces per wafer pass. By applying the air curtain, we can reduce this number to 0.006 pieces, and under optimal conditions we could not confirm the presence of particles on the wafer. Clearly, the air curtain operation was confirmed to have great potential for meeting the particle adder specification.

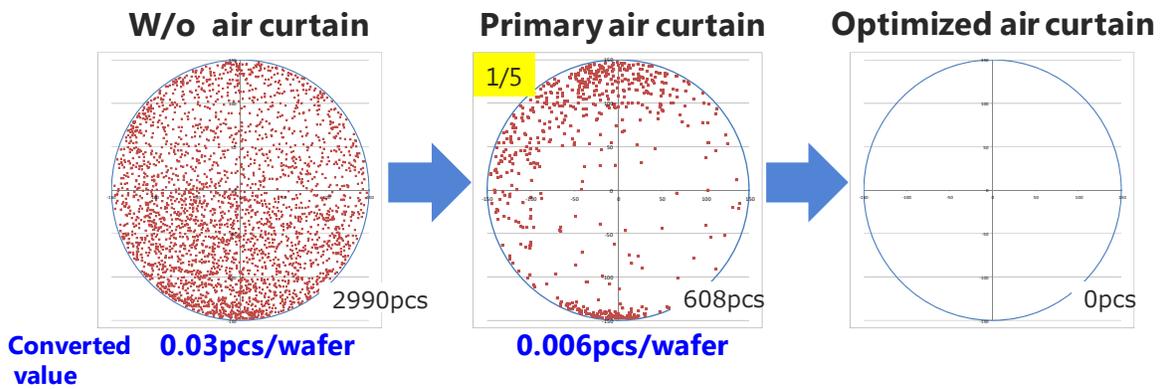


Figure 6. Particle adders per wafer based on three different operating conditions. An optimized air curtain is very effective in reducing particles at the wafer plane.

Figure 7 reviews particle adder history and provides a roadmap for the next two and a half years. Air flow control in the tool was established in 2014, and the air curtain system was introduced in the following year. We are now in the process of applying surface treatments to the materials within the tool. Over the next one and a half years, the air curtain will be optimized in order to meet or exceed the particle specification. With this approach, mask life can be prolonged to meet CoO targets, with a plan that provides 10X improvements each year for the next two years and meets the criteria for mask life > 1000 wafers.

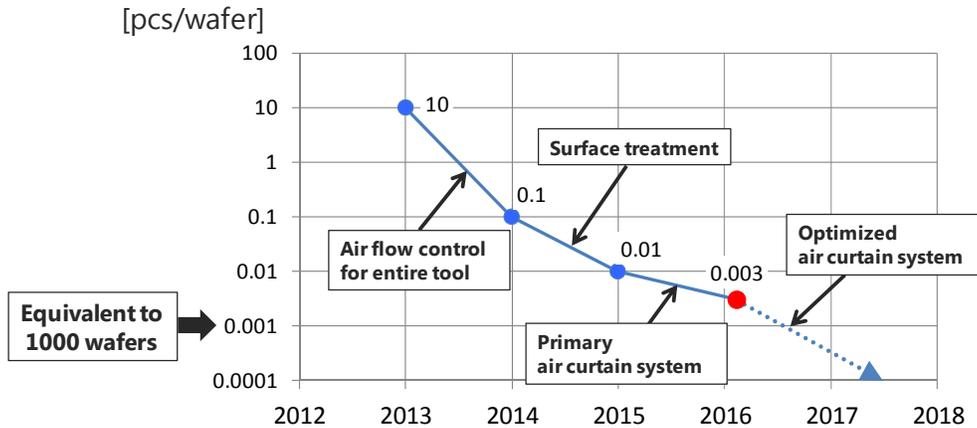


Figure 7. History and roadmap for particle reduction in the imprint tool.

#### 4. Mask Replication

The mask replication process requires good control for both the critical features and defectivity. Both of these criteria are the subject of previous papers.<sup>17,18</sup> Equally as important is the added image placement (IP) error induced during the replication process. Current image placement specifications for 1Z nm devices call for an added image placement error on the replica to be less than 1 nm. We are in the process of developing a new FPA-1100 NR2 mask replication tool which meets the target for the 1Z nm generation of devices. The tool leverages the high cost master mask to create any number of low cost replica masks that are used in the wafer tool. The current MR5000 model will give way in 2016 and 2017 to the NR2 tool. A schematic image of the tool is shown in Figure 8.



Figure 8. Schematic image of the FPA-1100 NR2 replication system.

To understand the current IP contribution to the replica mask, added image placement error was measured across 14 replica masks on the MR5000 tool. As shown in Figure 9a, the MR5000 typically adds, on average, just over three nanometers in y. By improving both imprint controls and separation controls, image placement performance can be improved to meet the 2X nm spec of 2.5nm.<sup>19</sup>

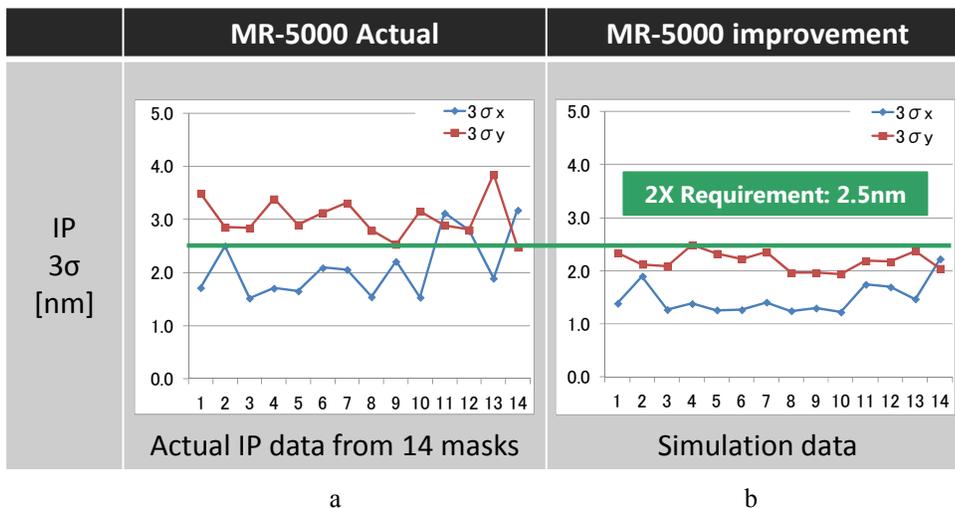


Figure 9. a) Residual image placement error from the MR-5000 replication tool. b) By improving system controls, this error can be reduced to meet 2X nm device specifications.

Meeting the residual image placement specification for 1Znm devices will require improvements in mask chuck flatness. Simulation results have confirmed that mask chuck flatness has a significant effect on added residual image placement. A chuck with peak to valley flatness of 120nm induces residual errors 1.5nm and 2.6nm, in x and y respectively (Figure 10a). By cutting the flatness down to 80nm, the error can be reduced to 1.2nm and 0.4nm (Figure 10b).

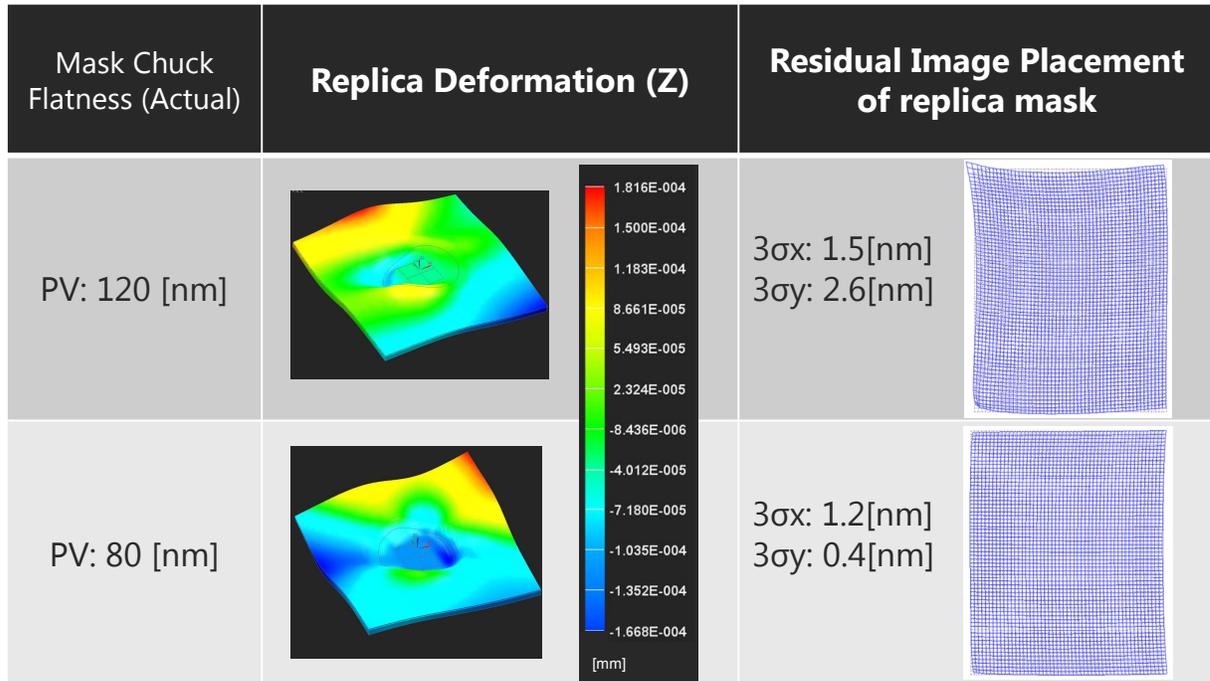


Figure 10. Simulations indicate that a mask chuck flatness of 80nm peak-to-valley will be required to meet the residual error specification in the NR2 replication system.

## Conclusions

Great progress has been made in the field of nanoimprint lithography over the last two years. Overlay of better than 5nm (mean + 3sigma) has been demonstrated, and throughputs are starting to approach the numbers required for high volume manufacturing. Defectivity has been reduced by more than two orders of magnitude and several imprint specific defect mechanisms have been identified and eliminated. The continued reduction of particle adders extends both the life of the master mask and the replica mask. In this work, methods for reducing particles generated from material surfaces was introduced, and an air curtain system was tested. In an optimized configuration in a test stand, the air curtain showed potential for enabling a replica mask life of greater than 1000 wafers. A new mask replication tool, the FPA-1100 NR2 was also introduced and the means for improving the residual image placement error in the tool to ~ 1 nm was presented. The combination of improved mask life and better image placement will be used to address advanced devices with half pitch dimensions less than 15nm for the memory markets.

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