Nanoimprint System Development and Status for High Volume Semiconductor Manufacturing

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Abstract

Imprint lithography has been shown to be an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography (J-FIL) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Criteria specific to any lithographic process for the semiconductor industry include overlay, throughput and defectivity. The purpose of this paper is to describe the technology advancements made and introduce the new imprint systems that will be applied for the fabrication of advanced devices such as NAND Flash memory and DRAM.

Overlay of better than 5nm (mean + 3sigma) has been demonstrated, and throughputs of 10 wafers per imprint station are now routinely achieved. Defectivity has been reduced by more than two orders of magnitude and particle adders within the tool have come down by approximately four orders of magnitude. A pilot line tool, the FPA-1100 NZ2, was used to generate most of the results in this work and conceptual plans are in place to address the requirements necessary for high volume manufacturing with an attractive cost of ownership relative to other HVM solutions for the semiconductor industry.

Keywords: Jet and Flash Imprint Lithography, J-FIL, overlay, throughput, defectivity, imprint lithography, nanoimprint lithography

1. Introduction

Imprint lithography is an effective technique for replication of nano-scale features.[1,2] Jet and Flash Imprint Lithography (J-FIL™) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate.[3-8] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6" x 6" x 0.25" fused silica was recently reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50 nm sensitivity.[9] Presently, Ichimura et al. have exceeded the targets for both CDU and IP. In addition, master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20 nm have been fabricated.[10]

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With respect to the imprint stepper, both CDU and line edge roughness meet the criteria of 2nm. A Collaboration partner has achieved overlay of 10nm (with a target of 8nm)[11] and defect levels ~ 5/cm^2 across a lot of 25 wafers.[12]

Other criteria specific to any lithographic process for the semiconductor industry include overlay, throughput and defectivity. In April of 2014, Canon Inc. completed the acquisition of the semiconductor business of Molecular Imprints Inc., and the company was renamed Canon Nanotechnologies, Inc. (CNT). CNT and Canon Inc. have been working closely to accelerate the development of imprint lithography and have combined the most important attributes of each company to bring the technology to a point where it can be applied for high volume manufacturing of semiconductor devices. CNT has focused on enhanced imprint module design, resist development for improved process performance and technology transfer to Canon Inc. Canon uses its expertise to design imprint production steppers by creating production infrastructure which includes resist production, collaborations with mask vendors, and close collaborations with the end user. This approach has resulted in the advancement of the three criteria mentioned above.

The purpose of this paper is to describe the technology advancements made and introduce the new imprint systems that will be applied for the fabrication of advanced devices such as NAND Flash memory and DRAM.

2. Experimental Details

To generate the test masks, patterns were exposed using a shaped beam pattern generator. A non-chemically amplified positive resist was chosen for mask patterning. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Replication of the mask was done using an MR5000 imprint replication system.[13]

The patterns chosen for evaluation of overlay, throughput and defectivity was a 26mm x 33mm mask consisting 2Xnm Flash-like device gate patterns and dummy fill die surrounding the device die. The mask also included peripheral structures such as align marks and metrology marks.

Imprinting was performed using a Canon FPA-1100 NZ2 system (See Section 4.). A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 300 mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the nanoimprint process have previously been reported.[14]

Defectivity was measured using KLA-Tencor wafer inspection tools. All inspections were performed in array mode.

3. Results

a. Overlay

Historically, overlay has been done using an Interferometric Moiré Alignment Technique.[15] This approach obtains real-time relative overlay errors between points on the imprint mask and the corresponding points on the wafer. The system is capable of measuring alignment errors at a single point well below 1nm. A magnification actuator system corrects for magnification and distortion between the mask and substrate, and works on the basis of imparting elastic deformations to fused silica over a small range of motion (typically on the order of a few ppm). The system incorporates an array of force feedback controlled actuators that are mounted around the imprint mask. This strategy allows in-plane corrections in X and Y, orthogonality, and to some extent higher order distortion corrections.[15]

Previous results have demonstrated mix and match overlay to a 193nm immersion scanner of approximately 10nm.[12] A newer "through the mask (TTM)" approach to alignment has been implemented to improve overlay. Figure 1 shows the measurement repeatability of a TTM system as a function of light intensity. With a sufficient signal, repeatability of better than 1 nm can clearly be achieved.

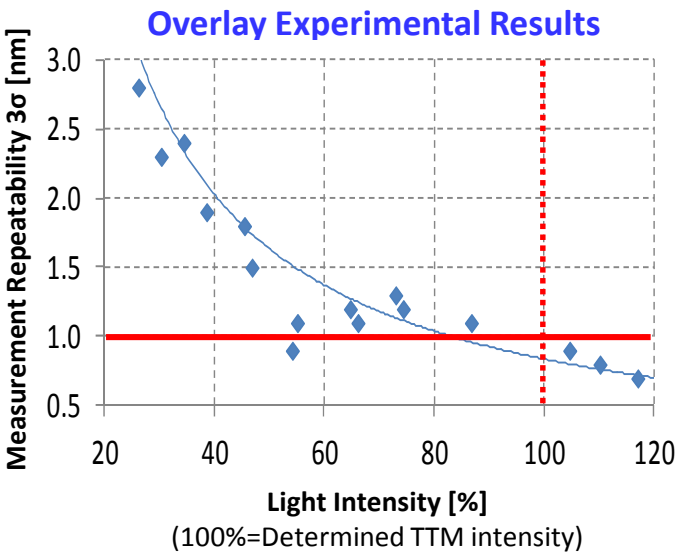

Figure 1. Measurement repeatability of a TTM overlay system as a function of light intensity.

When combined with better wafer flatness, enhanced wafer temperature control and reduced errors on the wafer have allowed overlay errors to be reduced to as little as 4.2nm in x and 4.8nm in y (mean + 3sigma), as shown in Figure 2. Overlay has improved by almost a factor of eight in only two years. Further improvements to both the mask and magnification actuator system are planned over the next two in order to meet demands of the semiconductor roadmap. It should be noted that all performance criteria (which includes overlay, throughput, defectivity and particle adders) are customer dependent.

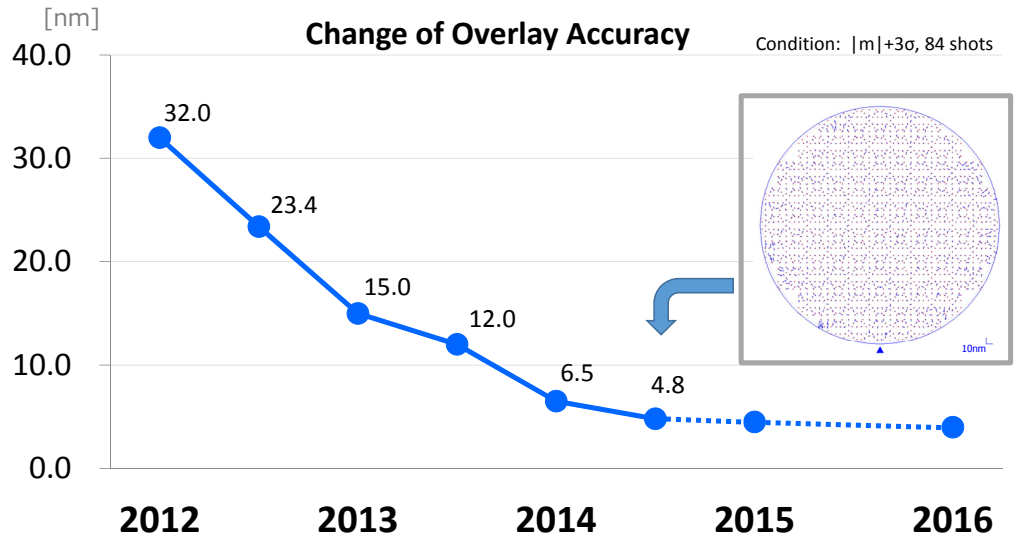

Figure 2. Overlay improvements made over the last two years.

b. Throughput

Non-fill defectivity must always be considered within the context of process throughput. An example of a non-fill defect located near an alignment mark is shown in Figure 3.[16] Processing steps such as resist exposure time and mask/wafer separation are well understood, and typical times for the steps are on the order of 0.10 to 0.20 seconds. To achieve a total process throughput of 20 wafers per hour (wph), it is necessary to complete the fluid fill step in 1.0 seconds, making it the key limiting step in an imprint process.

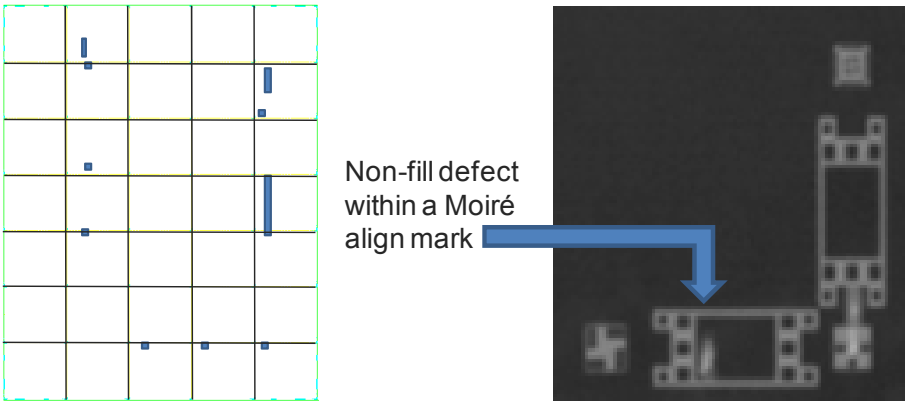

Figure 3. a) Field defect map showing the locations of non-fill defects using a fill time of 1.5 seconds. b) An example of a non-fill defect within a printed Moiré align mark.[16]

There are several parameters that can impact resist filling. Key parameters include resist drop volume (smaller is better), system controls (which address drop spreading after jetting), Design for Imprint or DFI (to accelerate drop spreading) and material engineering (to promote wetting between the resist and underlying adhesion layer). In addition, it is mandatory to maintain fast filling, even for edge field imprinting. Previously, we have demonstrated that it is feasible to fill a field in only one second.[17]

Currently, throughput specifications are typically limited by the ability to fill partial fields without the presence of non-fill defects. The issue is primarily a function of controlling resist spreading in smaller areas, where the process cannot begin at the center of the field. Partial fields with areas equivalent to at least 35% of the total area of a full field are generally quite manageable. An example of a fill sequence for a partial field is shown in Figure 4.

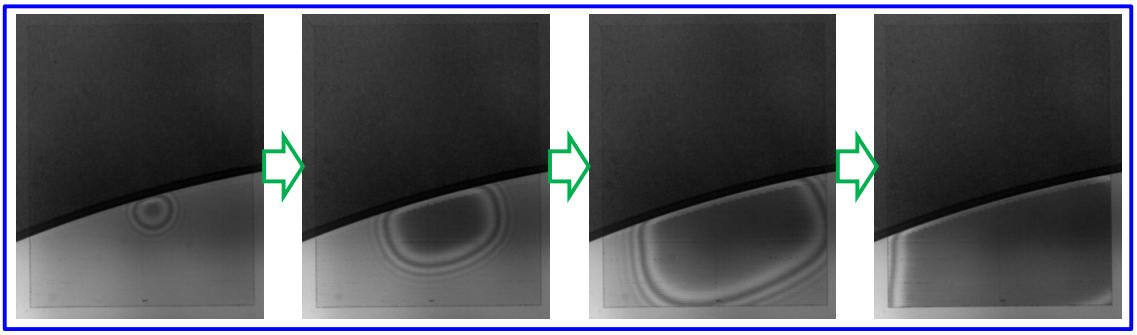

Figure 4. Filling characteristics of a partial field with a relative area of 52%.

As the relative area drops, non-fill defectivity for shorter fill times begins to rise, and an example of a field still containing detected non-fill defects is shown in Figure 5. In this example, non-fill defectivity in a field with a 22% area was 5.2/cm^2 after a fill time of two seconds. In general, a fill time of two seconds is sufficient for fields with areas greater than 25%.

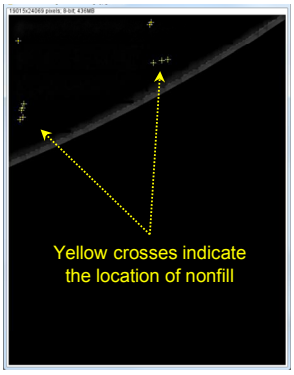

Figure 5. Non-fill defectivity in a partial field after a two second resist fill time.

It should be noted that the non-fill defectivity will continue to decrease as fill time is extended. This behavior is demonstrated in Figure 6. In this experiment, total defectivity was recorded on two wafers printed without partial fields (blue data points). The next two wafers included all partial fields and defectivity of the partial fields are denoted in red. No discernable pattern is observed between the two wafer sets, indicating that once filling is addressed, the printing of partial fields has no impact on overall defect levels. An example of a fully patterned wafer including edge fields is shown in Figure 7.

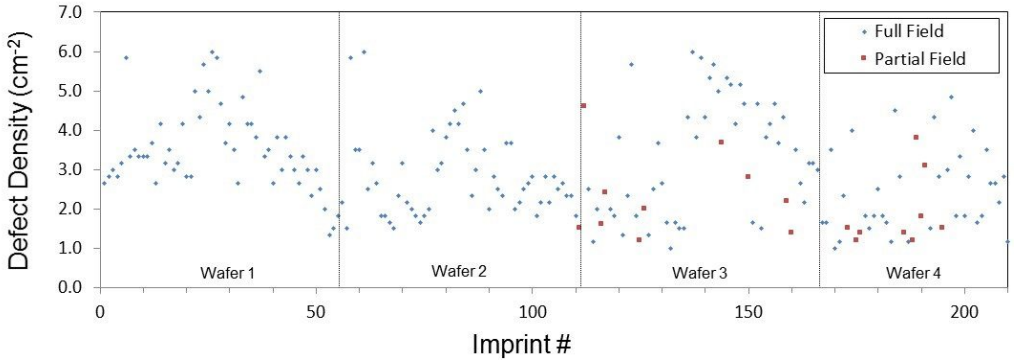

Figure 6. Defect density comparison between wafers printed with and without partial fields.

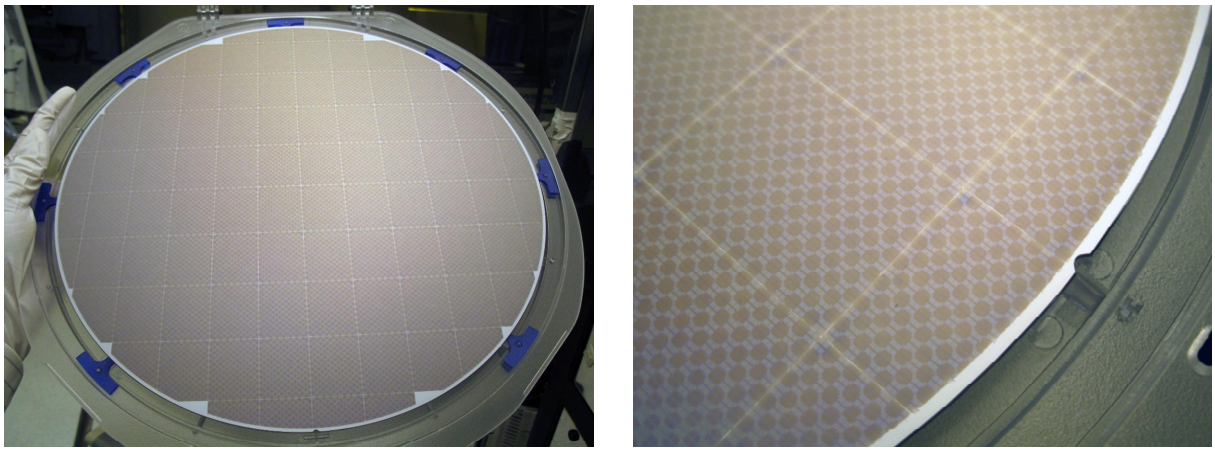

Figure 7. A fully imprinted wafer (left) and a close up of several imprinted edge fields (right).

The improvement in throughput performance over the last two years is shown in Figure 8. Performance has improved by greater than 5x in this timeframe. Note that throughput is defined as the throughput of a system consisting of four imprint stations. As an example, the current tool throughput of 40 wafers per hours denotes a system with an individual imprint station of 10 wafers per hour. Performance over the next two years is targeted to improve Cost of Ownership.

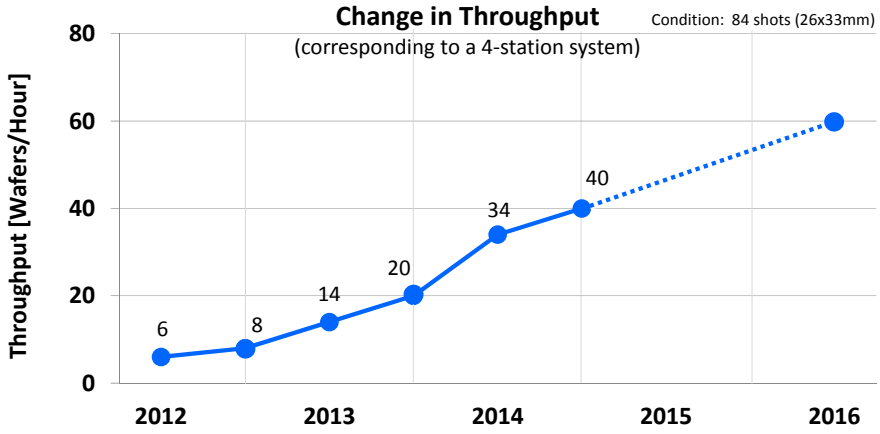

Figure 8. Throughput improvement over the last two years.

c. Defectivity

Device yield requires that certain defect density levels be achieved for a particular device. Because of the built in redundancy, NAND Flash memory is the first targeted device for nanoimprint lithography, with a requirement of approximately 1 defect/cm^2. DRAM devices are a logical second choice and typically require reductions in defectivity of about an order of magnitude relative to NAND Flash.

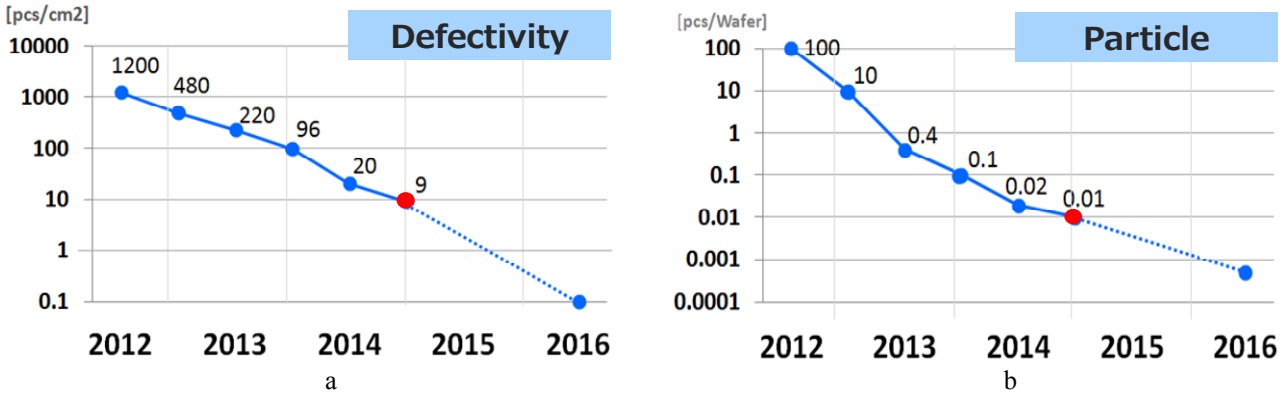

Figure 9. Defect density improvements over the last two years: a) Overall defect reduction as measured on a printed wafer, and b) particle adders per wafer in the imprint platform.

Figure 9 depicts the improvements in defectivity over the course of two years. Figure 9a shows the overall trend in defectivity, corresponding to a reduction in defects of greater than two orders of magnitude. As in any lithographic technology, there are multiple sources of defects. For imprint lithography, considerable efforts have been made to address filling and contamination defects while the resist is still in a liquid phase, shearing defects and contamination sources within the resist. Soft and hard particles have an impact on mask life, and Figure 9b describes the reduction in particle adders from the imprint tool. These results were achieved primarily by optimizing airflow within the imprint system and by reducing particle sources through the treatment of surfaces within the tool.

4. Imprint Systems

Most of the results shown in this manuscript were performed on a Canon FPA-1100 NZ2. The FPA-1100 NZ2 has

Figure 10. Canon FPA-1100 NZ2 single station wafer imprint system

a footprint smaller than an i-line tool, and has throughput and overlay specifications of 10 wafers per hour and 8nm, respectively. The system is suitable for pilot scale operation, device fabrication demonstration and process module development.

To address high volume manufacturing, a cluster approach will be used in order to meet throughput and cost of ownership requirements (CoO). A conceptual layout of a system containing four imprint stations is shown in Figure 11.

Figure 11. Conceptual drawing of a high volume nanoimprint system containing four imprint stations.

Clustering of modules is an approach that is widely adopted by the semiconductor industry and is extensively used for both deposition and etch systems. By clustering imprint stations, it is straightforward to meet throughput requirements that result in superior cost of ownership. As an example, a four station nanoimprint system with a throughput of 15 wafers per imprint station has a more attractive CoO than either ArF immersion multiple patterning

approaches or an EUVL system running at 125 wafers per hour. A basic model depicting CoO for each lithographic approach is shown in Figure 12.

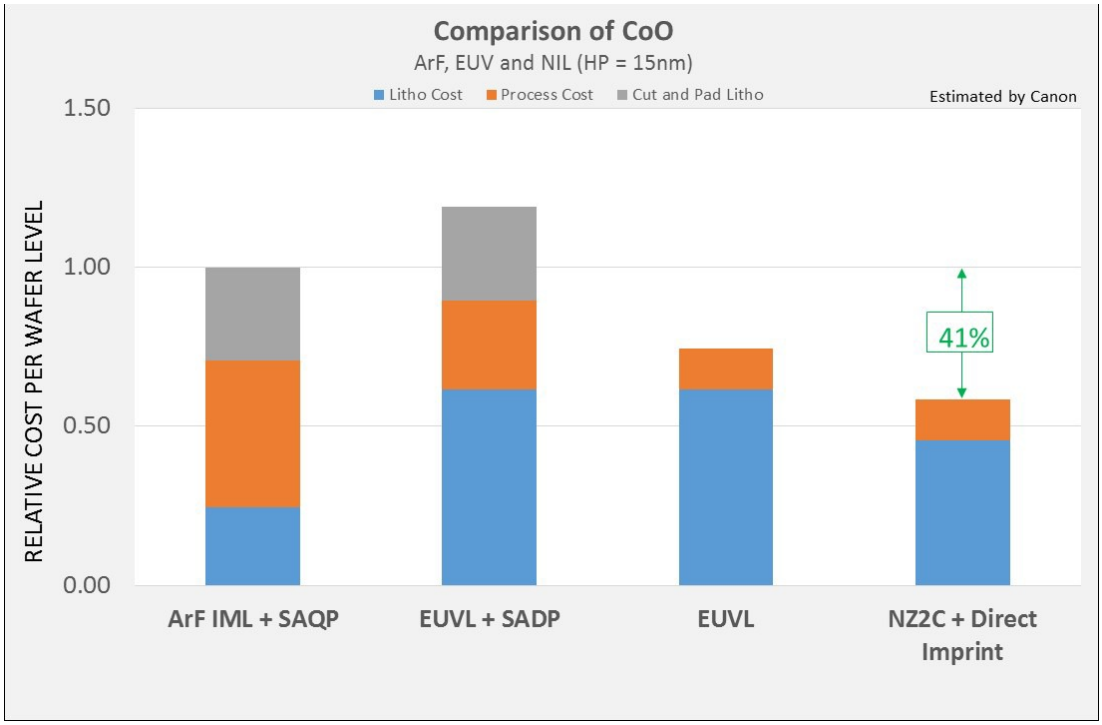

Figure 12. Cost of Ownership for different lithographic approaches. Nanoimprint lithography has reduces CoO relative to an ArF immersion SAQP process by approximately 41%.

Conclusions

Great progress has been made in the field of nanoimprint lithography over the last two years. Overlay of better than 5nm (mean + 3sigma) has been demonstrated, and throughputs of 10 wafers per imprint station are now routinely achieved. Defectivity has been reduced by more than two orders of magnitude and particle adders within the tool have come down by approximately four orders of magnitude. A pilot line tool, the FPA-1100 NZ2, was used to generate most of the results in this work and conceptual plans are in place to address the requirements necessary for high volume manufacturing with an attractive cost of ownership relative to other HVM solutions for the semiconductor industry. The technology will be introduced for non-volatile memory at first and then expanded to DRAM and logic applications

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