

Nano-imprint lithography edges toward sub-50-nm feature sizes for integrated circuits.

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# making an imprint

As chip-makers strive to reduce the feature sizes of integrated circuits, the need for next-generation lithography (NGL) tools increases. The escalating cost of these tools for conventional optical and extreme ultraviolet (EUV) lithography is driven in part by the need for complex optical sources and optics. The cost for a single NGL tool could exceed \$50 million in the next few years, a prohibitive figure for many companies. As a result, several researchers are looking at low-cost alternative methods for printing sub-100 nm features.

In the mid-1990s, several research groups started investigating different methods for imprinting small features. Imprint lithography is essentially a micro-molding process in which the topography of a template patterns the photoresist on a wafer; this contrasts with optical lithography, in which the resist is patterned by optical exposure and development. Imprint lithography does not use a reduction lens—

the size of the template determines the size of the pattern. One advantage of this approach is that the parameters that limit resolution in classic photolithography (including wavelength and numerical aperture) do not apply; investigations in the sub-50-nm regime by our group and others indicate that imprint lithography resolution is limited only by the resolution of the template fabrication process.

Many of these methods, although very effective at printing small features across an entire wafer, are limited in their ability to do precise overlay. In 1999, Willson and Sreenivasan developed step and flash imprint lithography (S-FIL), which uses low-viscosity, UV-curable silicone monomers to perform high-aspect-ratio, high-resolution imprinting at low pressures and room temperatures.<sup>1</sup> In this method, the planarized wafer is coated with a layer of photoresist, then with a layer of silicon-containing monomer (see figure 1). Pressing the optically transparent template

into the monomer physically patterns the material, and UV light shining through the template hardens the monomer into an etch barrier of varying thickness. After separation of template and wafer, a subsequent etch step removes the residual layer left between features, leaving a pattern of photoresist-protected areas and bare wafer. The patterned wafer is now ready for deposition, etch, or implantation.

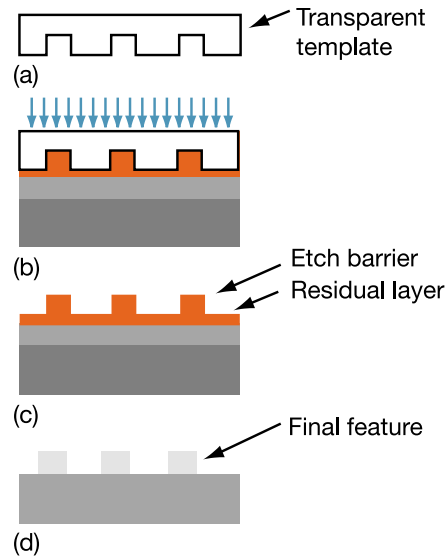
The quartz template used in S-FIL is transparent through the visible and most of the UV spectral regions, making it compatible not only with UV curing but also with optical alignment of the wafer and template. As a result, S-FIL appears to be the most suitable imprint technique for fulfilling the stringent requirements of silicon integrated circuit fabrication. We have made progress developing a tool, template, and resist for S-FIL and are studying defects and the ability to overlay different mask levels.

The first step-and-repeat system was built at the University of Texas at Austin by modifying a 248-nm stepper (Ultratech Stepper; San Jose, CA). Key system attributes include a micro-resolution z-stage that controls the imprint force; an automated x-y stage for step-and-repeat positioning; a pre-calibration stage that enables parallel alignment between the template and wafer; a fine-orientation flexure stage that provides highly accurate, automatic parallel alignment of the template and wafer; an exposure source to cure the etch barrier; and an automated fluid delivery system that accurately dispenses known amounts of the liquid etch barrier.

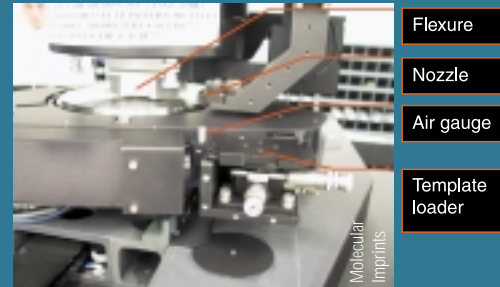
A commercialized version of an S-FIL tool (Molecular Imprints; Austin, TX) is designed to address the compound semiconductor and photonics markets, the devices of which require high-resolution features but are typically less sensitive to defects. These markets also operate at low wafer volumes and are hence more sensitive to cost, especially that of tools. The S-FIL tool is essentially a precise mechanical system with specialized fluid mechanics sub-systems and a mercury arc lamp exposure source, which limits cost (see figure 2). The resist delivery system incorporates a microsolenoid nozzle capable of dispensing drops of less than 5 nL. When integrated with a well-designed flexure stage and wafer chuck, the system yields a tool capable of printing an etch barrier with residual layers well under 100 nm. The system has achieved residual layers with a mean thickness of 85 nm, with a  $3\sigma$  variation of 20.

### template

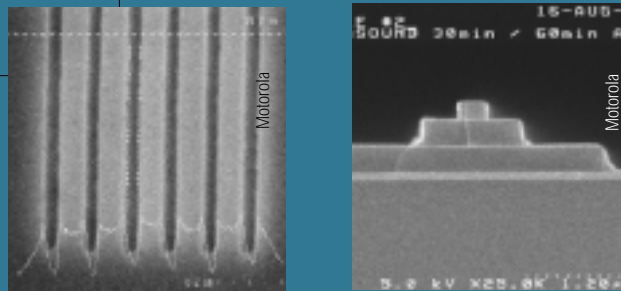
Early template fabrication schemes started with a  $6 \times 6 \times 0.25$ -in. conventional photomask plate and leveraged established chromium and phase-shift etch processes to define features in the glass substrate. Photoresist served as an etch barrier to pattern the chromium, which subsequently served as an etch barrier to pattern the glass. Although researchers have achieved sub-100-nm geometries, the etching process for the 80 to 100-nm-thick metal chromium layer com-



**Figure 1** In step and flash imprint lithography, a transparent template (a) is lowered onto a treated substrate and the gaps are filled with a low-viscosity UV-curable monomer (b). UV light shining through the substrate causes the monomer to convert into a hardened etch barrier. Upon removal of the template (c), the etch barrier covers the substrate in a pattern of thick barriers separated by a thin residual layer. One etch removes the residual layer to expose areas of treated substrate; a subsequent etch transfers the pattern to the substrate (d).



**Figure 2** Commercial nano-imprint tool designed for the compound semiconductor and photonics market incorporates a nozzle capable of dispensing drops of less than 5 nL.



**Figure 3** The resolution of printed features is limited by the resolution of the template. New methods create templates with features as small as 20 nm (left) or with multiple layer structures (right).

promises control of critical dimension (CD). These CD losses make the templates unsuitable for use with non-reduction lithography methods such as imprinting.

Two recent mask fabrication methods may provide alternatives.<sup>2</sup> The first method uses a much thinner (15 nm) layer of chromium as a hard mask. Thinner layers still suppress charging during the electron-beam patterning of the photoresist, while minimizing CD losses encountered during the pattern transfer. Once again, the process is to pattern the chromium, then use it to pattern the glass, after which the metal is removed. The drawback is that the final template lacks a conductive layer, which compromises SEM and defect inspection.

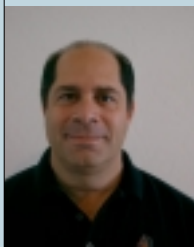
The second method deals with this issue by incorporating a conductive, optically transparent layer of indium tin oxide (ITO) on the glass substrate to suppress charging. In this process, a layer of oxide deposited over the ITO by plasma-enhanced chemical vapor deposition is covered with photoresist, then patterned. The template pattern appears in the oxide layer, and the ITO layer remains beneath to suppress charging during inspection.

Using these methods, we were able to create a template with 20-nm features (see figure 3 on page 19). Note that the methods described in this section can also be used sequentially to form multilayer structures on a template that can be used to fabricate devices such as T-gates or optical grating couplers.

silicon-containing etch barrier applied over an antireflective coating (also referred to as the transfer layer). The S-FIL process relies on photopolymerization of the resist, a low-viscosity acrylate-based solution. The current etch barrier liquid consists of four different components. A silylated monomer provides etch resistance for the oxygen transfer etch. Crosslinker monomers provide thermal stability to the cured etch barrier and also improve the cohesive strength of the etch barrier. Organic monomers serve as mass-persistent components and lower the viscosity of the etch barrier formulation. A photoinitiator dissociates to form radicals upon UV irradiation, and these radicals initiate polymerization.

The results include features as small as 20 nm (see figure 4). The profiles closely replicate the relief image in the template for both single- and multitiered structures. Critical dimension uniformity studies demonstrate little variance in the CD caused by the printing process.

Prior to etching the underlying transfer layer, it is necessary to remove the thin (about 100 nm) residual etch barrier material that remains between the features intentionally etch-protected. Because the silicon content of the etch barrier material is at least 12%, a combination of best selectivity between the etch barrier and the transfer layer is achieved by using a combination of carbon tetrafluoride and oxygen. Once the transfer layer is exposed, the gas chemistry for the reactive ion etch consists of oxygen alone.



### resist

The resist stack for wafer patterning typically consists of a

### defects and overlay

To ensure damage-free release of the template from the patterned wafer, a low-surface-energy, self-assembled monolayer is applied to the template prior to printing. To

## sports to semiconductors, Resnick pushes the envelope

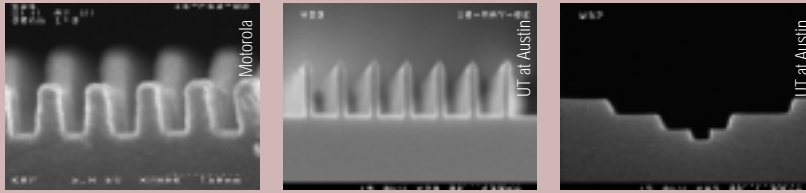
**D**eveloping new technologies for next-generation lithography tools is a hard road, filled with successes and setbacks—not unlike the world of sports. In both cases, mistakes can lead to victories and practice makes perfect.

For Motorola's Doug Resnick, sports and physics have gone hand in hand since his days at Plainview High School in Long Island, NY, when a family friend, teacher, and coach captured the young man's imagination by illustrating the principles of physics on the tennis court. Determined to prove that jocks and science can mix, Resnick played baseball as an undergraduate at the State University of New York (Binghamton, NY), eventually winning an Eastern Conference Athletic League scholarship for his efforts on and off the field. That scholarship carried Resnick to a doctorate in physics at Ohio State University (Columbus, OH), and by 1981, to the virtually

exploding world of microlithography research. During the next nine years at AT&T Bell Laboratories (Murray Hill, NJ), Resnick would go on to work on most of the major next-generation lithography technologies, including e-beam, x-ray, and extreme ultraviolet.

A few decades later, the baseball diamond has been replaced by golf courses in the Arizona desert; chasing baseballs supplanted by chasing children; and yet, little has changed. Like sports, developing next-generation lithography tools requires experience, knowledge, and the determination to keep trying. "When you start a new program like imprint lithography, you get to borrow from the success, problems, and lessons from others, and that's helping us up the learning curve quickly," says Resnick.

And when something does not work, there's always the baseball bat. —Winn Hardin



**Figure 4** Features printed using the S-FIL process include 30-nm lines printed in the etch barrier (a), 40-nm lines after etch (b), and a three-tiered structure (c).

understand whether defects accumulate during the imprint process, Stephen Johnson and others conducted a study of imprinted wafers on a KLA-Tencor 2139 wafer inspection tool. Initial inspection of 96 consecutive imprints showed relatively high levels of detected defects, but no significant upward trend in defects over time.<sup>3</sup> Additional studies will be necessary to fully characterize defectivity issues.

In order to overlay different mask levels, the system must include precision alignment capabilities, corrected for distortion errors such as magnification and orthogonality. The current alignment method leverages the transparent template to align marks on both the wafer and template. The presence of a low-viscosity liquid in the gap between the template and substrate allows lubricated nano-resolution, stiction-free alignment adjustments immediately prior to UV exposure. Early experiments with off-the-shelf optics and low-resolution gratings indicate that sub-100-nm alignment moves can be achieved. We believe that this can be readily extended to obtain sub-25-nm alignment corrections.

The real challenge, then, is to be able to correct for distortion between the template and wafer. To date, modeling and preliminary experiments suggest that the use of a template with a thickness substantially larger than the depth of the etched features allows for magnification corrections that are independent of the features etched into the template. Also, very uniform strain fields can be obtained by mechanical means. Experimental verification of these magnification systems as part of a complete imprinting step-and-repeat tool still remains to be done.

Nanoimprint lithography has come a long way in a very short period of time.

Tools, templates, and resists already available will be used to answer the open issues such as defectivity and overlay. If these issues can be solved, the last consideration then becomes the supporting infrastructure. Reduction lithography has been in the mainstream now for over 20 years, so the ability to write, inspect, and correct a 1X template will need to be developed. Still, the semiconductor industry has a history of rising to challenges, and S-FIL seems the best imprinting option for meeting the stringent requirements of future generations of silicon-based circuitry. **oe**

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