## Full field imprinting of sub-40 nm patterns

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## Abstract

Imprint lithography has been included on the ITRS Lithography Roadmap at the 32, 22 and 16 nm nodes. Step and Flash Imprint Lithography (S-FIL ®) is a unique patterning method that has been designed from the beginning to enable precise overlay to enable multilevel device fabrication. A photocurable low viscosity resist is dispensed dropwise to match the pattern density requirements of the device, thus enabling patterning with a uniform residual layer thickness across a field and across multiple wafers. Further, S-FIL provides sub-50 nm feature resolution without the significant expense of multi-element projection optics or advanced illumination sources. However, since the technology is 1X, it is critical to address the infrastructure associated with the fabrication of imprint masks (templates).

For sub-32 nm device manufacturing, one of the major technical challenges remains the fabrication of full-field 1x imprint masks with commercially viable write times. Recent progress in the writing of sub-40 nm patterns using commercial variable shape e-beam tools and non-chemically amplified resists has demonstrated a very promising route to realizing these objectives, and in doing so, has considerably strengthened imprint lithography as a competitive manufacturing technology for the sub-32nm node. Here we report the first imprinting results from sub-40 nm full-field patterns, using Samsung's current flash memory production device design. The fabrication of the imprint mask and the resulting critical dimension control and uniformity are discussed, along with image placement results. The imprinting results are described in terms of CD uniformity, etch results, and overlay.

# Keywords: S-FIL, imprint mask, imprint lithography, full field, overlay, pattern transfer, NAND Flash

### 1. Introduction

Small feature imprint lithography has existed for several years. The original technique involved the use of a patterned mold which is impressed onto a thermo plastic material and, with the combination of heat and pressure, the pattern in the mold was transferred to the substrate. Recently the technique has been significantly improved with the development of Step and Flash Imprint Lithography (S-FIL ®).<sup>1</sup> This technique involves the deposition of a low viscosity imprint resist on the substrate, lowering an imprint mask into the fluid which then flows into the patterns of the mask. Following this fill step, the imprint resist is exposed to UV light to cross-link it and convert it into a solid, and the imprint mask is removed leaving the solid pattern on the substrate.<sup>2</sup> The advantages of this process make it uniquely capable for CMOS applications.

Critical to the success of the technology is the commercial availability of 1X imprint masks. Recently, there have been several publications addressing the fabrication of imprint masks with 32nm and sub-32nm half pitch dimensions using high resolution Gaussian beam pattern generators.<sup>3,4</sup> Examples of features imprinted with these imprint masks are shown in Figure 1. Several commercial mask shops now accept orders for 1X imprint masks made by Gaussian beam tools. Currently, these systems are proving useful for unit process development and device prototyping purposes.

For sub-32nm device manufacturing, one of the major technical challenges remains the fabrication of full-field 1x imprint masks with commercially viable write times. Recent progress in the writing of sub-40 nm patterns using commercial variable shape e-beam tools and non-chemically amplified resists has demonstrated a very promising route to realizing these objectives, and in doing so, has considerably strengthened imprint lithography as a competitive manufacturing technology for the sub 32nm node. Here we report the first imprinting results from sub-40 nm full-field patterns, using Samsung's current flash memory production device design. The fabrication of the imprint mask and the

Emerging Lithographic Technologies XII, edited by Frank M. Schellenberg Proc. of SPIE Vol. 6921, 692107, (2008) · 0277-786X/08/\$18 · doi: 10.1117/12.775115 resulting critical dimension control and uniformity are discussed, along with image placement results. The imprinting results are described in terms of CD uniformity, etch results, and overlay.



Figure 1. High resolution imprints generated from imprint masks written with a Gaussian beam pattern generator. Pictured are 22nm, 28nm, and 32nm dense lines, 32nm Metal-1 and Logic test patterns, and 25nm half pitch contacts.

## **2. Experimental Details**

To generate the imprint mask, patterns were exposed by Dai Nippon Printing using a 50 keV variable shaped beam pattern generator. ZEP520A resist was chosen as the positive imaging resist. After development, the chromium and fused silica were etched using  $Cl_2/O_2$  and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process, followed by a dice and polish step were employed to create a finished 65 mm x 65 mm imprint mask.<sup>5</sup>

The pattern chosen for evaluation was a 38nm half pitch full field NAND Flash gate layer. The patterned area consisted of repeating core, a repeating periphery and non-repeating test chips. The approximate device size was 18 mm x 30 mm. Key elements of the repeating core are the dense 38nm lines and the transition regions to larger pitches at right angles to the primary pattern. This is best illustrated in the lower right hand corner of Figure 2. The write time for the imprint mask was approximately 10 hours.

Imprinting of the imprint mask pattern was performed by using a Molecular Imprints Imprio 250 tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 300 mm silicon wafer. The imprint mask was then lowered into liquid-contact with the substrate, displacing the resist and filling the imprint field. UV irradiation through the backside of the imprint mask cured the acrylate resist. The process was then repeated to completely populate the silicon substrate. Details of the imprint process have previously been reported.<sup>6</sup>

CD and LWR measurements on the imprinted patterns were performed in two different ways. In the first case, high resolution SEM images were taken with a JEOL JSM-6340F field emission cold cathode SEM, equipped with a tungsten emitter. The accelerating voltage of the tool can be varied from 0.5 to 30 kV. The system has intrinsic 1.2 nm resolution capability at 15 kV accelerating voltage, and 2.5nm at 1 kV.

Critical dimension (CD), line width roughness, and line edge roughness (LER) data were extracted offline from SEM images using the SIMAGIS<sup>®</sup> automated image metrology software suite from Smart Imaging Technologies.<sup>7</sup> For the analysis of within wafer uniformity and wafer-to-wafer uniformity, an AMAT NanoSEM was used to collect information on CD, LWR and LER. The beam accelerating voltage was 500V. The length of a line scan was 1 µm, and 512 scans were performed.



Figure 2. Key elements of gate layer, including the dense 38nm lines and the transition regions to larger pitches at right angles to the primary pattern

## 3. Results

#### a. Imprint mask Fabrication and Characterization

The imprint mask was written using a high resolution ZEP520A resist process. A multipass writing strategy was employed to compensate for the low resist sensitivity. It is important to note that the write times were still reasonable ( $\sim 10$  hours) when compared with a 4x photomask counterpart. This an expected result, due primarily to the reduced writing area and no requirement for optical proximity correction (OPC) in the case of imprint masks. Previously published results on two different 32 nm patterns have demonstrated a reduction in write time (relative to a 4x photomask) of 1.2x to 3x.<sup>8</sup>

A brief analysis of the imprint mask was done after the fused silica etch, but before the chromium was stripped. Pattern fidelity is illustrated in Figure 3. The 38 nm half pitch lines are well resolved. The spaces measure 33.1 nm and the  $3\sigma$  variation for five locations was 2.2 nm. The line width roughness measurements on the imprint mask ranged from 3.9nm to 5.1 nm,  $3\sigma$ . It should also be noted that, although no pattern optimization was performed in the non-repeating test areas, several of the test patterns were resolved below 38 nm. Pictured in Figure 4 are line space pairs at 32 nm and 35 nm, respectively.

A set of nine metrology marks were also included in the pattern, in order to determine image placement. An LMS IPRO II metrology system was used to read the nine marks. The 3 sigma image placement variation from this data in x and y, was extremely low: 1.6 nm and 2.6 nm, respectively.



Figure 3. Primary pattern of the 38nm NAND Flash Gate layer. The 38 nm half pitch lines are well resolved and the right angle transition regions are characterized by good fidelity in the corner areas.



Figure 4. 35nm and 32nm half pitch features in the imprint mask.

## **b.** Imprint Results

The imprint mask was used to imprint the device layer on 300 mm wafers. The resulting imprints are shown in Figure 5. Figure 5a depicts a low magnification SEM image of the gate layer. All patterns were clearly resolved, including both the 38 nm half pitch lines and the right angle transition regions. Figure 5b shows a larger magnification of the same region. 30 degree tilted views show the resolution of both regions described above. The 38nm lines have a profile close to 90 degrees, and there is very little line width roughness observed. A SIMAGIS calculation of the features in Figure 5c yields a CD of 39.6nm and LWR of only 3.7 nm,  $3\sigma$ . Figure 5d depicts a magnified view of the well defined corner regions. SIMAGIS software was also used to measure in field CD uniformity. Eighteen locations were measured in the core area. Each location used eleven lines to determine CD. As a result a total of 198 lines were measured. The mean CD was 41.9 nm with a three sigma variation of 2.13 nm. LWR was 3.56 nm,  $3\sigma$ .



Figure 5. Imprinted 32 nm half pitch lines are resolved over an electron beam exposure dose range of nearly 20 percent.



Figure 6. In order to determine field-to-field and wafer-to-wafer variations, 18 measurements were made within a field, at three field locations, across a four wafer set. CDU, LWR and LER are noted in the box at the bottom right.



Figure 7. 32nm Metal-1 and 32nm half pitch lines

Field-to-field and wafer-to-wafer CD uniformity was measured using an AMAT CD SEM. Nine measurements were made per repeating device core, for a total count of 18 measurements per field. Three fields were measured per wafer across a four wafer set (See Figure 6). The field-field  $3\sigma$  variation was only 3.17 nm and corresponding wafer-to-wafer variation was only 0.37 nm. The average LWR and LER values were 3.76 nm and 2.39 nm, respectively.

Image resolution was further explored by examination of the non-repeating test areas. Shown in Figure 7 are Metal-1 and dense lines resolved at 32nm.

#### c. Overlay Results

All imprint tools for CMOS applications must be designed to mix-and-match with existing 193nm optical lithography tools. The Imprio-250 uses a field-by-field alignment system.<sup>9</sup> This method does not add to the imprint time since the alignment occurs during the time that the fluid is filling the imprint mask features. Since the imprint mask and substrate are in close proximity (<10 $\mu$ m) during the alignment process, it is practical to capture the relative positioning error between two matching alignment marks using a Moiré image based technique<sup>9,10</sup>

Magnification correction is achieved by mechanically compressing the imprint mask. Positive magnification can be achieved by writing the imprint mask 5ppm oversize and releasing the compression. In this way +/- ~4ppm magnification can be obtained. Since the distortion is this small, well within the elastic regime of the material, it is perfectly reversible. A multi-point forcing mechanism was developed<sup>(19)</sup> that can induce optimized vectors of correction forces along the periphery of the imprint mask.

The efficacy of the alignment and magnification control systems were tested by performing a mix and match test. The 38 nm NAND Flash gate level was overlayed to a zero level applied with a scanner, covered by a representative etch layer stack used by SEC. By performing a send ahead measurements and inserting an offset, a mean plus 3 sigma overlay of 34 nm in x and 21 nm in y was achieved. The data set, picturing overlay results accumulated in 30 fields is displayed in Figure 8. A second send ahead wafer yielded values of 28 nm in x and 27 nm in y. The major sources of the error are thought to be from thermal distortions, placement errors on the imprint mask and image field distortions from the 193nm scanner. Further improvements are expected to reduce the overlay errors down to less than 10 nm.

	X (mm)	Y (mm)	MagX (ppm)	MagY ()	ppm) Theta(	mrad) Skew(mr	ad)											
F1 Overlay:	0.000012	0.000004	1.0000005 1.0	000004	-0.000300	-0.0000002												
F3 Overlay:	0.000015	0.000005	1.0000005 1.0	000001	-0.000664	-0.0000005												
F5 Overlay:	0.000012	0.000013	1.0000004 1.0	000004	-0.000323	-0.0000002		Wafer Y			/							
F7 Overlay:	0.000015	0.000002	1.0000004 1.0	000003	-0.000286	-0.0000001		*		/		407	400	405				
F9 Overlay:	0.000013	0.000003	1.0000004 1.0	000004	-0.000305	-0.0000001						107	106	105				
F11 Overlay:	0.000012	-0.000000	1.0000004 0.	99999999	-0.000449	9 -0.0000003			/		100	101	102	103	104		$\mathbf{i}$	
F13 Overlay:	0.000015	0.000007	1.0000002 1.	0000002	-0.000429	9 -0.0000003				~~	00		00	0.5		00		
F15 Overlay:	0.000013	0.000005	5 1.0000005 1.	0000003	-0.000279	0 -0.0000003				99	98	97	96	95	94	93		
F17 Overlay:	0.000009	0.000001	1.0000002 1.	0000004	-0.000155	5 -0.0000005				86	87	88	89	90	91	92	``	
F19 Overlay:	0.000006	-0.000004	1.0000003 1.	0000001	-0.000047	-0.0000002												$\setminus$
F21 Overlay:	0.000010	-0.000002	1.0000002 1.	0000003	-0.000480	-0.0000002			/ 85	84	83	82	81	80	79	78	77	
F23 Overlay:	0.000009	0.000002	1.0000000 1.	0000001	-0.000226				68	69	70	71	72	73	74	75	76	
F25 Overlay:	0.000014	0.000003	1.0000004 1.	0000006	-0.000397	-0.0000003				00	10	* •	12	10		15	10	
F20 Overlay.	0.000007	-0.000001	1.00000000 1.	0000004	-0.000173			- 1/	67	66	65	64	63	62	61	60	59	
F31 Overlay:	0.000003	0.000000	1.0000003 1.	0000000	-0.000310	-0.0000003			50	51	52	53	54	55	56	57	58	
F33 Overlay:	0.000003	-0.000002	1.00000002 1.	0000000	-0.000364	0.0000001		1	50	51	32	33	54	55	50	57	50	
F35 Overlay:	0.000009	-0.000003	1.0000004 1.	0000000	-0.000393	-0.0000002			49	48	47	46	45	44	43	42	41	
F37 Overlay:	0.000005	-0.000001	. 1.0000003 1.	0000002	-0.000312	-0.0000001			22	22	24	25	26	27	20	20	40	
F39 Overlay:	0.000012	0.000001	1.0000004 1.	0000000	-0.000561	-0.0000002			1 32	33	34	33	30	31	30	39	40	
F41 Overlay:	0.000008	-0.000000	1.0000003 0.	9999998	-0.000197	0.0000000			\ 31	30	29	28	27	26	25	24	23	
F43 Overlay:	0.000007	-0.000000	1.0000003 0.	9999999	-0.000451	-0.0000003				40	47	40	40	20	24	22		
F45 Overlay:	0.000002	-0.000009	1.0000001 0.	9999997	-0.000254	ŧ −0.0000002				10	17	18	19	20	<u>Z1</u>	22		·
F47 Overlay:	0.000007	-0.000001	. 1.0000003 1.	0000000	-0.000334	-0.0000001				15	14	13	12	11	10	9		
F49 Overlay:	-0.000007	0.000001	. 1.0000001 1.	0000004	-0.000110	) -0.0000001						-		-	0	-	'/	
F51 Overlay:	-0.000003	0.000003	1.0000001 1.	0000002	0.000014	ŧ −0.0000000					4	5	6	1	8			
F53 Overlay:	0.000004	-0.000005	1.0000005 0.	99999996	-0.000218	3 -0.0000003						3	2	1				
F55 Overlay:	0.000002	-0.000005	5 1.0000004 0.	99999997	-0.000407	-0.0000001						<u> </u>	-	•				
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159 Overlay:	-0.000000	-0.000007	0.9999995 0.	9999992	0.000098	0.000001											~ 1101	
Overall Resu	lts																	
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Raw 3Sig (mm	): +0.0000	26 +0.000	021			00	rrec	cted										
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Figure 8. Mix-and-match overlay results. The left hand image shows the print layout of the gate layer for a 300 mm wafer. The mean plus 3 sigma values in x and y were 34 nm and 21 nm, respectively.

#### d. Etch Results

Etch properties of the imprint resist were determined using a test imprint mask consisting of arrays of dense lines with half pitches ranging from 32 nm to 44 nm. The imprinted features are shown in Figure 9a. The feature profiles are nearly vertical, and the residual layer thickness is less than 15 nm. Pattern transfer consisted of a descum step to remove the thin residual layer, a hardmask etch, etch of an thick organic resist and finally, an etch into the pattern transfer layer. Figures 9b and 9c show the final result. Cross section images are depicted in Figure 9b. CD is maintained, and aspect ratios of greater than 4:1 were easily achieved. Top down SEMs (Figure 9c) show minimal line width roughness. Measured values of LWR ranged from only 1.8 nm to 2.6 nm,  $3\sigma$ .



Figure 9. Pattern transfer process for dense features. a) Imprinted lines b) Cross section images after etch c) Top down images after etch. The final LWR ranged from only 1.8 nm to 2.6 nm,  $3\sigma$ .

## 4. Conclusion

Previous results in fabricating imprint masks using variable shape beam generators were limited in resolution, primarily through the use of fast chemically amplified resists. By applying a high resolution ZEP520A resist process, a 38 nm half pitch NAND Flash gate level imprint mask was successfully fabricated in write times that are industrially acceptable. Resolution, CD uniformity, and image placement were excellent across the full field. The imprint mask was then used to imprint the device layer on 300 mm wafers using an Imprio 250 from Molecular Imprints. The pattern quality was excellent, and test features down to 32 nm half pitch were resolved. Mix-and-Match tests demonstrated overlay better than 30 nm, mean+3 sigma. Further reductions in overlay errors can be achieved by better control of thermal budgets and reductions in image placement and lens distortions. Pattern transfer experiments clearly resolved high aspect ration 32 nm half pitch lines with minimal line width roughness. Continued work on improving overlay, defects, and throughput will lead to a decision regarding this technology's use for prototyping devices and in a mix-and-match strategy with optical lithography.

## Acknowledgments

The authors would like to thank Masaaki Kurihara, Shiho Sasaki, Nobuhito Toyama and Naoya Hayashi from Dai Nippon Printing for their excellent imprint mask fabrication work.

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