Toward 22 nm for unit process development using step and flash imprint lithography

Gerard M. Schmid, Ecron Thompson, Nick Stacey, Douglas J. Resnick,
Molecular Imprints, Inc., 1807C West Braker Lane, Austin TX 78758, USA
Deirdre L. Olynick, Erik H. Anderson
Lawrence Berkeley National Laboratory, 1 Cyclotron Rd, Berkeley CA 94720

Abstract

Imprint lithography has been included on the ITRS Lithography Roadmap at the 32 and 22 nm nodes. Step and Flash Imprint Lithography (S-FIL[TM]) is a unique method that has been designed from the beginning to enable precise overlay for creating multilevel devices. A photocurable low viscosity monomer is dispensed dropwise to meet the pattern density requirements of the device, thus enabling imprint patterning with a uniform residual layer across a field and across entire wafers. Further, S-FIL provides sub-100 nm feature resolution without the significant expense of multi-element, high quality projection optics or advanced illumination sources. However, since the technology is 1X, it is critical to address the infrastructure associated with the fabrication of templates.

This paper addresses steps required to achieve resolution at or below 32 nm. Gaussian beam writers are now installed in mask shops and are being used to fabricate S-FIL templates. Although the throughput of these systems is low, they can nevertheless be applied towards applications such as unit process development and device prototyping.

Resolution improvements were achieved by optimizing the ZEP520A resolution and exposure latitude. Key to the fabrication process was the introduction of thinner resist films and data biasing of the critical features. By employing a resist thickness of 70 nm and by negatively biasing features as much as 18 nm, 28 nm half-pitch imprints were obtained. Further processing improvements, including a high resolution lift-off method, show promise for achieving 20 nm half pitch features on a template.

Keywords: S-FIL, template, imprint lithography, 22 nm

1. Introduction

Over the last thirty years, many different varieties of Next Generation Lithographies (NGLs) have been posed as successors to optical lithography. Examples include proximity x-ray lithography, ion beam lithography (both 1X and projection), and variants of projection electron lithography (such as SCALPEL and PREVAIL)[1-4]. Research targeted towards making these technologies viable for high density silicon manufacturing has all but stopped for the cases mentioned above. The reason for the discontinuation of funding for each case had very little to do with resolution. Each technology was clearly capable of resolving 100 nm features and had the potential to resolve geometries much smaller than 100 nm. Instead, the continued extension of optical lithography combined with the lack of a commercial mask infrastructure made it extremely difficult for any of these technologies to penetrate the silicon market.

Imprint lithography has been included on the ITRS Lithography Roadmap at the 32 and 22 nm nodes[5]. This technology has been shown to be an effective method for replication of nanometer-scale structures from a template mold. As a high fidelity replication process, the resolution of imprint lithography is determined by the ability to create a master template having the required dimensions. It is therefore possible to reduce the dimensions of the imprinted features without developing new optical systems or photoresist materials – ingredients which limit the extendibility and cost effectiveness of projection photolithography. When the imprint material is a photocurable liquid, it is possible to perform the imprint process at ambient temperature and pressure, which enables accurate overlay and reduces process defectivity. With this combination of capabilities, imprint lithography is a multi-node technique that is suitable for advanced prototyping of processes and devices to meet the anticipated needs of the semiconductor industry.

Step and Flash Imprint Lithography (S-FIL™) operates in a step-and-repeat fashion: the processes of deposition of imprint material, imprint, alignment, photocuring and release all occur sequentially as each die on a wafer is patterned. S-FIL utilizes UV-curable liquids that are dispensed in a drop-wise fashion to meet the local pattern density requirements of the template structures, thus enabling imprint patterning with a uniform residual layer. After the imprint liquid has been dispensed on the wafer, the template is brought into close proximity with the wafer and capillary forces cause the imprint material to fill the template topography.[6] Alignment is performed through the transparent template while the template and wafer are in lubricated contact. UV exposure solidifies the imprint material, and the template is then removed from the patterned die. S-FIL has demonstrated sub-20nm resolution and sub-10nm overlay capability, with uniform residual layer across a field and across a wafer.[7,8]

With S-FIL patterning, properties such as critical dimension (CD), CD uniformity, and feature sidewall angle are effectively transferred from the template. Template characteristics are also critical to maintaining low process defectivity and accurate overlay. It is therefore critical to address the infrastructure associated with the fabrication of templates. A key benefit of S-FIL is the great similarity between the processes for manufacturing and characterizing S-FIL templates and modern photomasks. S-FIL makes use of fused silica templates that can be fabricated with the same patterning and etch transfer processes that are used for manufacturing chromeless phase-shifting photomasks. The standard form factor for an S-FIL template is a 65mm x 65mm x 6.35 mm section which is diced from a standard six inch photomask. Although patterning at 1X dimensions is challenging, it should be appreciated that today's 4X optical proximity correction (OPC) designs require features as small as 1.5X. Writing time is also an advantage at 1X, because of the reduced writing area and the elimination of OPC.

Several commercial mask houses now accept orders for S-FIL templates, which are generally patterned using electron beam pattern generators. Such pattern generators exist in both variable-shape beam (VSB)[9] and Gaussian-beam (GB) configurations.[8] VSB tools have been designed for commercial photomask manufacturing and are capable of high throughput and accurate pattern placement. By comparison, GB tools have been mainly used by research-oriented organizations. GB pattern generators are much slower than VSB tools, but they offer a significant improvement in resolution; isolated sub-10nm structures are commonly achieved.[10] This high-resolution capability is of increasing commercial value, which is simultaneously driving both improvements in tool performance as well as placement of these tools in commercial photomask shops.

Although 50 kV VSB tools are responsible for the majority of high resolution writing in the mask shops today, the best results achieved on an imprint template are limited to a half pitch of 50 nm.[11] Since imprint lithography first appears on the ITRS roadmap at 32 nm, resolution approaching 22 nm must be demonstrated. GB writers are now installed in mask shops and are being used to fabricate templates. Although the throughput of these systems is low, they can nevertheless be applied for applications such as unit process development and device prototyping. The purpose of this work is to optimize the processing of electron beam resists in order to provide the most latitude for 32 nm half pitch features and beyond.

2. Experimental Details

To generate the template, patterns were exposed using a Vistec VB6 100 kV Gaussian beam writer. ZEP520A resist was chosen as the positive imaging resist. HSQ was used as a negative resist. After development, the chromium and fused silica were etched (courtesy of Dai Nippon Printing) using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process, followed by a dice and polish step were employed to create a finished 65 mm x 65 mm template.[12] The template process flow is depicted in Figure 1.

Imprinting of the template pattern was performed by using a Molecular Imprints Imprio 250 imprint tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 200 mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process have previously been reported.[13]

CD measurements and micrographs of electron beam resists were taken with a LEO 1560 Schottky field emission SEM. CD measurements and micrographs of the imprinted resist were taken with a JEOL JSM-6340F field emission cold cathode SEM equipped with a tungsten emitter. The accelerating voltage can be varied from 0.5 to 30 kV. The system has intrinsic 1.2 nm resolution capability at 15 kV accelerating voltage, and 2.5nm at 1 kV. Critical dimensions

are measured manually, by placing markers at the edges of the feature of interest (See, for example, Figures 2a and 2b.). Because the measurement process is manual, the repeatability of the CD-SEM is > 10 nm (3σ) for line measurements.
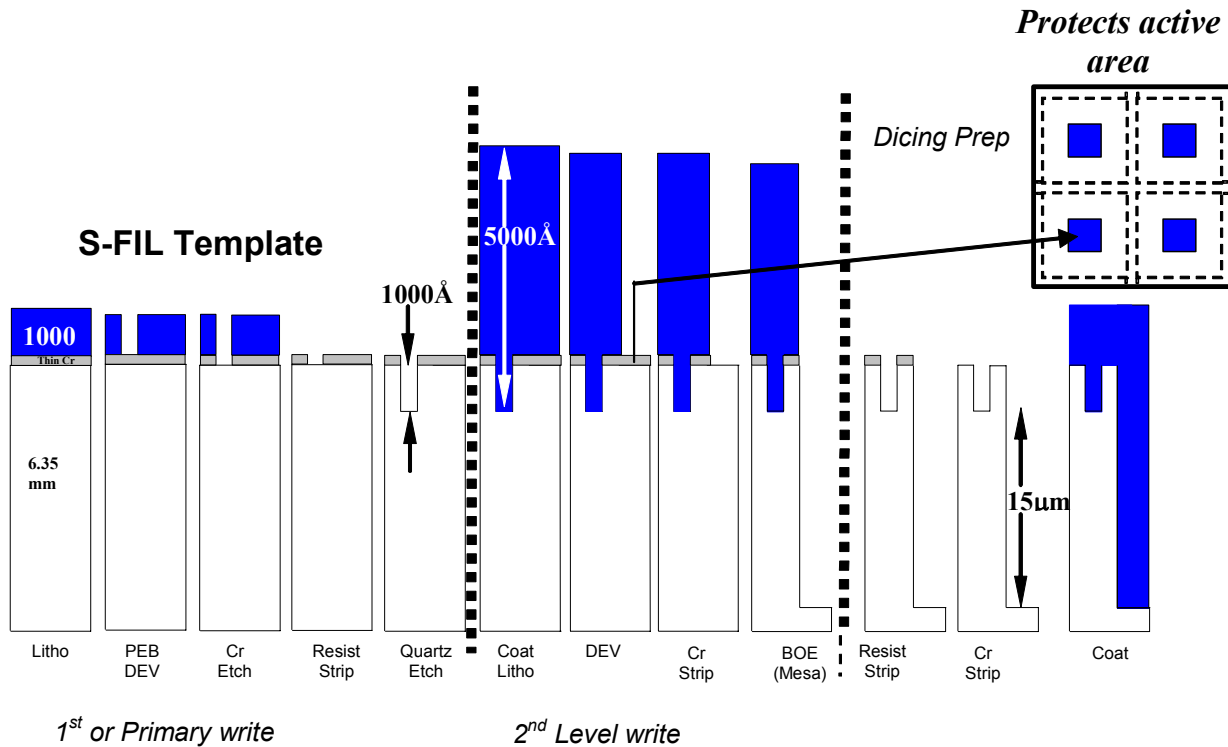

Figure 1. Template fabrication flow, including both the steps necessary to define both the high resolution patterns and the mesa area.

3. Results

a. 32 nm: Resist Processing

Previous work has demonstrated resolution on templates with half pitch dimensions of 35 – 40 nm.[14] An example of this work is depicted in Figure 2. The templates used to create these imprints were fabricated starting with 100 nm of ZEP520A resist and 15 nm of chromium.
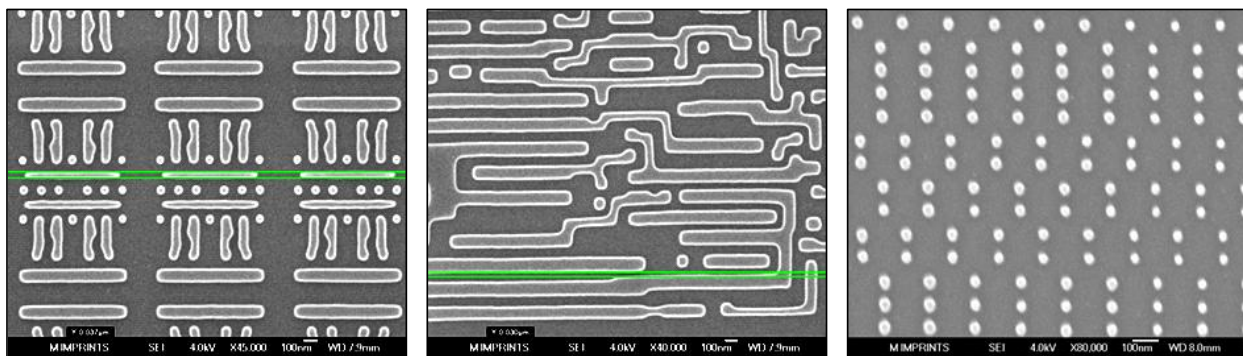
Figure 2. 35 and 40 nm half pitch imprinted features previously resolved using 100 nm of ZEP520A electron beam resist and 15 nm of chromium on a template.

To improve resolution, four steps were taken: 1) ultrasonic development of ZEP520A, 2) continued thinning of both the resist and chromium to minimize forward scattering and avoid line collapse, 3) applying proximity correction during exposure, and 4) applying a negative bias to all features in order to enhance exposure latitude. Typical patterns studies included dense lines, Metal 1 patterns, and Logic patterns.

To improve resolution to 32 nm, while still creating a 100 nm relief image in the template, the ZEP520A resist and chromium were thinned to 70 nm and 10 nm, respectively. Four developers, including two xylene mixtures, amyl acetate and hexyl acetate were evaluated. The typical develop time was 60 seconds in an ultrasonic bath. A rinse using isopropyl alcohol followed the develop process. The results of the develop test are shown in the response curves depicted in Figure 3a. Xylene based development improves resist sensitivity, but at a cost of contrast. Contrast ranged from 3.0 for xylenes up to 5.6 for hexyl acetate. Contrast for both amyl acetate and hexyl acetate were similar, and since the resist is more sensitive using amyl acetate, all subsequent testing was done using amyl acetate.

Exposure latitude was evaluated using a 40 nm half-pitch grating and three different feature biases: 0 nm (unbiased), -10 nm, and -20 nm. The results are shown in Figure 3b. Biasing the critical 40 nm feature by -20 nm results in an increase in exposure dose of approximately 2.5, however the exposure latitude improves by more than a factor of four. This is not surprising, because the control of the critical feature is determined primarily by the Gaussian beam tail.
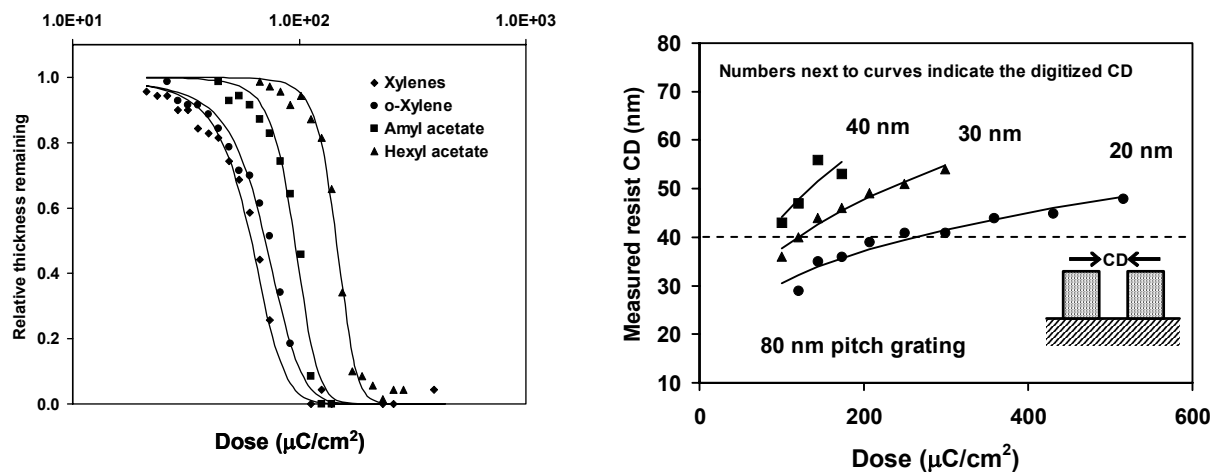
Figure 3. a) response curves for tow xylene mixtures, amyl acetate and hexyl acetate. The best combination of contrast and sensitivity is achieved with an amyl acetate developer. b) ZEP520A electron beam resist exposure latitude as a function of feature bias. The best latitude is achieved with larger negative biasing.

Given the success of the exposure latitude test, dense lines, Metal 1 patterns, and Logic patterns were then exposed in a 70 nm thick ZEP520A film with biases ranging from 0 to − 18 nm. Critical dimensions ranged from 26 to 40 nm. Again, the best latitude and cleanest lithography was obtained with the largest feature biases. The results are depicted in Figure 4. Shown are 28 nm half pitch lines exposed with a -18 nm bias, and 28 nm Metal 1 and Logic patterns exposed with a 16.8 nm bias. All features in each pattern are well resolved.
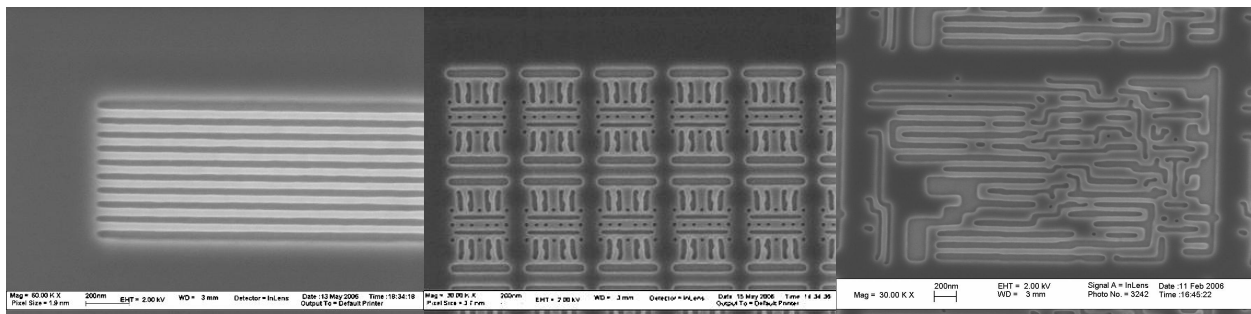
Figure 4. 28 nm resolution achieved in 70 nm of ZEP520A.

b. Template Fabrication and Imprint Results

Following resist development, plates were pattern transferred, cut into templates and imprinted on an Imprio 250. Shown in Figure 5 are two sets of 32 nm half pitch lines (patterned with a -18 nm data bias) at two magnifications. The difference in electron beam exposure dose used to define these features was approximately 20%. The difference in feature size over this range in exposure is only 5 nm. The marked improvement in electron beam exposure latitude is carried over through template pattern transfer and imprint, as shown in Figure 6. The resist data again shows the improvement in latitude resulting from a -20 nm feature bias. Also plotted is the latitude after imprint for 40 nm lines at 0 nm and -18 nm biases, and 32 nm half pitch lines exposed with a -18 nm bias. There is a small shift in critical dimension after pattern transfer and imprint. More importantly, however, the exposure latitude is comparable for all cases.
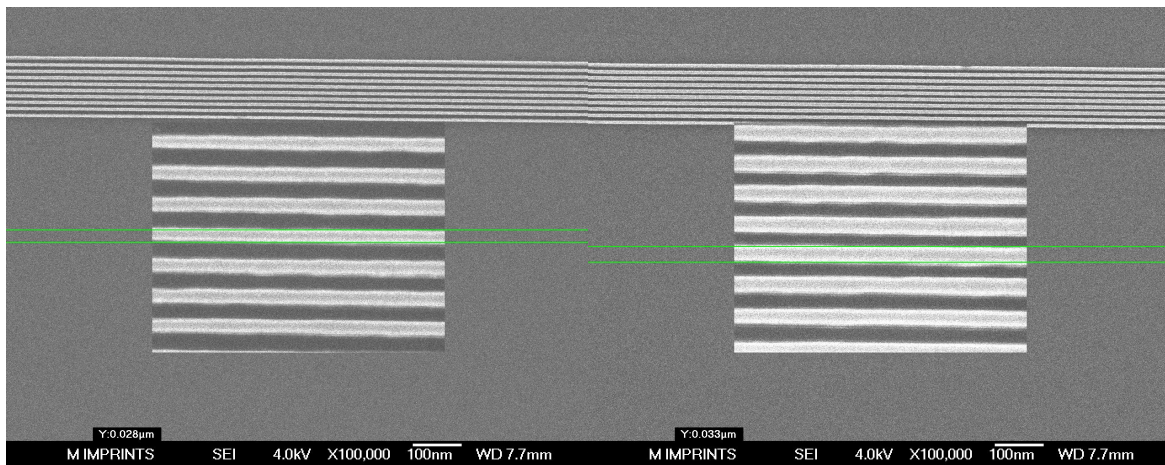

Figure 5. Imprinted 32 nm half pitch lines are resolved over an electron beam exposure dose range of nearly 20 percent.
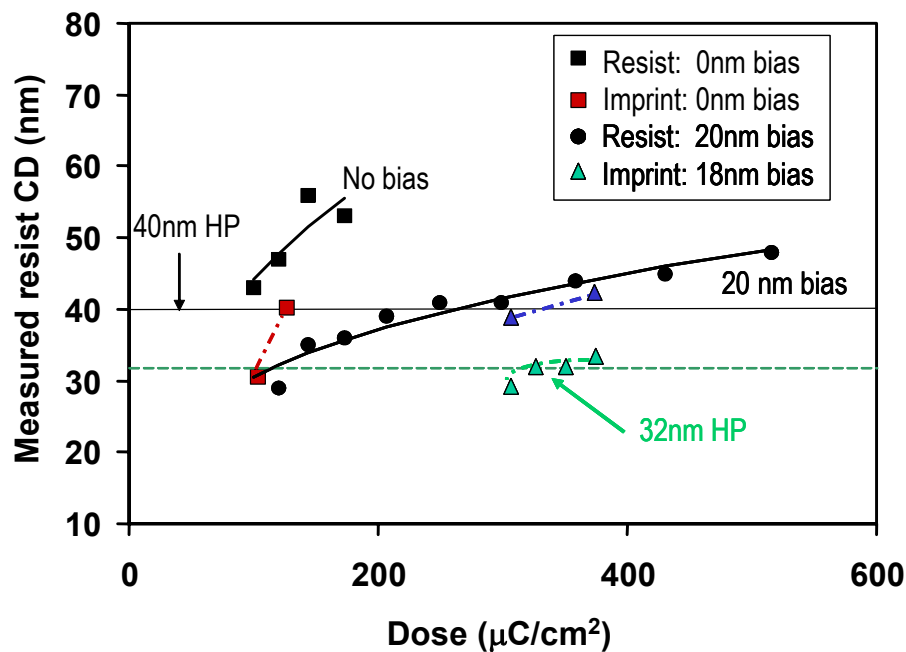

Figure 6. A comparison of exposure latitude after electron beam exposure and after imprinting. Latitude is maintained throughout the entire fabrication process.

The 28 nm half-pitch lines and Metal 1 patterns were successfully resolved on the template and the imprinted wafers, and examples are shown in Figure 7. A cross section of the 28 nm lines is shown in Figure 7b. Wall profile for all of the imprinted patterns was 87 – 88 degrees.
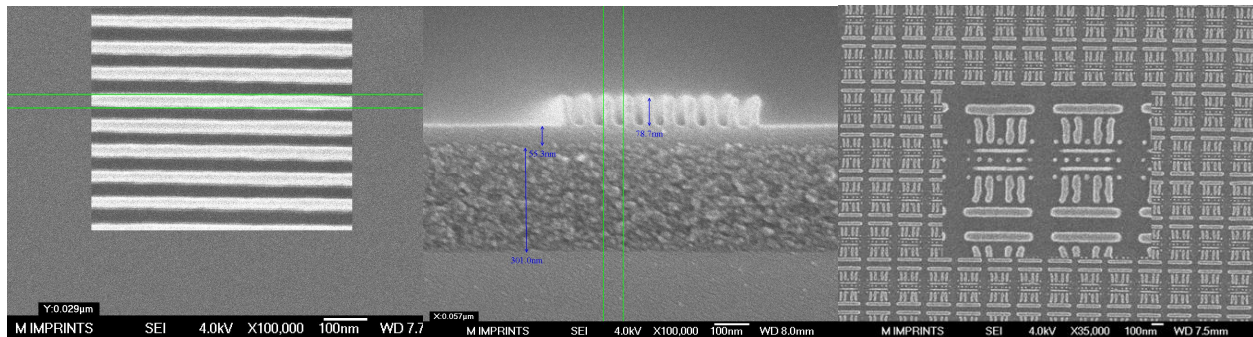

Figure 7. SEM images of 28 nm imprinted patterns. A cross section of the dense 28 nm lines depicts a wall profile of approximately 88 degrees.

c. Resist Processes for 22 nm

An attempt to improve the resolution of the ZEP520A to 22 nm resist consisted of a further reduction in resist thickness to 50 nm. The chromium thickness was also reduced on the test plate to 7 nm. The images obtained are shown in Figure 8. The 24 nm and 26 nm lines (Figures 8b and 8c) appear to be well resolved. The 22 nm half pitch features were also present (Figure 8a), although line edge fidelity was marginal and little exposure latitude was obtained. Further improvements in resolution may be realized by diluting the developer and developing at lower temperatures.[15]
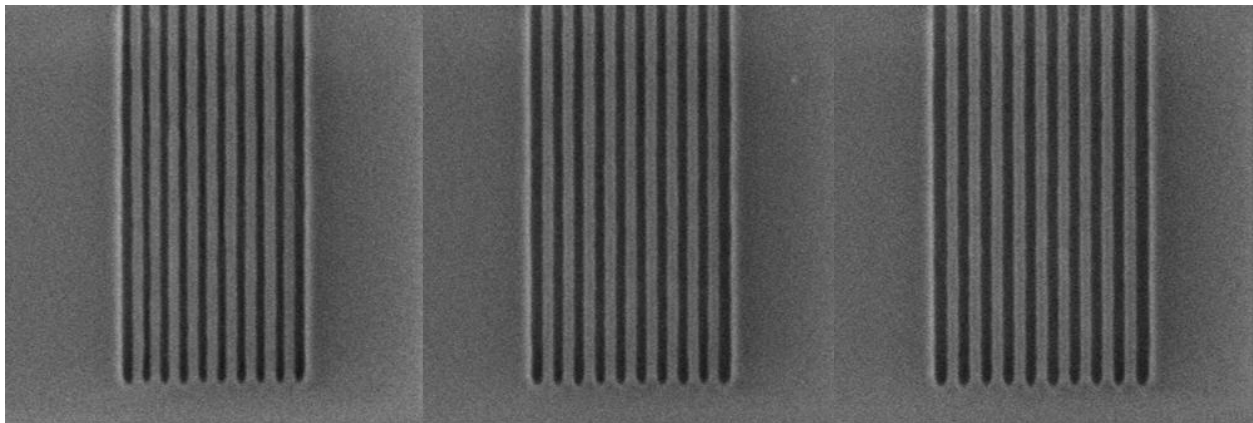

Figure 8. 22, 24, and 26 nm half pitch lines resolved in 50 nm of ZEP520A resist.

Sub-22 nm resolution is possible with negative tone HSQ resist. This material is coated from a 2 weight percent solution of HSQ in anhydrous MIBK. A 35 nm film of HSQ was exposed at 100 keV, developed in a 25 weight percent TMAH solution for 2 min, and rinsed in DI water. The resulting images are shown in Figure 9. Clockwise, from the top left are 20 nm Logic patterns, 20 nm half pitch lines, 20 nm Metal 1 patterns, and a 22 nm half pitch contact array. All patterns were obtained using a feature bias of -12 nm. Further development work is required to understand the resolution of the template patterns after chromium and fused silica etch, and to determine how far resolution can be pushed to address future silicon IC requirements.
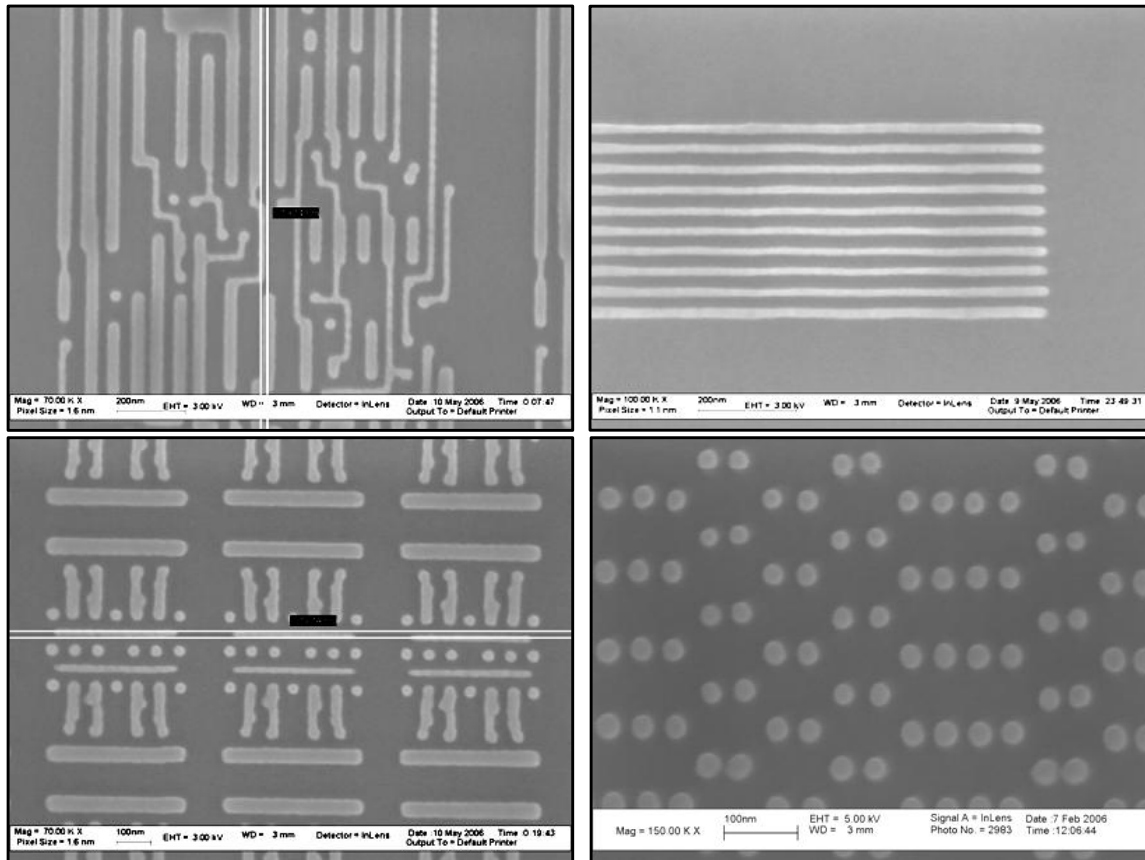
Figure 9. 20 and 22 nm features resolved in negative HSQ resist. Further work is required to convert the resist images into template features.

d. Lift-off Process for 22 nm

A lift-off process was employed in order to achieve resolution better than 28nm. All patterning was done on 150mm diameter fused silica wafers. Charging during electron beam exposure can be addressed by either applying a conductive topcoat on the e-beam resist, or by depositing a conducting layer beneath the resist. In this study, the latter method was employed. To generate the template relief images, patterns were exposed using a Vistec VB6 100 keV Gaussian beam writer. PMMA resist was chosen as the positive imaging resist. After development, a thin chromium layer was evaporated, followed a lift-off using dichloromethane. The remaining chromium features served as a hard mask for the etch into the fused silica.

The template features are defined using a reactive ion etch process. The etchant gases include CHF_3 and argon. The resulting features are shown in Figure 10. The features are well defined, with a minimum of defective areas. Occasional image placement problems were noted, however. In addition, there were several instances where the chromium did not adhere well to the substrate, resulting in missing pillar after the fused silica etch. One example of this can be observed in the image of the 23nm half pitch features below. The image profile is also less than optimal. It is likely that some erosion of the chromium mask occurs during the fused silica etch. A wall angle of better than 87° is preferred, and optimization of the etch process will be a subject for future investigation.
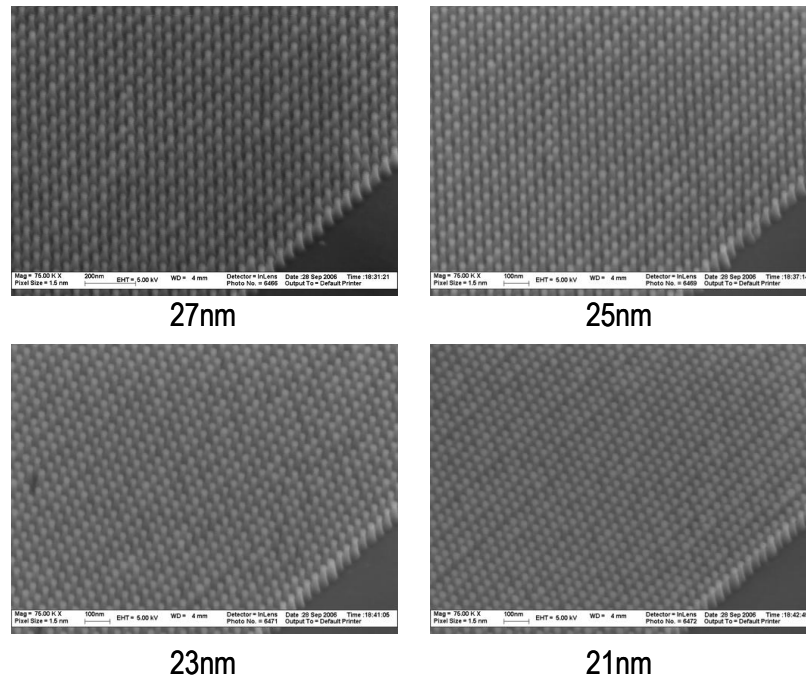
27nm   25nm

23nm   21nm

Figure 10. Template features after the fused silica etch. Dense features with a half pitch as small as 21nm were clearly resolved.

After the pattern transfer of the pillars was complete, the resulting templates were used for imprint studies. The results are depicted in Figure 11. Good uniformity was noted for the 27nm and 25nm arrays. More irregularities occur in the smaller features, and include CD nonuniformity, image placement errors, and missing holes. In general, the imprint process faithfully replicated the features on the template.
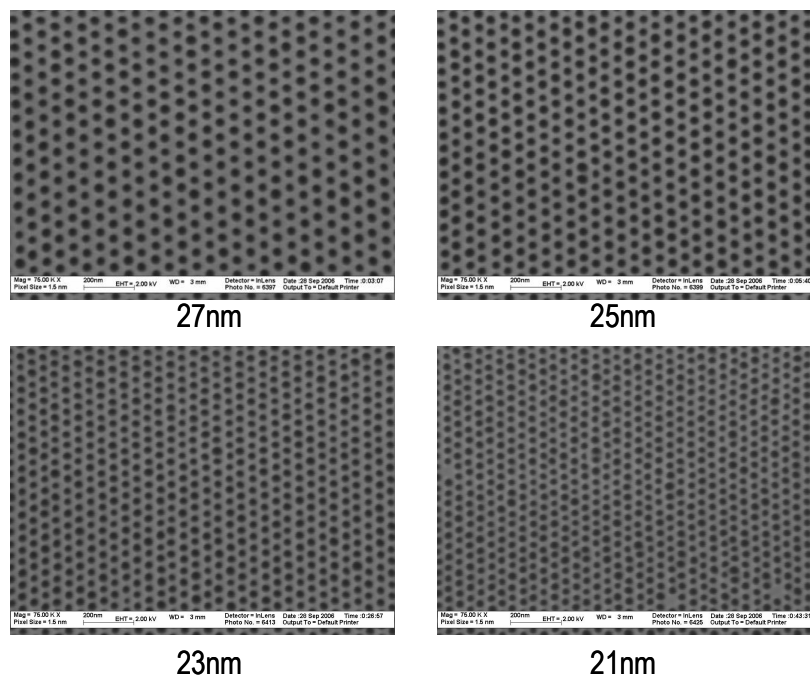

27nm   25nm

23nm   21nm

Figure 11. Imprinted contact patterns down to 21nm half pitch.

4. Conclusion

A template fabrication process was developed by improving the resolution and exposure latitude in ZEP520A resist. Imprinted features with a half pitch of 28 nm were clearly resolved. Resist processes have also been identified that can reduce the half pitch to 20 nm, however pattern transfer optimization of the template is required to realize the resolution enhancements. To address early unit process development at 22 nm, a lift-off process was used to create templates with half pitches as small as 21 nm. Templates were fabricated and successfully used to create corresponding imprints.

Acknowledgments

References

1. Henry I. Smith and S. E. Bernacki, J. of Vac. Sci. Technol. Vol. 12, Issue 6, pp. 1321-1323, 1975.

2. P. E. Mauger, A. R. Shimkunas, J. C. Wolfe, S. Sen, H. Löschner, and G. Stengl, J. Vac. Sci. Technol. B 10, 2819 (1992).

3. M. M. Mkrtchyan, J. A. Liddle, A. E. Novembre, W. K. Waskiewicz, G. P. Watson, L. R. Harriott, and D. A. Muller , J. Vac. Sci. Technol. B **16**, 3385 (1998)

4. H. C. Pfeiffer *et al.,* J. Vac. Sci. Technol. B **17**, 2840 (1999).

5. http://public.itrs.net/

6. T. Bailey, B. J. Choi, M. Colburn, M. Meissl, S. Shaya. J. G. Ekerdt, S. V. Sreenivasan, and C. G. Willson, J. Vac. Sci. Technol. B 18(6), 3572 (2000).

7. I. McMackin, J. Choi, P. Schumaker, V. Nguyen, F. Xu, E. Thompson, D. Babbs, S. V. Sreenivasan, M. Watts, and N. Schumaker, Proc. SPIE 5374, 222 (2004).

8. D. J. Resnick, W. J. Dauksher, D. P. Mancini, K. J. Nordquist, E. S. Ainley, K. A. Gehoski, J. H. Baker, T. C. Bailey, B. J. Choi, S. C. Johnson, S. V. Sreenivasan, J. G. Ekerdt, C. G. Willson, Proc. SPIE Vol. 4688, p. 205-213, 2002.

9. W. J. Dauksher, D. Mancini, K. Nordquist, D. J. Resnick, P. Hudek, D. Beyer, T. Groves, O. Fortagne, Microelectronic Engineering, Vol 75, Issue 4 , November 2004, 345-351

10. G. Jones, M. Saifullah, K. Subramanian, D. Anderson, D.-J. Kang, W. Huck, M. Welland, to be published in J. Vac. Sci. Technol. B., Nov/Dec 2006.

11. M. Irmscher, J. Butschke, G. Hess, C. Koepernik, F. Letzkus, M. Renno, H. Sailer, H. Schulz, A. Schwersenz, E. Thompson, Proc. SPIE Vol. 6151, (2006).

12. L. J. Myron, L. Gershtein, G. Gottlieb, B. Burkhardt, A. Griffiths, D. Mellenthin, K. Rentzsch, S. MacDonald, G. Hughes, Proc. SPIE, Vol. 5752, pp. 384-391, 2005.

13. M. Colburn, T. Bailey, B. J. Choi, J. G. Ekerdt, S. V. Sreenivasan, Solid State Technology, 67, June 2001.

14. D. J. Resnick, E. Thompson, L. J. Myron, G. M. Schmid, Microlithography World, Feb. 2006.

15. W. Hu, K. Sarveswaran, M. Lieberman, G. H. Bernstein, J. Vac. Sci. Technol. B 22(4), 1711 (2004).