Defect Inspection for Imprint Lithography Using a Die to Database Electron Beam Verification System

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ABSTRACT

Imprint lithography has been included on the ITRS Lithography Roadmap at the 32 and 22 nm nodes. Step and Flash Imprint Lithography (S-FIL™) is a unique method for printing sub-100 nm geometries. Relative to other imprinting processes S-FIL has the advantage that the template is transparent, thereby facilitating conventional overlay techniques. Further, S-FIL provides sub-100 nm feature resolution without the significant expense of multi-element, high quality projection optics or advanced illumination sources. However, since the technology is 1X, it is critical to address the infrastructure associated with the fabrication of templates.

With respect to inspection, although defects as small as 70 nm have been detected using optical techniques, it is clear that it will be necessary to take advantage of the resolution capabilities of electron beam inspection techniques. This paper reports the first systematic study of die-to-database electron beam inspection of patterns that were imprinted using an Imprio 250 system. The die-to-database inspection of the wafers was performed on an NGR2100 inspection system. Ultimately, the most desirable solution is to directly inspect the fused silica template. This paper also reports the results on the first initial experiments of direct inspection fused silica substrates at data rates of 200 MHz.

Three different experiments were performed. In the first study, large (350 -400 nm) Metal 1 and contact features were imprinted and inspected as described above. Using a 12 nm pixel address grid, 24 nm defects were readily detected. The second experiment examined imprinted Metal 1 and Logic patterns with dimensions as small as 70 nm. Using a pixel address of 3 nm, and a defect threshold of 20 nm, a systematic study of the patterned arrays identified problem areas in the design of the pattern layout. Finally, initial inspection of 200 mm fused silica patterned substrates has established proof of concept for direct inspection of imprint templates.

Keywords: imprint, lithography, electron beam, inspection, die to database, template

1. INTRODUCTION

Over the last thirty years, many different varieties of Next Generation Lithographies (NGLs) have been posed as successors to optical lithography. Examples include proximity x-ray lithography, ion beam lithography (both 1X and projection), and variants of projection electron lithography (such as SCALPEL and PREVAIL)[1-4]. Research targeted towards making these technologies viable for high density silicon manufacturing has all but stopped for the cases mentioned above. The reason for the discontinuation of funding for each case had very little to do with resolution. Each technology was clearly capable of resolving 100 nm features and had the potential to resolve geometries much smaller than 100 nm. Instead, the continued extension of optical lithography combined with the lack of a commercial mask infrastructure made it extremely difficult for any of these technologies to penetrate the silicon market.

Emerging Lithographic Technologies X, edited by Michael J. Lercel,
Proc. of SPIE Vol. 6151, 61510M, (2006) · 0277-786X/06/$15 · doi: 10.1117/12.659457

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Imprint lithography has been included on the ITRS Lithography Roadmap at the 32 and 22 nm nodes[5]. Step and Flash Imprint Lithography (S-FIL™) is a unique method for printing sub-100 nm geometries[6-8]. Relative to other imprinting processes S-FIL has the advantage that the template is transparent, thereby facilitating conventional overlay techniques. Further, S-FIL provides sub-100 nm feature resolution without the significant expense of multi-element, high quality projection optics or advanced illumination sources. However, since the technology is 1X, it is critical to address the infrastructure associated with the fabrication of templates.

The S-FIL blank has an advantage over the previously mentioned NGLs, in that the starting material is identical to what is being used in mask shops to today. In addition, the utilization of a stiffer substrate (as opposed to a membrane) minimizes the issues associated with pattern dependent image distortion. Although patterning at 1X dimensions is challenging, it should be appreciated that today's 4X optical proximity correction (OPC) designs require features as small as 1.5X. Writing time is also an advantage at 1X, because of the reduced writing area and the elimination of OPC.

The template fabrication sequence is very similar to the chromeless phase shift mask (PSM) process currently used in mask shops. Four 1X templates are fabricated on a standard fused silica quartz 6025 blank (6" x 6" x 0.25") with a 15 nm chromium layer. The processing sequence is depicted schematically in Figure 1. A standard positive tone resist is coated and exposed using either a fast shaped-beam pattern generator (common in mask shops) or a slower but higher resolution Gaussian-beam pattern generator (typically found in Research and Development facilities). The patterned resist serves as an etch mask for the thin Cr film. The Cr, in turn, is used as an etch block for the fused silica.

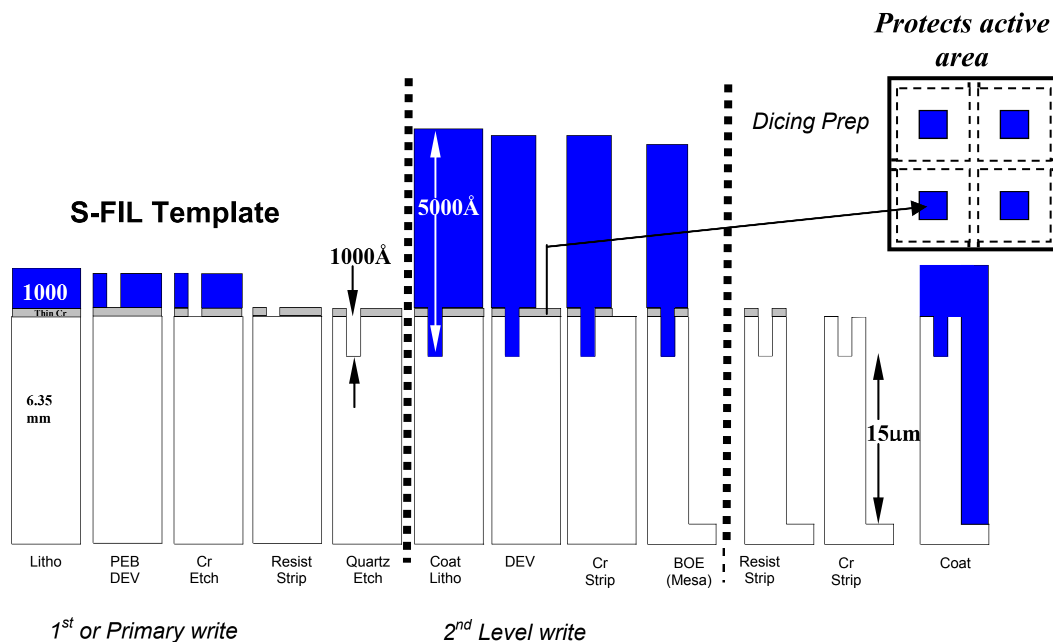

Figure 1. Template fabrication process flow

In both the Cr-less PSM and S-FIL template route, the second level lithography step is exposed using a fast optical writer, such as an Alta 3700 laser pattern generator. This step for Cr-less PSM is designed to expose the active area. In the case of an S-FIL template, it must protect the active area to enable formation of the 15 μm mesa or pedestal. The mesa is formed by etching the non-active areas using a wet buffered oxide etch (BOE) solution. The final step in the template process is a dice and polish step used to separate the plate into four distinct templates. An example of a final template is shown in Figure 2.

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Not described in the sequence above are the inspection and repair steps. With respect to inspection, although defects as small as 70 nm have been detected using optical techniques[9], it is clear that it will be necessary to take advantage of the resolution capabilities of electron beam inspection techniques. Previous electron beam inspection work established that programmed defects patterned on an ITO-based template can be calibrated in a CD SEM and inspected on a prototype e-beam inspection system of the KLA-Tencor eS30m[10]. This means that two important issues were addressed: the contrast is acceptable and surface charging does not seem to be an issue with a transparent conducting oxide such as ITO.

Although the methodology described above presents a viable approach for inspection, it also adds complexity to the template fabrication process. A second alternative is to perform electron beam inspection on an imprinted wafer, and compare the imprinted patterns to a database. This paper reports the first systematic study of die-to-database electron beam inspection of patterns that were imprinted using an Imprio 250 system. The die-to-database inspection of the wafers was performed on an NGR2100 inspection system. Ultimately, the most desirable solution is to directly inspect the fused silica template. This paper also reports the results on the first initial experiments of direct inspection fused silica substrates at data rates of 200 MHz.

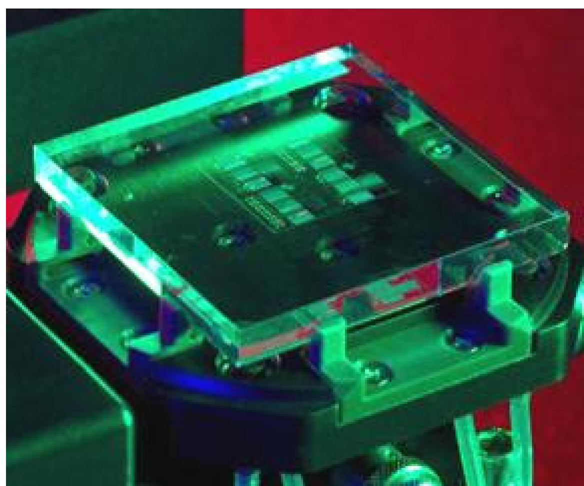

Figure 2. S-FIL template on an Imprio auto loader

2. EXPERIMENTAL DETAILS

For the first two experiments, 200 mm imprinted wafers were inspected. Templates were prepared in the typical way, generally following the flow described in Figure 1. Four 1X templates were fabricated on a standard fused silica quartz 6025 blank (6” x 6” x 0.25”) with a 15nm Cr layer. A common positive tone chemically amplified electron beam resist was coated (<150nm) and exposed using a 50keV electron beam pattern generator using. The Cr is used as an etch block for the quartz etch, both of which were dry etched using a production tool. Details of the pattern transfer process, including mesa formation and the dice and polish procedure, have been previously published[11]. The plate for the first experiment was provided by Toppan Photomask. The plate for the second set of experiments was provided by DNP.

After dice and polish, the templates were cleaned and imprinted using an Imprio 250 nano-imprint tool, on 200 mm wafers coated with 60nm of DUV30J, an inorganic bottom anti-reflective coating (BARC). A non silicon containing low viscosity Monomat material (resist) was used and cross-linked with UV light, exposed through the back of the transparent template. Process details and mechanics of S-FIL have also been described thoroughly elsewhere[7,12,13].

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The final inspection sample was prepared on a 200 mm fused silica wafer coated with a 15 nm Cr layer. A ZEP520A electron beam imaging resist was coated on the wafer and a high resolution Leica VB6 HR Gaussian beam writer operating at 100 KV was used to expose the patterns. The features of interest in this study included a Metal 1 like array, an SRAM contact pattern, and a Logic pattern. The specifics of each pattern are shown in Figure 3.

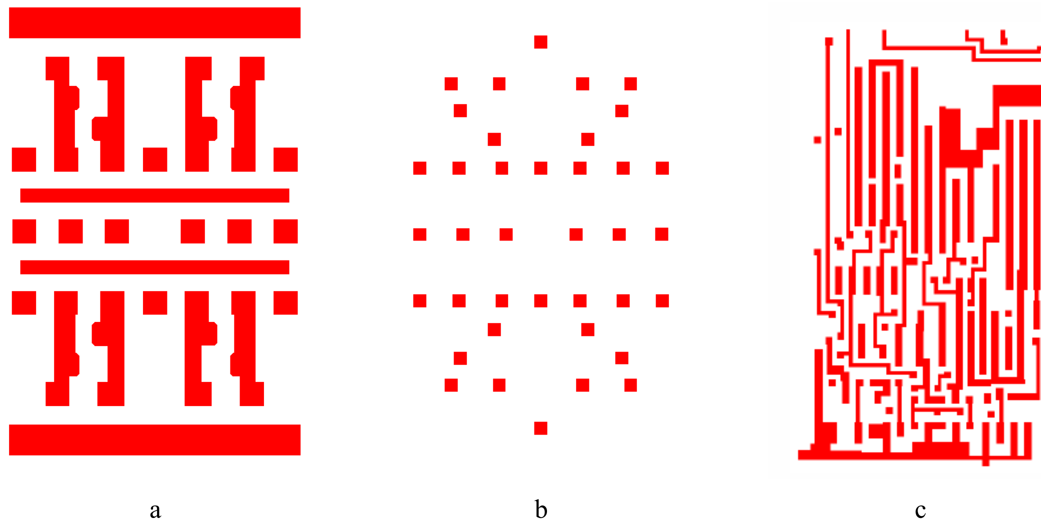

Figure 3. Patterns used for inspection: a) Metal 1 like structures. b) SRAM contact array. C) Logic pattern.

Inspections were performed with a Nanogeometry Research Inc. NGR2100 die-to-database system, which is presently configured to inspect 200 and 300 mm wafers[14]. The NGR2100 consists of an Electron Image Acquiring System (EIAS), a Geometry Verification Engine (GVE), and a GUI interface. The key features of the EIAS include high-resolution and high speed secondary electron acquisition capability, a scan generator to acquire images of a large area, and proprietary electron optics to eliminate field distortion over the wide scan field. A die is scanned by a field of view, step-by-step, to acquire the image to be verified. A feature contour is extracted, represented by lines and curves corresponding to the edges of the imaged feature. The contour is then compared to the target design data, to create a differential bias. The bias data is used to output to verify compliance with a known process window or CD measurement. The system operates at an accelerating voltage between 400 and 2000 V and samples at a maximum rate of 200 MHz. Examples of photolithographic defects detected with the NGR2100 are depicted in Figure 4.

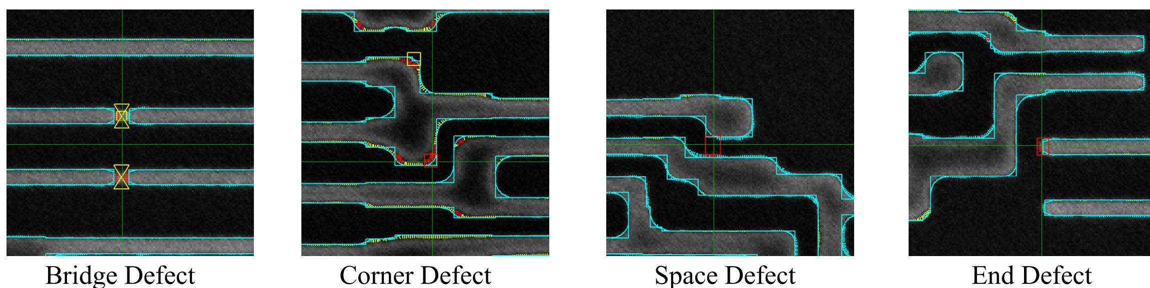

Figure 4. Four types of defects detected with the NGR2100 die to database inspection tool.

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3. RESULTS AND DISCUSION

a. 350 nm Metal 1 patterns and 400 nm Contacts

Initial experiments were performed on imprinted wafers using the Metal 1 and contact patterns depicted in Figure 3. Modest dimensions of 350 nm for the Metal 1 patterns and 400 nm for the contacts were chosen in order allow for defect learning on a KLA-Tencor 2132 resident at MII. Because of the larger pattern sizes, a pixel address of 12 nm was selected for inspection. Landing energy and probe current were 2300 V and 3 nA, respectively. The minimum threshold for defect detection was set to 24 nm.

Defects on the templates were determined by scanning multiple imprint fields and comparing the repeating defects to the database. For the 400 nm contact pattern, 162 defects were attributed to the template. Examples of two defect types are shown in Figure 5. Figure 5a. depicts a contact pattern with defects located toward the center and bottom right of the micrograph. In Figure 5b. the reference geometries are included, and the locations of the defects are marked in red. Arrows have been included in the micrograph as aids for the reader. The defect size for the center contact was measured to be 56 nm. Figure 5c. Shows the Metal 1 pattern with a small defect on the right edge of the center feature. Figure 5d includes the GDS layout and a marker for the detected defect. Again, an arrow has been added as a guide for the eye. The defect size in this case was 24 nm.

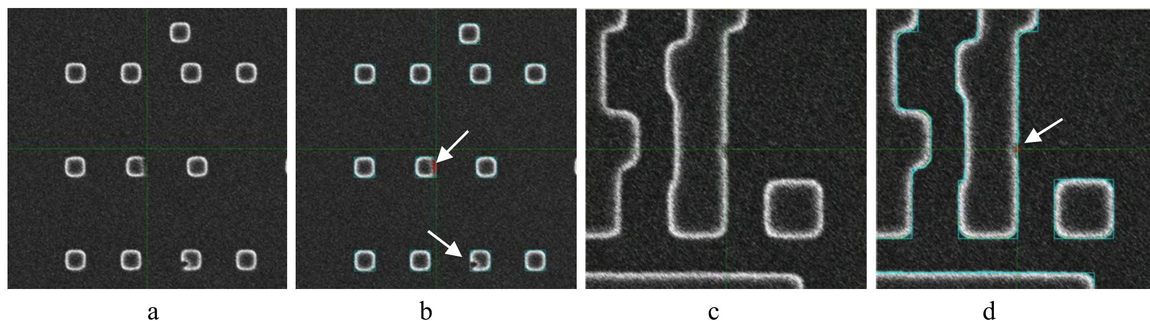

Figure 5. a) Defects detected on an imprinted contact array. b) The same contact array including the GDS layout and markers indicating the defect locations. c) Metal 1 pattern with a single defect. d) The same Metal 1 pattern with the GDS layout and a marker indicating the location of the defect.

b. Metal 1 and Logic patterns: 70 – 100 nm

Following the successful inspection of the larger patterns, the Metal1 and Logic patterns were scaled down to dimensions of 70, 80, 90 and 100 nm. Templates were fabricated and the resultant patterns were imprinted using an Imprio 250. Micrographs of the Metal 1 at 80 nm and 70 nm are shown in Figures 6a and 6b. For all feature sizes, the Metal 1 patterns were clearly resolved. In the case of the Logic pattern, the aggressive scaling eventually caused problems below 90 nm. Two areas in particular were noted in the 70 nm pattern and are marked on Figure 7. The first feature, shaped like a question mark (left), tended to close within the center of the feature at the smaller dimensions. The second feature, also in Figure 7(right), depicts a space with a dimension smaller than the coded dimension of the device. As a result, this feature tended to bridge at the smallest dimensions imaged.

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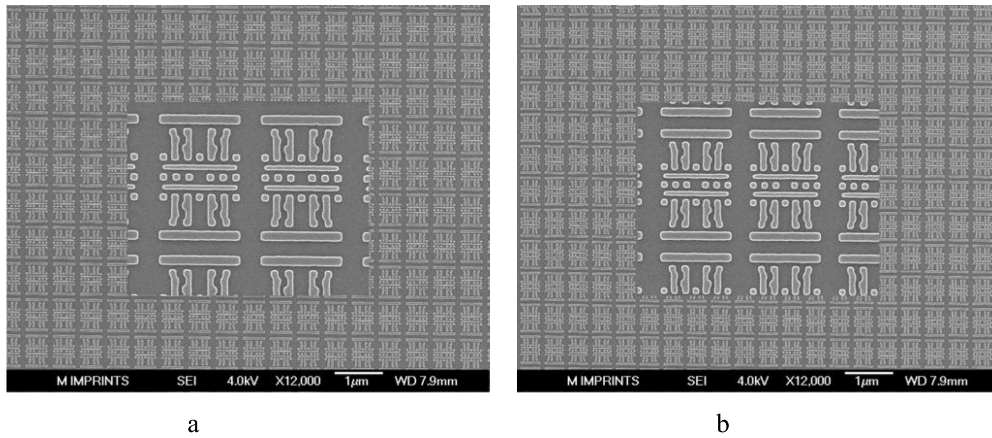

Figure 6. a) Imprinted 80 nm Metal 1 array. All of the Metal 1 patterns printed cleanly. b) Imprinted 70 nm Metal 1 array.

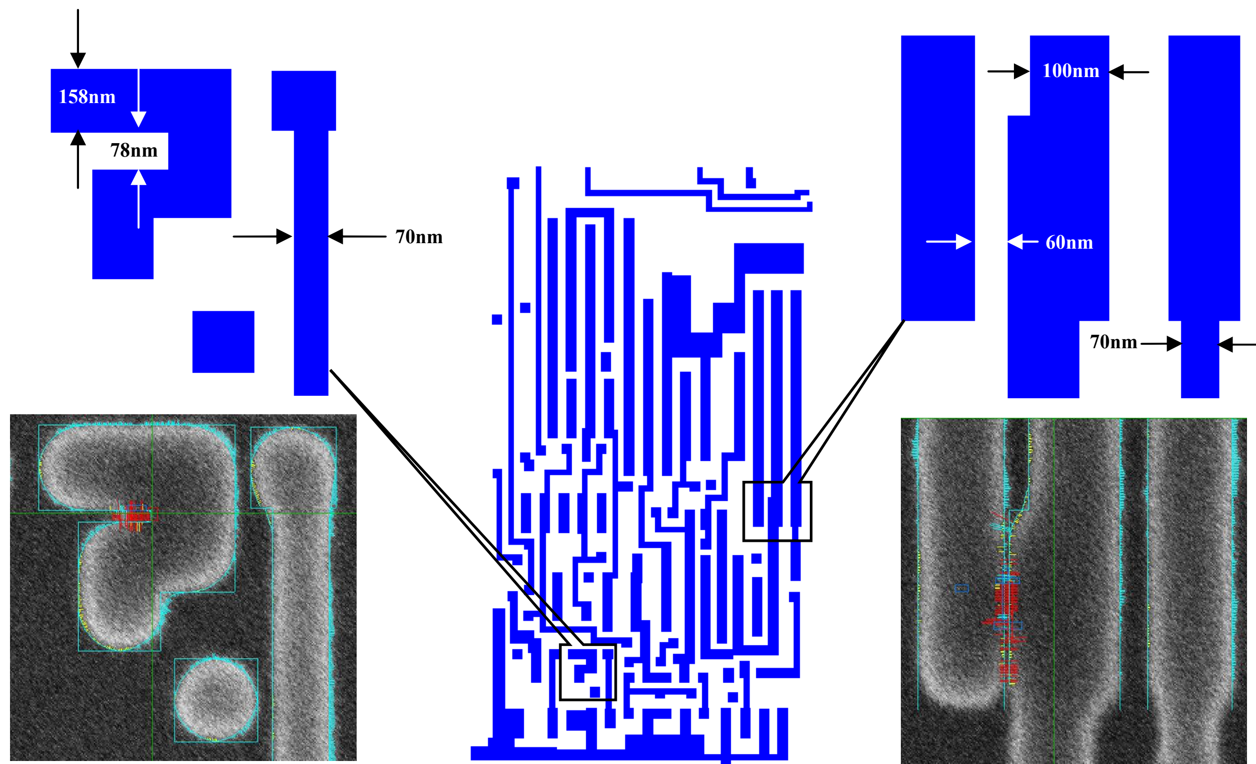

Figure 7. Imprinted 70 nm Logic CAD drawing (middle) and problem area magnifications on left (feature 1) and right (feature 2).

The clean Metal 1 pattern and degrading Logic pattern served as a good vehicle for inspection. The 0.50 mm x 0.50 mm areas containing the Metal 1 and Logic patterns were inspected at a 3nm pixel address. Threshold detection was set to 20 nm. Examples for two different arrays are shown in Figure 8. In each case, the Metal 1 patterns are located to the left, and the Logic patterns are located to the right. Starting in the upper left corner, the pattern dimensions

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start at 100 nm, and work their way clockwise down to 70 nm. The trend for both graphs is clear. Only one defect is detected in the Metal 1 arrays. In the case of the Logic patterns, very few defects are found at 100 nm and 90 nm. As the dimension shrinks to 70 nm, the number of defects detected becomes significant. In fact, 98% of the defects detected are the types described above.

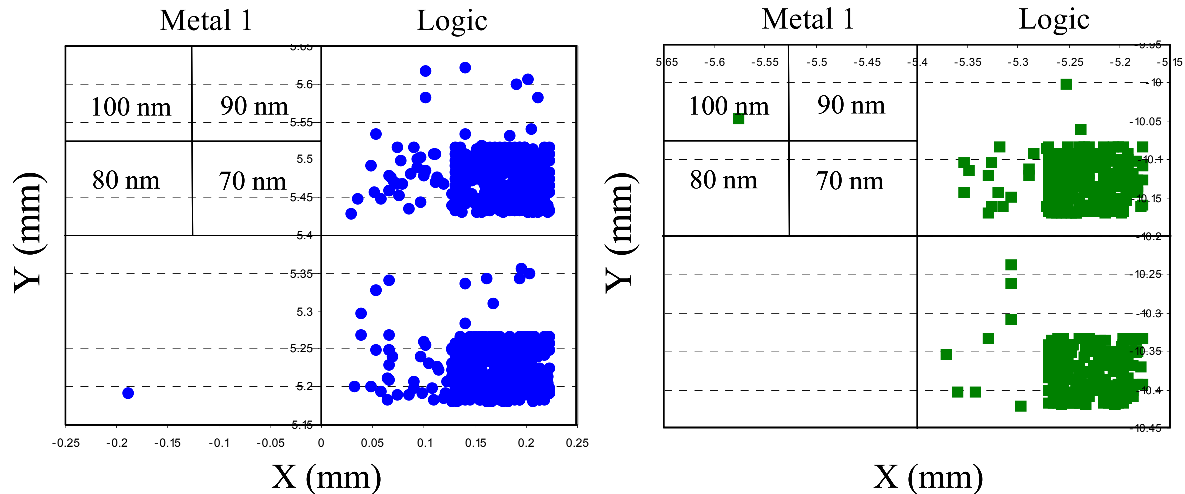

Figure 8. Graphic inspections of the Metal 1 and Logic patterns. The Metal 1 patterns remain defect free down to 70 nm. The Logic pattern degrades, however, as the dimension decreases.

c. Direct Inspection of Fused Silica Substrates

Direct inspection of a fused silica template is the preferred solution from an infrastructure point of view:

- It does not require change in materials for the fabrication of the template.
- It allows inspection of the template in the mask shop
- It does not require an additional imprint step to enable inspection

Inspection of dielectric substrates, in particular for the mask industry, has been demonstrated, and is now offered by several companies in CD SEMs and SEM review systems. Two examples include AMAT's gas injection RETicleSEM[11] and the Leica LWM 9000 SEM. The key issue is no longer charge dissipation, but addressing dissipation at data rates sufficient for mask or template inspection.

Because the current configuration of the NGR2100 accepts only 200 mm and 300 mm wafers, the final test patterns were prepared on a 200 mm fused silica wafer supplied by Shin-Etsu MicroSi. Logic and Metal 1 patterns were scaled down to 40 nm, and the images were etched 100 nm into the fused silica. Pixel addressing was set at 3 nm, with a threshold detection of 20 nm. Landing energy was set at 2700 V. The results from the first images are shown in Figure 8. Pictured in Figure 9a are the Metal 1 patterns. Starting from the upper left corner, the pattern dimensions start at 70 nm and decrease clockwise to 50 nm and 40 nm, and then increase back up to 60 nm. A magnified view of the 50 nm Metal 1 pattern is shown in Figure 9b. The roughness in the features is a result of an insufficient Cr etch, the fidelity of which is being captured by the NGR2100.

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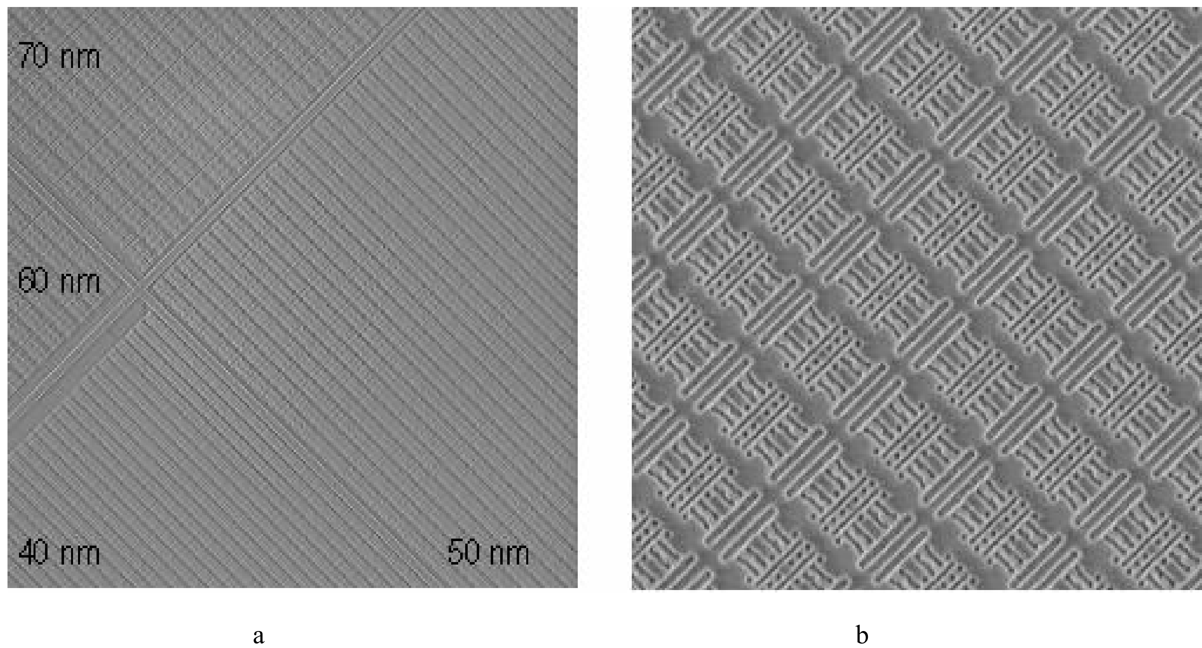

Figure 9. SEM images of Metal 1 patterns from a 200 mm fused silica wafer: a) 8000 x 8000 pixel image of the 40 – 70 nm Metal 1 patterns. b) A magnified view of the 50 nm Metal 1 pattern, extracted from Figure 9a.

Roughness in the final features precluded a systematic study, however the viability of the process is apparent. The Metal 1 patterns also included programmed defects located near the center of the pattern, as shown in Figure 10a. Programmed defect sizes ranged from 50 nm to 5 nm. Two examples of detected defects are shown in Figures 10b – 10e. Figure 10b depicts the SEM image from the NGR2100 of a 40 nm Metal 1 pattern including a programmed defect, indicated by circled area. Figure 10c includes the GDS layout of the pattern along with a marker for the defect area. The marker, in this particular case, shows up in a colored image as yellow, since the threshold value of 20 nm was not exceeded. A second example, shown in Figure 10d, depicts a bridge defect, and is indicated by the circled area. Figure 10e again includes the GDS layout along with a marker indicating the bridged area. The defect color, in this case is red, since the dimension exceeds the threshold of 20 nm. An arrow to the defect, has been included as a guide for the eye.

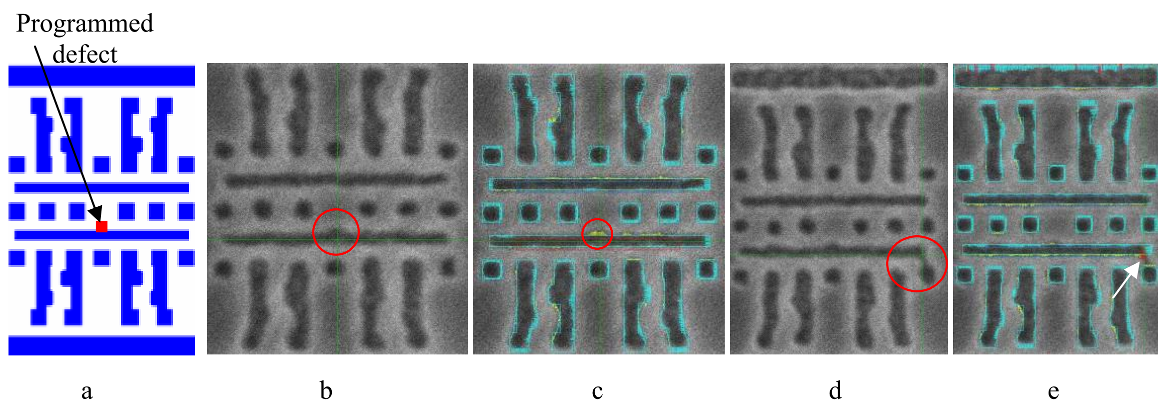

Figure 10. a) CAD drawing of the Metal 1 pattern including a programmed defect. b) SEM including a programmed defect. c) The same image with the GDS layout of the pattern and a marker of the programmed defect, measured at 15 nm. d) SEM photo depicting a bridge defect. e) Same photo including the GDS layout and a marker indicating the location of the bridge defect, measured at 20 nm. An arrow is included as a guide for the eye.

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4. CONCLUSIONS

Two methods have been presented for the inspection of imprint templates. The first methodology used a die to database approach on imprinted wafers. Information on template defects was extracted by measuring multiple printed fields and comparing repeating defects to the database. Proof of concept was also demonstrated for the direct inspection of fused silica substrates. Because the NGR2100 is not currently configured to accept photoplates or templates, proof of concept work was performed on 200 mm wafers. A pixel size of 3 nm and a minimum threshold detection of 20 nm were set for the finest work. It should be noted that this threshold is not the limit of the inspection tool, but a compromise on inspection time and signal to noise.

Future work will focus on inspection of sub 50 nm patterns and the direct inspection of photoplates and templates.

ACKNOWLEDGMENTS

The authors gratefully acknowledge Nobuhito Toyama and Naoya Hayashi from DNP, David Standfast from Motorola, Ed Nichols from Shin-Etsu MicroSi and Toppan Photomask's Round Rock site for the fabrication of imprint templates and substrates used in this analysis. The authors would also like to thank S. V. Sreenivasan, and Mark Melliar-Smith from Molecular Imprints Inc., and Michael Hoffman and Masahiro Yamamoto from NanoGeometry Research Inc. for supporting this research.

REFERENCES

1. Henry I. Smith and S. E. Bernacki, J. of Vac. Sci. Technol. Vol. 12, Issue 6, pp. 1321-1323, 1975.

2. P. E. Mauger, A. R. Shimkunas, J. C. Wolfe, S. Sen, H. Löschner, and G. Stengl, J. Vac. Sci. Technol. B 10, 2819 (1992).

3. M. M. Mkrtchyan, J. A. Liddle, A. E. Novembre, W. K. Waskiewicz, G. P. Watson, L. R. Harriott, and D. A. Muller , J. Vac. Sci. Technol. B **16**, 3385 (1998)

4. H. C. Pfeiffer *et al.,* J. Vac. Sci. Technol. B **17**, 2840 (1999).

5. http://public.itrs.net/

6. T. Bailey, B. J. Choi, M. Colburn, M. Meissl, S. Shaya. J. G. Ekerdt, S. V. Sreenivasan, and C. G. Willson, J. Vac. Sci. Technol. B 18(6), 3572 (2000).

7. M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S. V. Sreenivasan, J. Ekerdt, and C. G. Willson, Proc. SPIE, Emerging Lithographic Technologies III, 379 (1999).

8. M. Colburn, T. Bailey, B. J. Choi, J. G. Ekerdt, S. V. Sreenivasan, Solid State Technology, 67, June 2001.

9. Harald F. Hess, Don Pettibone, David Adler, and Kirk Bertsche, Kevin J. Nordquist, David P. Mancini, William J. Dauksher, and Douglas J. Resnick, J. Vac. Sci. Technol. B 22(6), Nov/Dec 2004, 3300 – 3305.

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10. Kevin J. Nordquist, William J. Dauksher, David P. Mancini, Douglas J. Resnick, Harald F. Hess, Donald W. Pettibone, David Adler, Kirk Bertsche, Roy White, Jeffrey E. Csuy, and David Lee, Proc. SPIE Vol. 5567, p. 853-863 (2004).

11. J. Myron, Liraz Gershtein, Gidi Gottlieb, Bob Burkhardt, Andrew Griffiths, David Mellenthin, Kevin Rentzsch, Susan MacDonald, Greg Hughes, Proc. SPIE, Vol. 5752, pp. 384-391, 2005.

12. M. Colburn, A. Grot, M. Amistoso, B. J. Choi, T. Bailey, J. Ekerdt, S.V. Sreenivasan, J. Hollenhorst, C. G. Willson, Proc. SPIE, Vol. 3997, pp. 453-457, 2000.

13. B. J. Choi, S. Johnson, M. Colburn, S.V. Sreenivasan, C. G. Willson, J. Precision Engineering, Vol. 25, no. 3, July 2001.

14. Tadashi Kitamura, Kazufumi Kubota, Toshiaki Hasebe, Futoshi Sakai, Shinichi Nakazawa, Neeti Vohra, Masahiro Yamamoto, Masahiro Inoue, Proc. SPIE, Vol. 5756, 73-84, 2005.

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