Fabrication of Nanometer Sized Features on Non-Flat Substrates Using a Nano-Imprint Lithography Process

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ABSTRACT

The Step and Flash Imprint Lithography (S-FIL™) process is a step and repeat nano-imprint lithography (NIL) technique based on UV curable low viscosity liquids. Generally nano-imprint lithography (NIL) is a negative acting process which makes an exact replica of the imprint mold and is subsequently dry developed to reveal the underlying substrate material. The authors have demonstrated a novel imprint process, which reverses the tone of the imprint and enables dry develop on nonflat wafers with good critical dimension control and resist layer thickness. This positive acting NIL process termed SFIL/R™ (reverse tone S-FIL), enables nano-imprinting over intrinsic substrate topology of the type commonly found on single side polished substrates. This paper describes the SFIL/R process and the results of pattern transfer on single side polished silicon wafers.

Key Words: Nanoimprint Lithography, Nano lithography, Imprint Lithography, Step and Flash Imprint Lithography

1. INTRODUCTION

The Step and Flash Imprint Lithography (S-FIL™) process is a step and repeat nano-imprint lithography (NIL) technique based on UV curable low viscosity liquids.[1,2,3] Investigations by this group and others have shown that the resolution of replication by imprint lithography is limited only by the size of the structures that can be created on the template (mold). S-FIL uses field-to-field drop dispensing of UV curable liquids for step and repeat patterning. This approach allows for nano-fabrication of devices with widely varying pattern densities and complicated structures. The imprint material can be tailored to have good etch resistance for subsequent pattern transfer. In particular Molecular Imprints has formulated imprint materials which demonstrate good etch selectivity and are therefore useful for hard mask processes. The imprinted pattern is transferred to the substrate by dry plasma processes here referred to as the dry development step.

Generally nano-imprint lithography (NIL) is a negative acting process which makes an exact replica of the imprint mold and is subsequently dry developed to reveal the underlying substrate material. A number of challenges exist with standard NIL including template lifetime, throughput and residual layer tolerances, and critical dimension control during the dry develop. Molecular Imprints has implemented successful solutions to these problems through template design and fabrication, materials formulation, imprint tool and process development including the dry develop step. Patterning non flat substrates with nano-features is particularly challenging; especially when substrate topology exceeds the imprint feature height. At some length scale imprint lithography effectively planarizes the substrate thus creating a variation in the residual layer of the imprint. The S-FIL process, when practiced using a rigid template, effectively planarizes substrates within the imprint field. This of course can present problems when imprinting patterned wafers or typical single side polished wafers. The nanotopology of single side

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polished wafers can be significant, even up to many hundreds of nanometers, within an 25 x 25 mm imprint field area.[5]

A simple calculation can be used to illustrate the importance of wafer flatness for standard NIL processes. Assuming a non-conforming template and a residual layer thickness variation defined by the intrinsic wafer nanotopology, the maximum surface height variation for pattern transfer is given by:

$P\text{-}V = F_h / n,$

where $n > 2$ if the pattern is to survive the dry development step, F_h is the feature height, P is the highest point on the wafer surface and V is the lowest point on the wafer surface. Based on this calculation the wafer flatness required for standard non conformal NIL is 60 nm if the feature height of the imprint layer is 60 nm high.

The authors have demonstrated a novel imprint process which reverses the tone of the imprint and enables dry develop on nonflat wafers with good critical dimension control and resist layer thickness. This positive acting NIL process termed SFIL/R™ (reverse tone S-FIL), enables nano-imprinting over intrinsic substrate topology of the type commonly found on single side polished substrates.[5] The SFIL/R process is capable of pattern transfer of sub-onehundred nanometer features on these non-flat substrates and can also be applied to lift-off applications owing to the ability to produce "T" topped features under certain process conditions. This multilayer imprint process is enabled by the particular material set developed by the authors, which results in improved critical dimension control during etch pattern transfer due to good differential etch resistance.[4] The dry develop process utilizes a hard mask approach as the key enabler in the fabrication of nano structures on a range of substrate types with varying degrees of flatness including, but not limited to GaAs, InP, germanium, quartz and silicon. The material set and process flow are described in detail and new data presented correlating measured substrate topology with the resulting transferred pattern critical dimension variations for sub one hundred nanometer features.

The S-FIL/R process flow is similar to standard NIL processes with the added step of applying a planarization layer on top of the imprint subsequent to the dry develop step. The imprint material is purely organic in nature such that its etch rate differential is small compared to the underlying transfer layer. The planarization layer is etched back to reveal the tops of the imprint pattern. The planarization layer in the work described here is a high silicon content material which when exposed to an oxygen plasma forms a hard mask of SiO_2. The etch back of this layer to reveal the imprint feature tops is accomplished using a fluorine and oxygen containing plasma. The detailed process flow for the S-FIL/R process is described below.

2. S-FIL/R PROCESS FLOW

Step 1: Transfer layer application. In most cases the substrate is coated with one or more transfer layers prior to imprinting. The typical transfer layer thickness is between 60 and 240 nm depending on the feature size and substrate etch chemistries involved. The choice of transfer layer materials depends on several factors including but not limited to good wetting and adhesion performance of the imprint material to the underlying substrate, and subsequent process requirements. For example, if a lift-off process or substrate etch masking is required. For routine processing, where lift-off is not required, Brewer Science, DUV30J is used because of its adhesion, wetting performance and etch resistance. The transfer layer planarizes submicron features and provides conformal coating of larger features. Figure 1 depicts the substrate coated with the transfer layer. The substrate is drawn with a curved line to depict the presence of nanotopology.

Figure 1: Substrate is coated using Brewer Science DUV30J as a transfer layer. A typical coating thickness of between 60 and 240 nm is used.

Step 2: Imprinting. The coated substrate is then imprinted with the target device layer patterned template using a non-silicon containing imprint material (MonoMat™). The imprint layer effectively planarizes the local nanotopology on the substrate such that underlying substrate topology largely determines residual layer thickness variations. If the imprint were to be dry developed at this point, complete loss of the pattern could result if the residual layer thickness variations were at least the dimensions of the feature height.

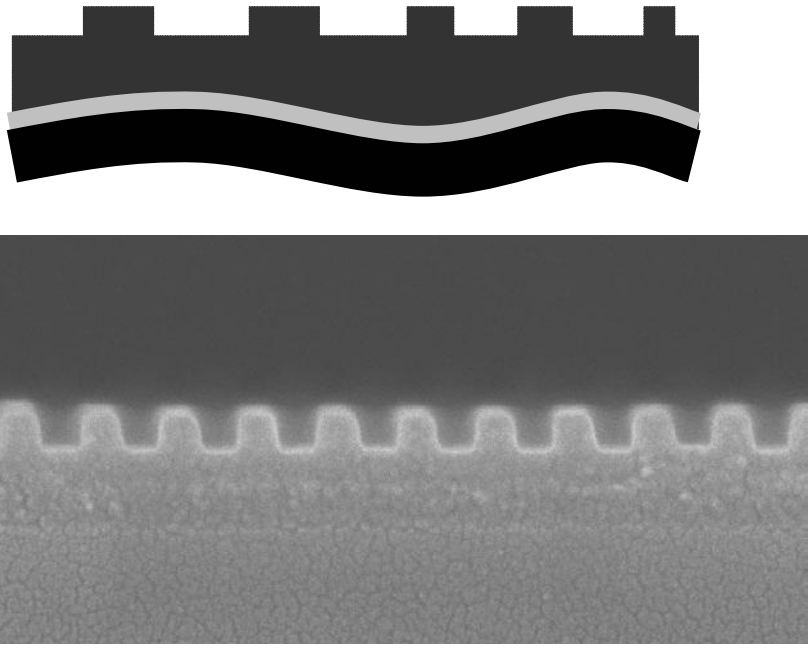
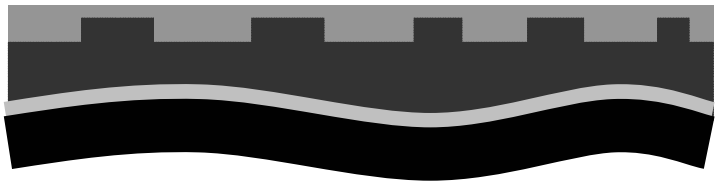


Figure 2: Imprint on transfer layer. The imprint layer on prime, double side polished lithography grade silicon wafers has a mean residual layer thickness of 60 nm and a tooth height of 60 nm.

Step 3: Planarization over imprint. The imprinted substrate is then spin coated with a high silicon content resist material (SilSpin™), which planarizes the imprint pattern topography. The Silspin is specially formulated to enable planarization over nanometer and micron sized features, which minimizes layer thickness variations over large (>100 μm sized) features. The Silspin provides good etch selectivity with the underlying resist layers and substrate etch chemistries.



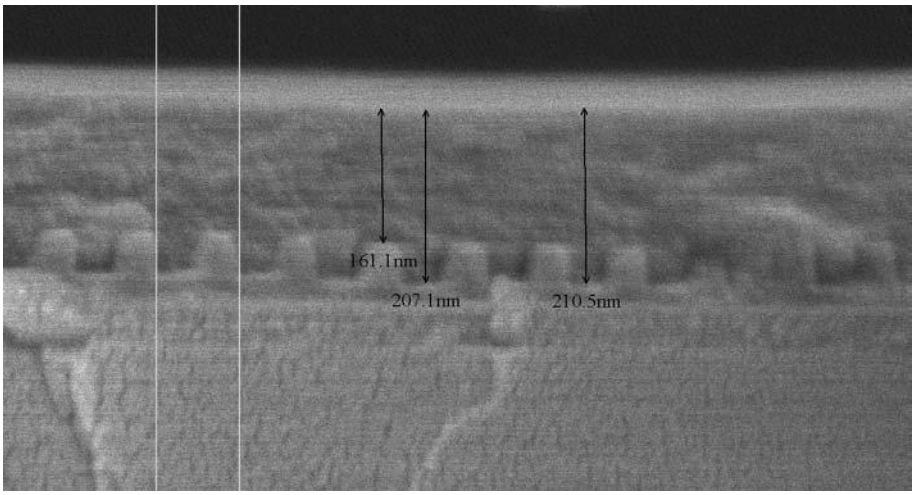


Figure 3: Spin-on planrization of imprint using Silspin. Silspin is a high silicon content spin on planarization material, which provides good etch selectivity to the underlying imprint and transfer layers.

Step 4: Break through Silspin etch. The Silspin planarization layer is etched back using a halogen-oxygen etch under anisotropic conditions, e.g. CHF_3/O_2. Once the tops of the imprinted features are exposed the halogen etch is stopped. This process step requires sufficient time and oxygen for oxidation of the high silicon content Silspin layer to occur, resulting in improved etch selectivity relative to the underlying resist layers and substrate.

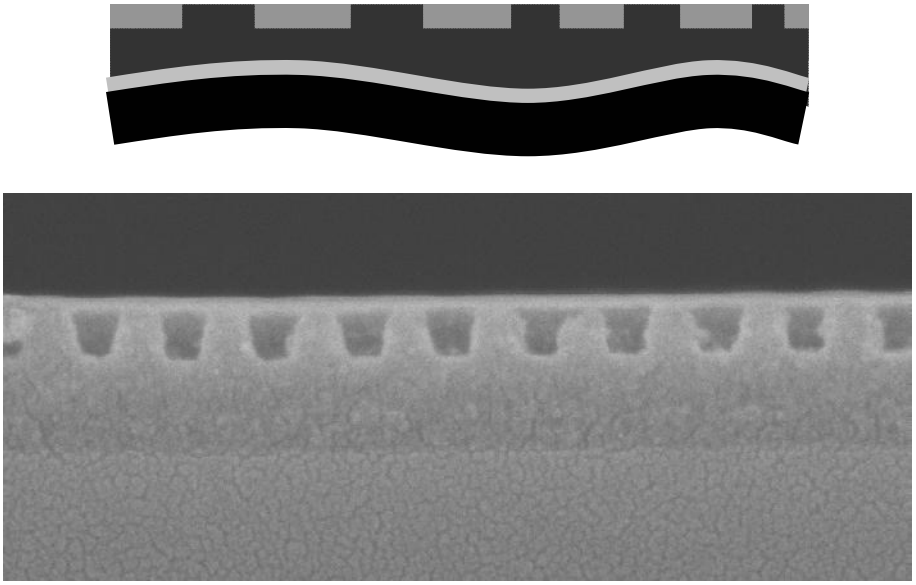


Figure 4: Breakthrough etch of Silspin planarization layer. The Silspin is etched back to reveal the tops of the imprinted features at which point the etch process is stopped.

Step 5: Feature definition. The exposed imprint layer regions are selectively etched through the transfer layer to the substrate using oxygen under anisotropic conditions. The oxidized Silspin provides good etch selectivity compared to the imprint and transfer layers resulting in good critical dimension control of the newly formed features.

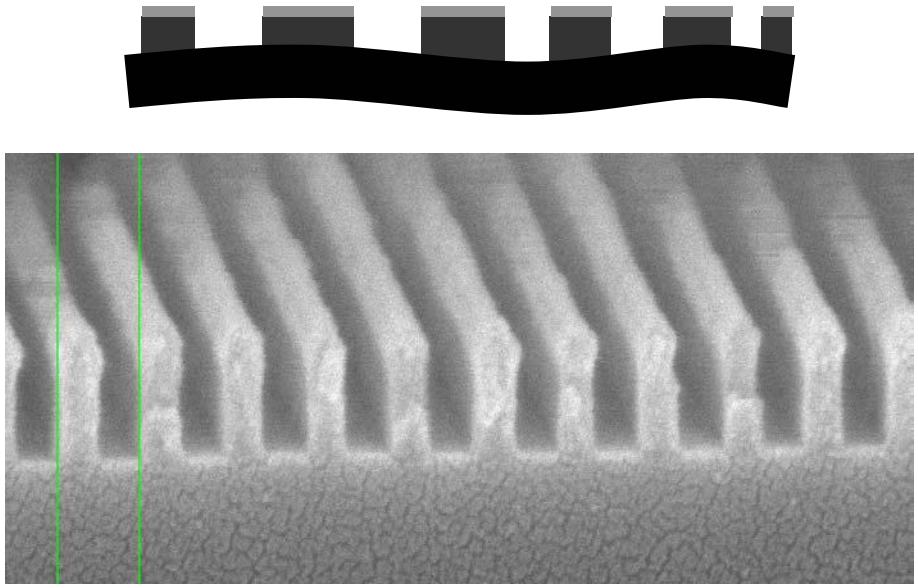


Figure 5: Final etch to define features. The imprint and transfer layers are etched down to the substrate using oxygen under anisotropic conditions.

The S-FIL/R process makes use of the hard mask approach to improve etch selectivity so that the features are dry developed with good feature fidelity.

3. PATTERN TRANSFER RESULTS USING S-FIL/R

Single and double side polished 100 mm diameter silicon wafers were imprinted and dry developed using the S-FIL/R process. The Si wafer surface height variations were estimated using the residual layer thickness variations for the imprinted wafers. Single side polished Si wafers demonstrated near 100 nm in residual layer variations while the double side polished Si wafers demonstrated near 25 nm of variation peak to valley. It is important to understand the effect the dry develop step will have on the critical dimension variation of the features, which are transferred by dry etching. A simple model describes the tolerances between the etch anisotropy and the critical dimension of the features to be transferred. The features of interest in the present study are 50 nm line/space features. The equation which describes the allowable wafer surface height variation for a given target critical dimension is as follows:

$$P\text{-}V = 2(CD)EA,$$

where CD is the desired critical dimension variation, EA is the etch anisotropy, P is the highest point on the wafer and V is the lowest point on the wafer plane. For a 50 nm feature a critical dimension variation of ten percent is allowable. The etch anisotropy is assumed to be 10:1. Given these values the maximum allowable surface height variation predicted by equation 2 is 100 nm. Given that the surface height variations measured for the single side polished wafer are near 100 nm these wafers provide a good test case of the S-FIL/R process.

To analyze the effect of the dry develop step on the critical dimension transfer the imprints from the template were measured to understand the relative critical dimension variation of the template features. Figure 6 contains a cross section and top down SEM micrograph of a section of the imprinted features. As can be observed from the micrograph the critical dimension variation of the imprinted features is near 5 nm.

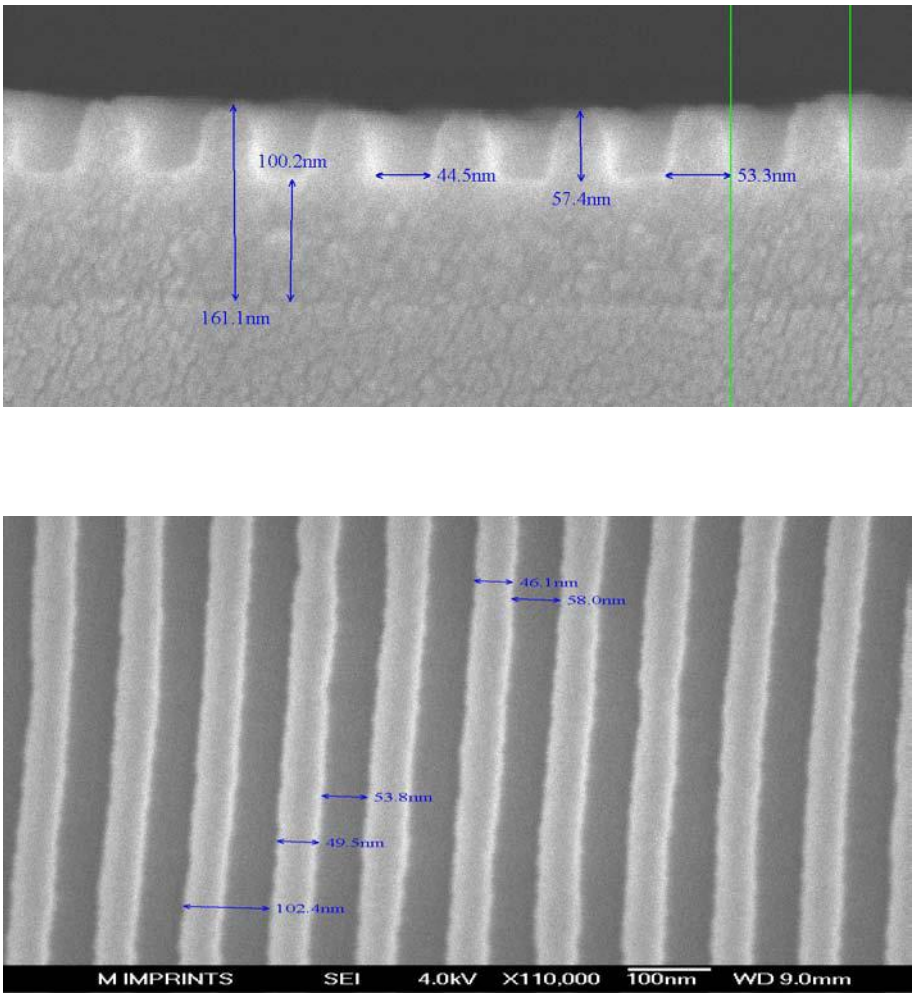


Figure 6. SEM micrographs of a cross section (top) of the 50 nm l/s imprint. The feature height is 60 nm, the residual layer is 40 nm, the transfer layer is known to be 60 nm and the critical dimension of the feature is near 50 nm. The top down SEM micrograph (bottom) shows a nearly 5 nm variation in the critical dimension for the pattern. This variation is mainly due to the line edge roughness of the template.

As can be seen the in SEM micrographs, the critical dimension of the cross section is near 50 nm, the feature height is 60 nm, and the residual layer is 40 nm. The transfer layer thickness as measured before imprinting was 60 nm. Imprinted single and double side polished Si wafers were coated with Silspin and dry developed.

Double side polished wafers with 30 nm of residual layer thickness variation were processed using the S-FIL/R process. The results show little variation in dry developed feature height, which can be expected from the small residual layer thickness variation. Subsequent to S-FIL/R processing it was observed that the critical dimensions of the dry developed features were near those of the imprinted features. Figure 7 shows a micrograph of 50 nm l/s features after dry develop.

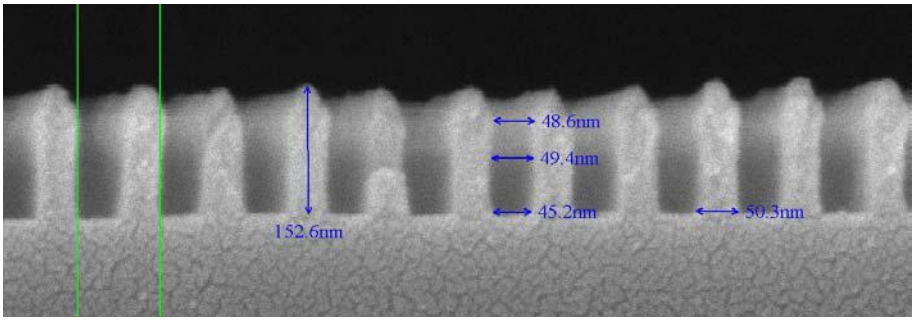


Figure 7. SEM micrograph of an 50 nm l/s pattern after dry developing an imprint. The critical dimension of the features is near that shown in the top down and cross section images of Figure 6.

Prior to pattern transfer the sample had the film thicknesses shown in Table 1.

Table 1. Layer thicknesses of SFIL/R patterned wafers on double side polished 100 mm diameter wafers.

Imprint Layer	**Thickness**	**Unit**
Transfer layer	60	nm
Mean residual layer	50	nm
Residual layer variation	25	nm
Feature height	60	nm

The resulting resist stack height prior to the dry develop step is 170 nm. After the dry develop step the resist height was near 150 nm indicating nearly 20 nm of Silspin is etched away during the feature definition etch step. No critical dimension variations outside those due to line edge roughness of the template and measurement variability were observed for the dry develop step on double side polished Si wafers.

Single side polished Si wafers were processed using S-FIL/R in a similar manner to the double side polished wafers. The residual layer thickness variations were more than three times those of the double side polished wafers at greater than 100 nm as seen in Table 2.

Table 2. Layer thicknesses of SFIL/R patterned wafers on single side polished 100 mm diameter wafers.

Imprint Layer	**Thickness**	**Unit**
Transfer layer	60	nm
Mean residual layer	50	nm
Residual layer variation	100	nm
Feature height	60	nm

Figure 8 shows SEM micrographs of the features that result after imprinting and dry developing the 100 mm diameter single side polished wafers.

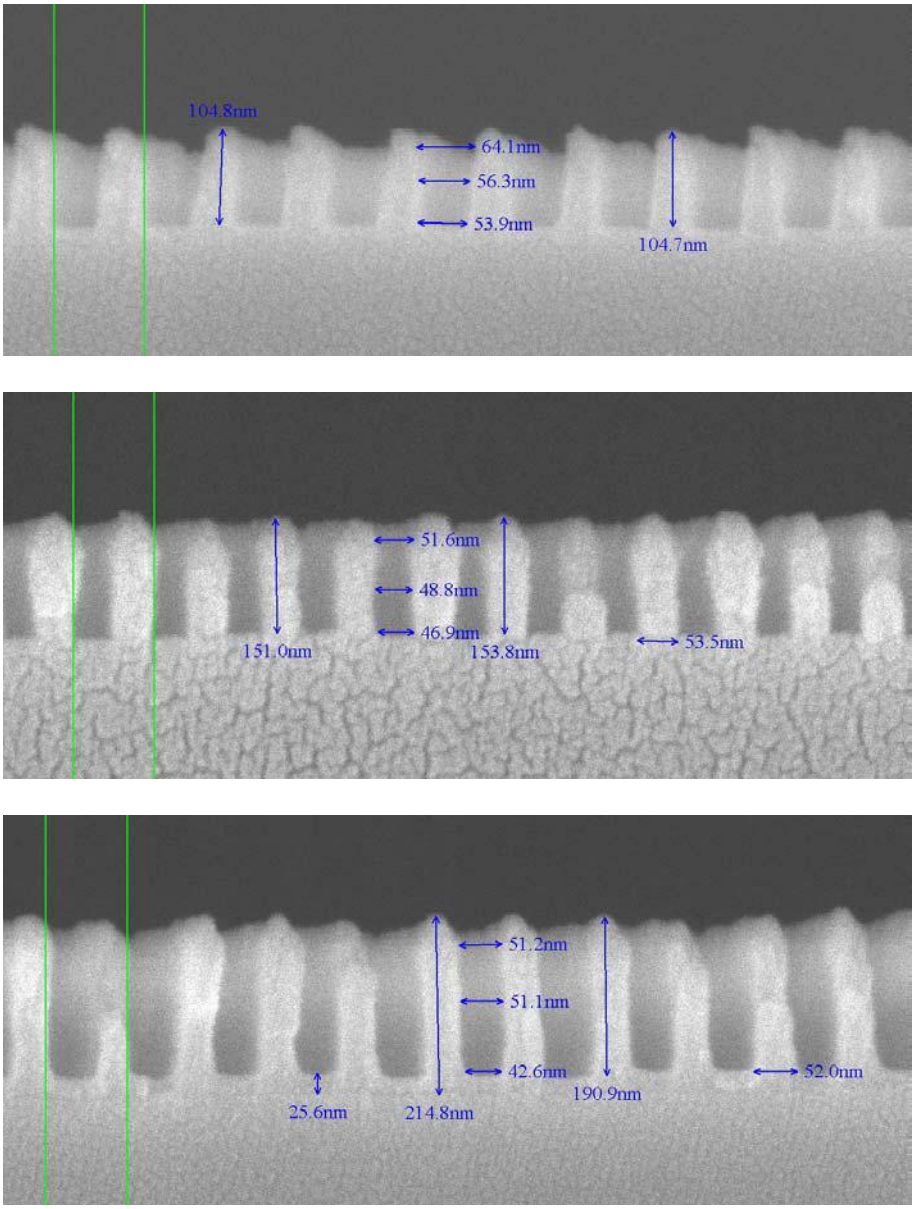


Figure 8. SEM micrographs if 50 nm l/s patterns after the dry develop step. The feature height variation is the result of intrinsic wafer height variations. The resist height variation of 114 nm is observed with a critical dimension near the calculated 5 nm window.

The observed resist height variation of 114 nm is near the measured residual layer variation of 100 nm and thus can be assigned to the surface height variations of the single side polished wafer. The micrographs show feature heights in the 90 nm range as a result of the residual layer variations. The bottom micrograph shows features that were not etched to the substrate, but the critical dimension measures within the 5 nm variation expected from the measurement of the imprinted features. The critical dimension measurements in Figure 8 are within the expected line edge roughness and measurement variation tolerances.

4. SUMMARY

The S-FIL/R process was presented and described using a simple model and experimental data from process runs on double and single side polished silicon wafers. The model is based on the dry develop etch anisotropy and critical dimension tolerance as a means to predict the allowable wafer height variations for good critical dimension control. The S-FIL/R process was used on 100 mm diameter double and single side polished wafers as a means to verify the model. The results shown in Figures 7 and 8 demonstrate the ability of the S-FIL/R process to replicate critical dimensions of imprinted features even on wafers with surface height variations in excess of 100 nm.

Future work will focus on wafers with greater topology to determine the limits of the SFIL/R process for critical dimension control. However, this work demonstrates that the SFIL/R process is capable of maintaining good critical dimension control of sub-onehundred nanometer features on wafers with surface height variations as seen on single side polished wafers .

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