Development of an Etch-definable Lift-off Process for Use with Step and Flash Imprint Lithography

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ABSTRACT

Along with other Next Generation Lithography (NGL) methods, imprint lithography has been included on the International Roadmap for Semiconductors (ITRS) for the 32 nm node, predicted to be production-ready by 2013[1]. Step and Flash Imprint Lithography (S-FIL) is one of the imprinting technologies being pursued due to its impressive imprinting capabilities, where imprinted features of less than 30 nm have been demonstrated. Unlike optical-based lithography, S-FIL uses techniques similar to that of contact printing, and thereby does not require complex and expensive optics and light sources to create images. Couple this with a reliable pattern transfer, and S-FIL could become a contender as a viable NGL technology. Similar to other imprint lithography systems, S-FIL printed features possess a residual layer several hundred angstroms thick, which requires a breakthrough etch prior to etching a subsequent layer. Of a greater concern, however, is the etch barrier used as the imaging layer for S-FIL. The present silicon content is limited to approximately nine percent, and the formulation is optimized for dispensing and achieving mechanical properties for the imprinting process. As a result, oxygen-based plasmas typically used for pattern transferring more conventional bi-layer structures are not compatible with the current S-FIL resist stack, and therefore pose a challenge from an etch perspective. The development of a recent etch process incorporating an ammonia-based plasma was a key enabler for pattern transfer, and ongoing development is being done to improve critical dimensions (CD). In this study, we examined a lift-off process using S-FIL. The material stacks with and without a "glue" layer will be discussed, and the challenges from imprinting to etch will be shared. Finally, the lift-off process will be used to demonstrate fabrication of a surface acoustic wave (SAW) device in addition to demonstrating patterning of a non-reactive metallization scheme such as Ti/Au.

KEY WORDS: Lift-off, Step and Flash Imprint Lithography, S-FIL, etch

1.0 INTRODUCTION

To meet the demand for the ever-changing and rapid advancements in the microelectronics industry, the need for sub-nanometer features while increasing device performance is to be expected. These critical dimensions have placed limitations for conventional lithography for sub-100 nm resolution due to optics and resist constraints. As a result, a change in philosophy for device manufacturing must be realized. Using phase shift mask technology, 193-nm "dry" photolithography has demonstrated sub-100nm features; however, beyond the 90-nm node, feature resolution becomes limited[2]. For the last several years, the industry has recognized 157 nm lithography and Extreme Ultra Violet Lithography (EUVL) as the two leading Next Generation Lithography (NGL) techniques to supplant 193-nm dry lithography. Recently, 193-nm immersion lithography has attracted much attention. This technology utilizes a thin liquid film between the final lens and the wafer to improve depth of focus due to the changes in light path[3]. At Semicon West 2004, Carl Zeiss SMT boasted of its newly developed Starlith® 1250i lens for 193-nm immersion lithography, which claims to produce resolution down to 70 nm. While these Next Generation Lithography systems offer hope for optical-based technologies, none have a clear pathway to overcome cost-effective solutions for technical issues such as optics, illumination sources, imaging materials, etc., to successfully be implemented for a production environment. Along with projected cost of ownership, the

technical hurdles for both optical upgrades along with material research could constrain these NGL technologies from being competitive.

In parallel, imprinting technologies are being pursued as an alternative approach for nanolithography. Unlike optical technologies, these imprinting techniques are based on contact printing, and therefore do not require expensive and complex optics and light sources for creating images. As a result, imprinting may offer the possibility of greater simplicity and lower cost for producing sub-100 nm resolution. Step and Flash Imprint Lithography is one of several nano-imprint techniques showing some potential and could create a viable and competitive lithography solution for both semiconductor and non-semiconductor-related applications.

S-FIL utilizes a multi-layer scheme similar to that of bi-layer resist technology; however, unlike bi-layer systems, a residual layer of the etch barrier (EB) remains as part of the imprinted pattern. This residual layer requires a breakthrough etch prior to etching the underlayer materials, and therefore, a lift-off stack using a bi-layer structure with a re-entrant profile similar to that of optical lithography is not possible using S-FIL. A two-layer or three-layer stack is required. Another obstacle with S-FIL technology is the imaging resist used. Distinct from optical resist, the EB material used for S-FIL is of a different material formulation. This formulation especially deviates from typical resist systems in that the silicon content is extremely low (~ 9%). In addition, the material properties for the EB are selected based upon imprint requirements (e.g., viscosity, mechanical strength, etc.), and not necessarily on etch requirements. As a result, this film not only provides insufficient etch resistance during pattern transfer when using conventional oxygen-based plasma etching techniques, but adhesion of the EB to some materials is limited. While the detail process for S-FIL has been discussed elsewhere[4-6], Figure 1 depicts the basic S-FIL process steps to obtain an imprinted feature, where the EB is first dispensed on the wafer (a) follow by an in-situ low pressure compression of the template to the EB and UV (ultra violet) cure (b). The template is then release leaving the micro-molded pattern (c) along with a residual layer several hundred angstroms thick.

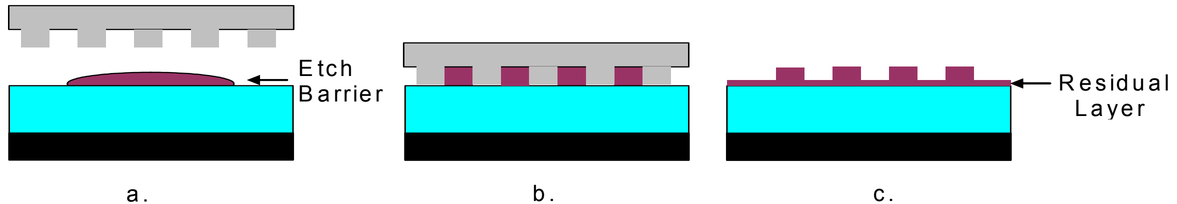
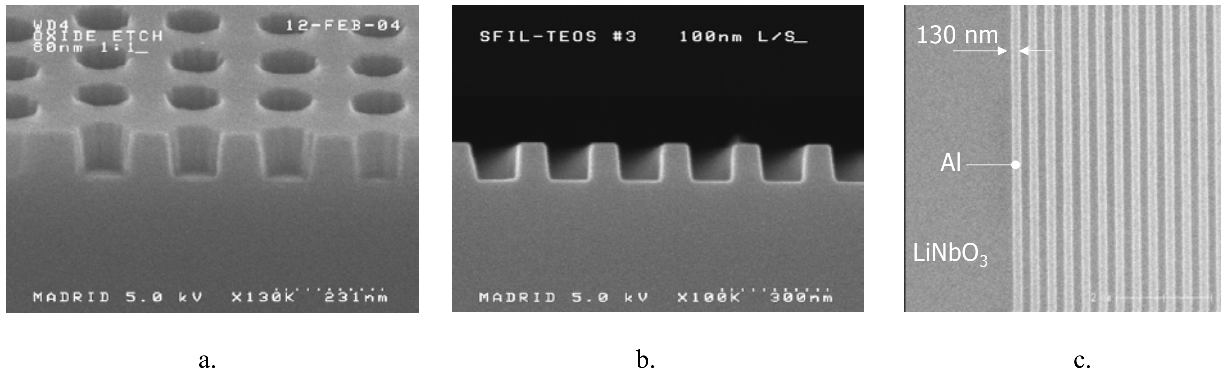


Figure 1. a) Etch barrier is dispensed onto the substrate; b) compress and UV cure; c) imprinted feature leaving a residual layer.

As with other NGL technologies, S-FIL has its share of technical problems to overcome to be considered as a production-worthy lithography method. Issues such as defects, critical dimensions (CD), residual thickness, and template inspection must be solved. In addition, a reliable pattern transfer to the underlayer substrate must also be demonstrated. Recent work has focused on the development of an NH_3-based plasma etch process to create features suitable for etching the underlying layers[7]. Figure 2a) depicts pattern transfer in underlayer oxide of 80 nm vias and (b) 100 nm line/space features. Also, using the NH_3 baseline etch process, (c) the world's first surface acoustic wave correlator devices on 100-mm diameter z-cut $LiNbO_3$ substrates using S-FIL technology were fabricated[8]. The purpose of this work is to present a processing scheme suitable for lift-off processing using S-FIL technology. There are several attributes in using a lift-off method; one of which we find attractive is the ability to deposit non-volatile materials such as copper, gold, platinum, etc., without the worry for an etch process. In order to develop this process, several problems must be overcome. These include obtaining an etchable hardmask that would adhere to the etch barrier imaging material and establishing a selective etch process to maintain the proper undercut require for metal deposition and solvent lift-off. The results from the lift-off material stack with and without a "glue" layer development work will be shared.



a. b. c.

Figure 2. a) 80 nm 1:1 pitch vias in oxide with a sidewall slope angle of ~ 80 °; b) 100 nm 1:1 line/space features in oxide; c) patterned 130 nm Al lines on $LiNbO_3$ substrates.

2.0 EXPERIMENTAL

In order to fabricate wafers for the lift-off studies, a layer of 2000 Å thick MicroChem polymethylglutarimide (PMGI) is first spin-coated on 200 mm double-sided polished silicon wafers using an SVG90S coater. The wafers are then vacuum-baked for 12 hours (240 °C) to drive off solvents. Next, a masking layer such as TEOS is deposited using a Novellus C-1 system; this is followed by a spin-coated thin adhesion layer of Brewer Science DUV30J anti-reflective coating (ARC). And finally, a proprietary Si-containing acrylate-based etch barrier monomer imaging material is dispensed at the point of use at each die location, and the dies are printed using an Imprio-100 tool manufactured by Molecular Imprints, Incorporated.

Etching of the entire material stack was performed in a semi-custom Unaxis Versalock 700 (VLR) system. The breakthrough etch of the residual etch barrier layer and hardmask was accomplished using a fluorine-based high pressure (30-90 mT) and high bias (50-300 W) recipe. The undercut etch of the PMGI is done with an oxygen-based RIE process with low pressure (10-30 mT) and low bias (5-50 W). While the breakthrough etch process is timed, the PMGI undercut process monitoring is conducted using a spectrometer-based (200-800 nm wavelength range) endpoint system. Metal deposition of Al or Ti/Au is deposited by means of an evaporation method on a Temescal 1800 tool. Shipley SVC-14 solvent was used for all lift-off processing. CD measurements and cross-sectional SEMs were done on a Hitachi S-4500 system.

3.0 RESULTS AND DISCUSSION

3.1 S-FIL Lift-off Process

While optical-based lithography lift-off processes have been proposed which use from one to three layers of resist[9-11], Figure 3 shows the S-FIL lift-off material stacks without a glue layer (a) and with a glue layer (b) that are currently being pursued. In this system, the top layers typically consist of a masking layer and an etch barrier imaging layer, and the undercut layer is PMGI. In the case of the glue layer stack, a thin layer, which is typically ARC, is required between the EB and the hardmask since the EB materials do not adhere well to most dielectric materials such as oxide or nitride.

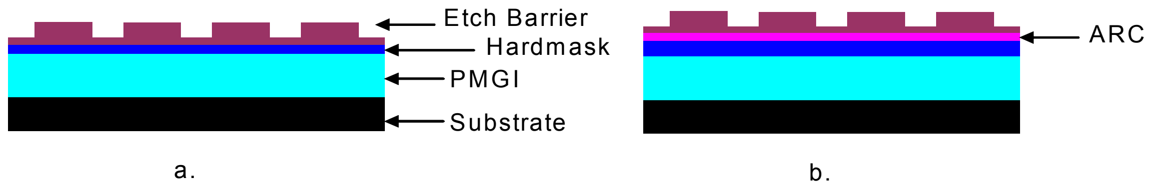


Figure 3. a) S-FIL material stack with no glue layer; b) S-FIL material stack with a glue layer

The fundamental requirement for a successful lift-off process is the creation of a re-entrant resist profile. Figure 4 illustrates a step by step cartoon of the S-FIL lift-off process. In creating the undercut profile, the first step is to perform a breakthrough etch stopping on PMGI (a), followed by a selective process to establish the undercut in PMGI (b). The desired metals such as Al or Ti/Au are deposited (c). And finally, a solvent lift-off is used to dissolve the PMGI while lifting the excess metal, leaving the isolated metal features (d).

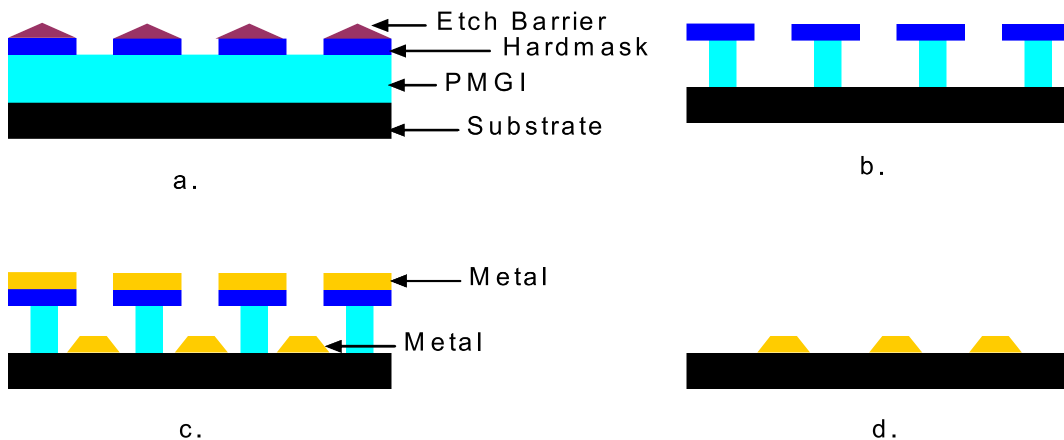
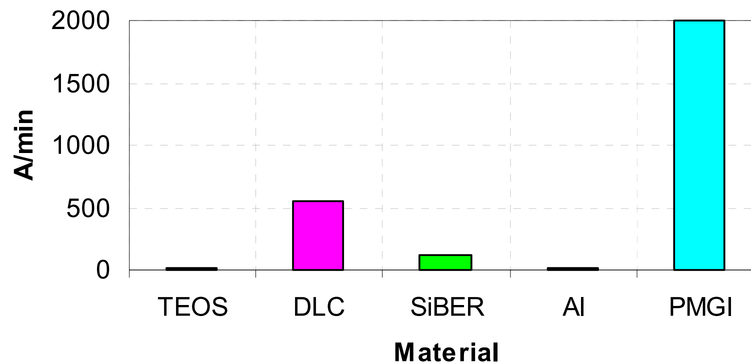


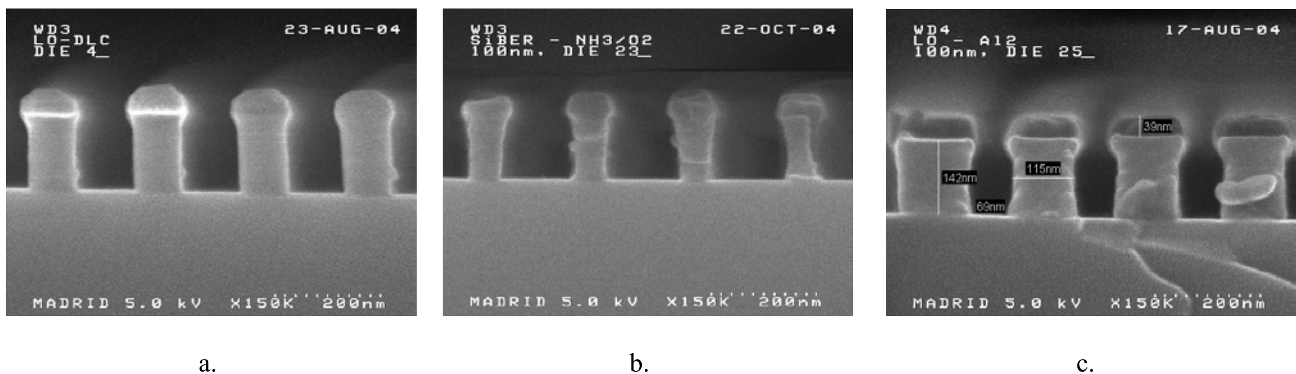
Figure 4. a) S-FIL breakthrough etch; b) S-FIL undercut profile; c) metal deposition; d) lift-off leaving isolated features

3.2. Lift-off Results of no glue layer

The initial development work was done using a material stack without a glue layer scheme. As a starting point, we utilized the NH_3 baseline process established for the subtractive S-FIL work due to its compatibility with the EB. Selectivity of various hardmask materials such as DLC (diamond-like carbon), SiBER, aluminum, and oxide were gathered. Graph 1 shows the blanket etch rate result of PMGI in comparison to various hardmasks. As shown, selectivity of PMGI to both oxide and Al were almost infinite (> 2000:1), while the selectivity to DLC (4:1) and SiBER (17:1) were marginal. With the exception of the DLC, the other materials are well within the desired selectivity of greater than 10:1 (PMGI: hardmask), and therefore, a good initial point for development. Figures 5a, 5b, and 5c, depict the results of DLC, SiBER, and Al, respectively, after PMGI undercut. Although the selectivity is sufficient, definite anomalies were observed. From the various hardmasks used, the DLC material yielded the most promising results; however, as can be seen from SEM, rounding of the features is observed before an undercut profile was achieved. Feature roughness and poor feature fidelity along with CD bias were unsatisfactory with the SiBER and Al materials as well. The final attempt was to try the oxide hardmask, but it was found that the adhesion of the EB to the oxide was poor and a different strategy needed to be implemented.



Graph 1. Graph showing blanket etch rates of various hardmask materials with PMGI to measure selectivity.



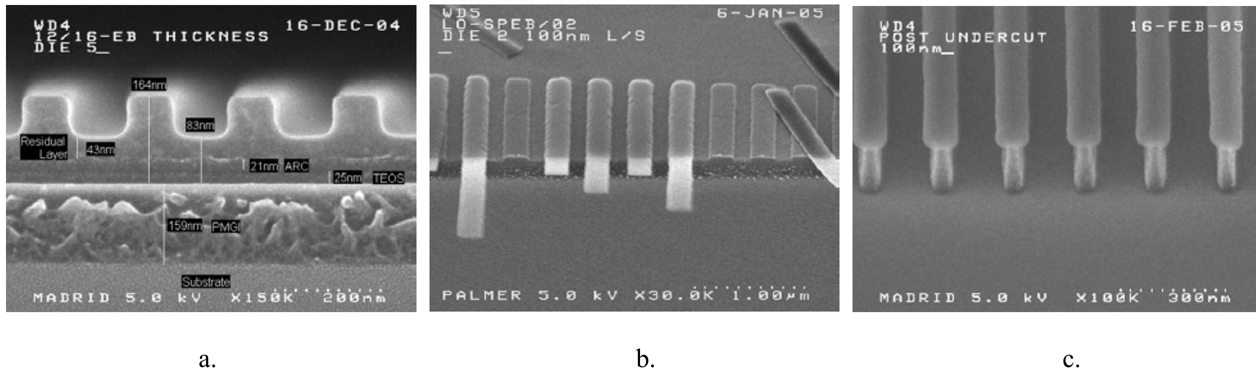
a. b. c.

Figure 5. a) SEM cross-section of DLC hardmask depicting rounding of features; b) SiBER hardmask showing gross sidewall roughness and feature degradation; c) Al hardmask depicting poor CD bias.

3.3 Lift-off Results with a glue layer

Based on the poor results obtained for the no glue layer development approach, our next attempt was to shift to a more well-known conventional oxygen-based process to establishing the undercut profile in PMGI. Knowing that the oxygen process is not compatible with the current EB material, and the oxide is very selective in an oxygen-based plasma environment, an oxide hardmask makes a logical choice. A selectivity of greater than 2000:1 (PMGI: oxide) was measured using one of our in-house oxygen RIE processes. In order to use the oxide hardmask though, several issues needed to be overcome. The first obstacle was to see how we can imprint features and still be able to employ oxide. In addressing this hurdle, a thin (~ 30 nm) glue layer was implemented between the EB and oxide. Figure 6a) illustrate the glue layer stack post imprint. The next issue was to establish a breakthrough etch to clear the residual, ARC, and oxide layers while maintaining feature fidelity. Taking into account the residual layer and ARC thicknesses of about 40 nm and 30 nm, respectively, and given the poor selectivity of oxide to EB of about 1:1; it was estimated that a thin oxide layer of

approximately 30 nm would be sufficient to pattern transfer using the CF_4/O_2 breakthrough baseline process. As shown in figure 6b), a timed etch of around 80 seconds was required to breakthrough the top layers, defining the features and stopping on PMGI. Evidence of sidewall roughness was observed, but this may be inherited from the imprinting template itself. To create the undercut profile, a low pressure, low bias RIE oxygen process was used to establish an undercut of approximately 35 nm per side on 100 nm features as shown in figure 6c).



a. b. c.

Figure 6. a) SEM cross-section of a glue layer stack showing the oxide hardmask, ARC , and residual layer; b) top down of the 100 nm line/space features post breakthrough etch; c) cross-section showing an undercut of approximately 35 nm per side in PMGI.

3.4 S-FIL Lift-off SAW Device Results

The lift-off process demonstrated for the 100 nm line/space features were used to fabricate a SAW structure. The SAW pattern consists of an interdigitated transducer (IDT) of 140 nm lines and 190 nm spaces. Figure 7 shows top down (a) and cross-sectional SEMs (b) post Al metal deposition, and the completion of a solvent lift-off leaving the isolated Al metal features of about 40 nm thick (c). To compare surface roughness of the Al features (~ 20 nm), several additional wafers were processed using evaporated Ti/Au. Figure 8 depicts a smoother surface roughness (~ 5 nm) using Ti/Au (a) and cross-sections of the metal lines at 50 nm thick (b) and 90 nm thick (c).

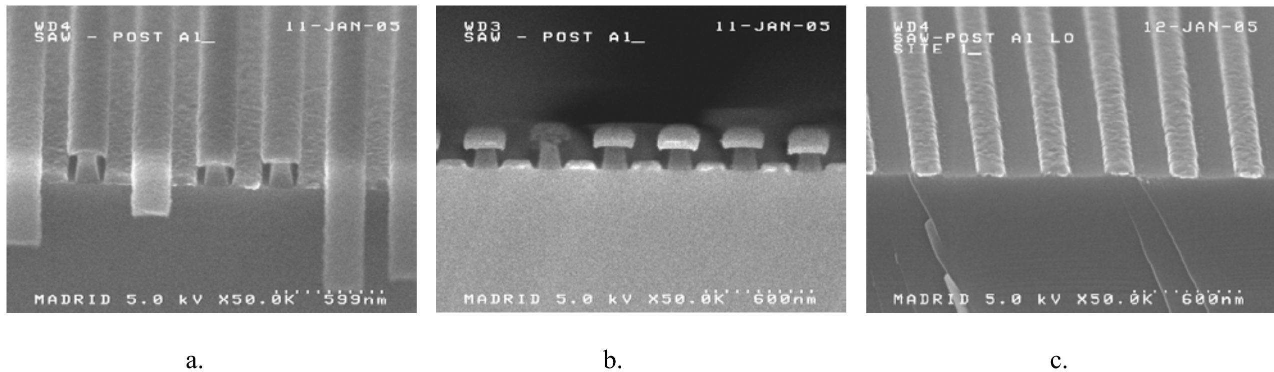


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Figure 7. a) Top down SEM showing post Al metal deposition; b) cross-section depicting post Al deposition; c) Al metal features post solvent lift-off.

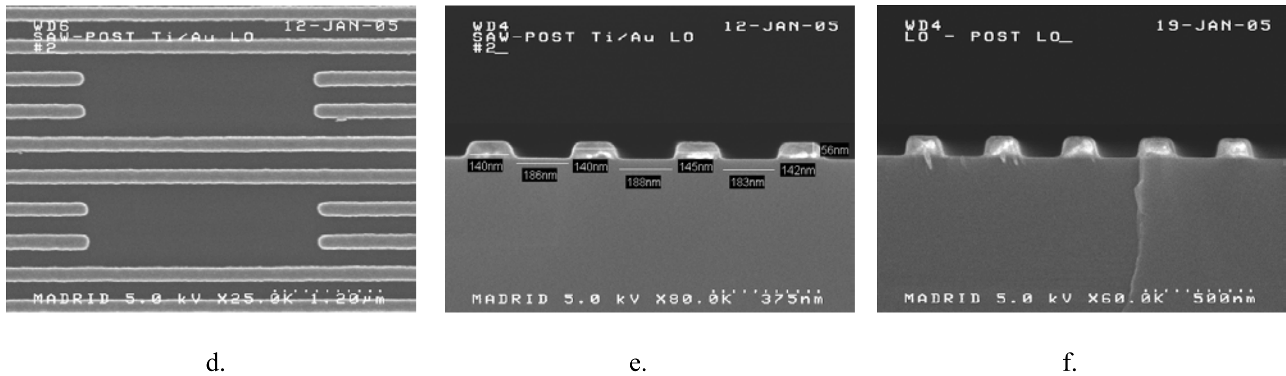

Figure 8. a) Top down SEM showing post Ti/Au metal deposition; b) cross-section of 50 nm thick Ti/Au metal features; c) cross-section of 90 nm thick Ti/Au metal features.

4.0 CONCLUSION

A feasibility study of a lift-off process with the use of Step and Flash Imprint Lithography (S-FIL) glue layer stack has been done. This glue layer stack which integrates a thin layer of a developable anti-reflective coating (ARC) applied between the etch barrier and the oxide allows for a different processing methodology. In incorporating the oxide as a hardmask, the current etch barrier imaging resist was no longer a factor; and thereby, a more conventional reactive-ion-etch oxygen-based process can be used to achieve the undercut profile. The results have demonstrated feasibility in creating an undercut of 30 nm per side with a re-entrant profile suitable for lift-off of 100 nm dense 1:1 lines/spaces. The final process was incorporated to fabricate the surface acoustic wave (SAW) device pattern on silicon wafers. Although the lift-off process has shown capabilities down to the 100 nm node, the development work reveals possible challenges with pursuing high aspect ratio sub-nanometer resolution beyond 70 nm due to features collapsing. Future development work will need to focus on understanding these limitations and possible alternative techniques such as S-FIL reverse-tone (SFIL/R) process to mitigate these concerns.

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