S-FIL™ Technology: Cost of Ownership Case Study

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Abstract

The escalating costs of lithography for the sub 90nm regime have been well documented. The semiconductor industry is exploring evolutionary improvements to existing photolithographic techniques as well as disruptive, but cost effective patterning technologies for the demanding high-resolution requirements.

Step and Flash Imprint Lithography (S-FIL™) is an innovative patterning technology commercialized by Molecular Imprints. S-FIL has demonstrated the capability to pattern very high-resolution features and has been recognized as an NGL candidate by inclusion on the ITRS Roadmap in December 2003. This paper describes the S-FIL process and examines its comparative cost of ownership relative to conventional photolithography at the 90nm node and to immersion photolithography at the 65nm node for patterning contacts and dual damascene.

Introduction

Historically, the lithography technology of choice has been photolithography. The minimum feature size (F) in photolithography is given by: $F = (k_1)(\lambda)/NA$. Here λ is the exposure wavelength, NA is the numerical aperture of the lens system in the photolithography tool with typical values of 0.5 to 0.8, and k_1 is a process related term with typical values of 0.4 to 0.7. The reduction of F has been achieved by periodically going to smaller and smaller exposure wavelengths. Photolithography has been operating at a deep UV wavelength of $\lambda = 248$ nm, while $\lambda = 193$ nm has been in production more recently and the near future appears to welcome 193nm immersion photolithography which has been in beta testing [1].

Until a few years ago $\lambda = 157$ nm was being investigated along with extreme ultraviolet lithography (EUV), which operates at $\lambda = 13.2$ nm. This continuous reduction in wavelength combined with highly sophisticated designs of lenses and mirrors, design of advanced and complex masks, innovation in materials, processes, and precision machines has enabled sub-100nm lithography. However, with shorter wavelengths, there are long lists of new and substantial technical challenges. For instance, fused silica has been the established lens material in optical lithography. But, fused silica is not transparent at 157 nm. Therefore, the 157 nm research efforts were focused on using CaF_2 as the lens material, which led to significant original research problems with respect to manufacturing sufficient quantities of high-purity CaF_2 and circumventing the high level of birefringence that is characteristic of this material. At $\lambda = 13.2$ nm, there are no known transparent materials; therefore, all the optical systems and photo masks are based on reflective optics. Further, obtaining a source with sufficient power at this EUV wavelength is still an open problem. High-resolution e-beam lithography techniques,

though very precise, are too slow for high-volume commercial applications. They are believed to be best suited for directly writing photo masks used in photolithography.

In the interim, 193nm immersion photolithography has emerged as a very high potential technology contender at the 65 nm node. In immersion lithography, a liquid is interposed between an exposure tool's projection lens and the wafer. Immersion technology offers the opportunity for better resolution over conventional projection lithography because the lens can be designed with NAs greater than one, thus creating the ability to produce smaller features.

The Exponential Cost of Going Smaller

It is not physical limits, but prohibitive costs that are likely to make the traditional photolithography approach of decreased wavelength impractical. Even today, optical lithography is an extremely expensive unit process. Historically, the cost of optical exposure tools has increased exponentially (see Figure 2). Even if fundamental challenges are overcome at λ = 157 nm and 13.2 nm, it is believed that the historical exponential increase in tool cost could become even steeper.

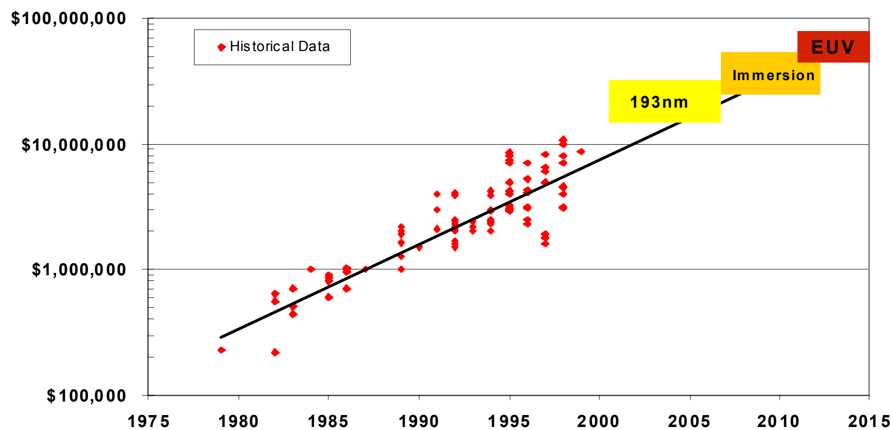

Figure 2: Exponential Increase in the Cost of Lithography Tools[1]

Preliminary list price estimates for a EUV prototype/alpha tool expected to be ready by 2007 are $ 47 M with a throughput of 10 WPH [2]. In addition to the cost of the tool, the recurring and consumable costs associated with process materials, environmental control, complicated photomasks, etc. makes next generation lithography a high-risk proposition.

The only way to recover these costs is to have high throughputs and/or long tool lives and/or long photomask lives, and excellent feature fidelity within a field, between fields, and between wafers. While lithography was primarily developed by the silicon microelectronics industry, it is fast becoming a key unit process for other application areas such as micro-fluidic devices, optical switches, flat panel displays, and SAW devices. Emerging nano-resolution applications include sub-wavelength optical components, biochemical analysis devices, high speed compound semiconductor devices,

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[1] Source: S.V. Sreenivasan, C.G. Willson, *et al*. NIST-SPIE Conference on Nanotechnology, September 2002

distributed feedback lasers, photonic crystals, and high density patterned magnetic media for data storage. The above discussion clearly indicates that there exists a need for low-cost alternatives to nano-resolution photolithography. It is believed that if a sufficiently low cost lithography solution can be developed, it will provide a major competitive edge to manufacturers of traditional and emerging devices, and enable new kinds of devices that are currently not economical. The cost and complexity trends in photolithography have motivated Molecular Imprints, Inc. to investigate and develop a non-optical, low-cost lithography technique known as Step and Flash Imprint Lithography (S-FIL).

The S-FIL™ Technology

S-FIL technology was developed by a team supervised by Professors S.V. Sreenivasan and Grant C. Willson of the University of Texas at Austin. Molecular Imprints Inc. has exclusively licensed this technology from the University of Texas at Austin, and subsequently improved upon it. The process includes the use of a proprietary imprint fluid that serves the role of a resist in the S-FIL process. The S-FIL process has been well documented [3]. S-FIL involves imprinting sub-100 nm sized features on to a pre-planarized substrate using a template (mold). The template is usually manufactured from an industry standard mask blank made of fused silica using a phase mask process. The main difference being that the feature sizes on the template are 1:1 rather than 4:1.

Enhancements to the S-FIL process resulted in a new process called S-FIL/R, as described in [4]. The following figure illustrates the S-FIL and S-FIL/R process:

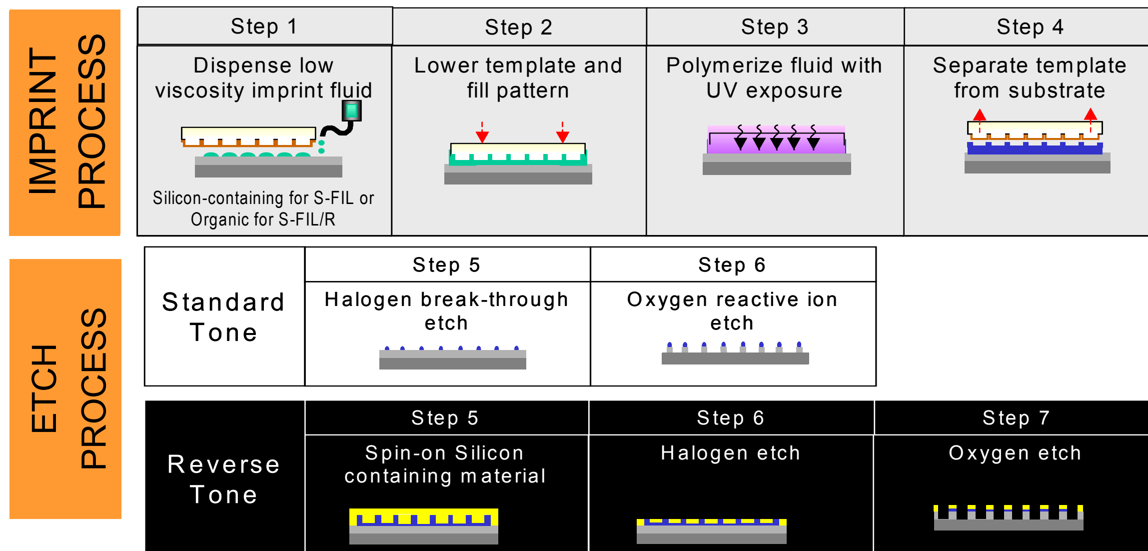


Figure 3: S-FIL and S-FIL/R Process Steps

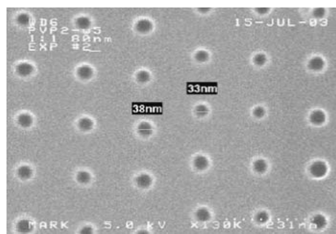
The S-FIL/R process enables good critical dimension control on wafers with moderate levels of topology. The transfer etching process is straightforward and does not involve any unusual gases or etch techniques. The advantages that S-FIL/R provides over S-FIL include the following i) Improved line-width control with no faceting at the line edges, ii) Improved critical dimension control over topography, iii) Formation of "T"-topped features suitable for lift-off processing and (iv) Improved etch resistance and selectivity during pattern transfer.

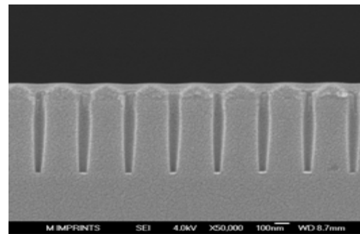
For the purposes of this paper, we have considered S-FIL/R process as the baseline process.

Cost of Ownership Analysis
Molecular Imprints has teamed up with Wright Williams & Kelly, Inc. (WWK), well known in the semiconductor industry for their industry standard software tools and expertise in calculation of cost of ownership. WWK's TWO COOL® software tool is used by OEMs, chip manufacturers, and others to develop a comprehensive cost of ownership model of semiconductor tools and processes.

S-FIL/R, despite being a new entrant in the field of semiconductor lithography, has generated strong interest. In 2003, the ITRS included imprint lithography on the roadmap [5]. Although this roadmap currently applies imprint lithography to the 32 nm node and beyond, Molecular Imprints believes that imprint technology offers possibilities in the immediate future.

One of the key demonstrated capabilities of imprint lithography has been the ability to imprint sub-100 nm contacts. Figure 4 below demonstrates results obtained by Molecular Imprints.





Sub-40 nm imprinted contacts *60 nm imprinted contacts etched into oxide*

Figure 4: Imprinted contacts using S-FIL and S-FIL/R

Another interesting ability of imprint technology is to be able to imprint multi-dimensional features such as the one shown below in Figure 5. This capability raises the possibility of imprinting a via-trench combination (2-tier template) in dual damascene patterning processes in a single step as opposed to 2 masks needed in photolithography. Figure 6 illustrates actual dual damascene process results using the 2-tier template in Figure 5.

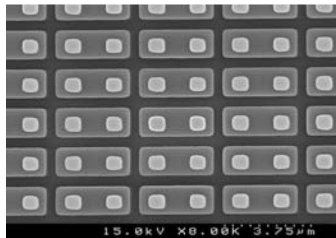


Figure 5: 2- tier imprint template for dual damascene [6]

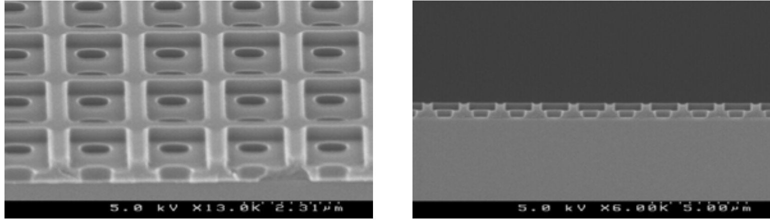


Figure 6: Dual damascene imprint results in dielectric [6]

The above two examples are considered in this paper to demonstrate the attractiveness of imprint technology from a cost of ownership perspective.

S-FIL vs. Conventional Photolithography at the 90nm node

The following assumptions were utilized for the cost of ownership study. Note, the values assumed for the imprint process are based on logical extensions of the current state of imprint technology offered by Molecular Imprints.

Parameter	Photolithography	S-FIL/R
Tool Price ($)	20 M	10 M
Installation Cost ($)	1 M	0.5 M
Mask/Template Price ($)	**62,500**	**25,000**
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
Wafer Size	300 mm	

Table I: Assumptions underlying the COO study for the 90 nm node

Note: In the above table tool price for photolithography equipment does not include resist coating/baking/developing equipment. Installation cost is estimated at 5% of equipment purchase costs and transportation costs are not included.

A key difference in the costs of the two technologies is the template/mask pattern generation cost. A template is anticipated to be lower in cost than a conventional photo mask because of the following reasons: the templates need no optical proximity correction (OPC). Pattern-writing time (a key cost driver for masks) is shorter by a factor of 4 for templates because of the smaller field sizes (1/16th the area of traditional photo masks). Also, templates have shorter pattern writing times because of smaller data-preparation files (no optical proximity correction factors). The template inspection is over a smaller area and hence lowers the cost. For conventional photo masks, even though they have an advantage of 4:1 reduction ratio, the write times are not short because the feature sizes attributed to MEEF and OPC are approximately 1.5 the actual feature size.

Contacts at the 90 nm Node

The first cost of ownership analysis investigates patterning of the metal layer 1 (M1) for a 4-layer DRAM device. Per the ITRS specifications, this layer is the most demanding in terms of the pitch. Photolithography techniques struggle with the pitch specifications

even at today’s 90 nm node levels. Memory device designers have to adhere to numerous design rules to avoid the so-called “forbidden pitch” ranges.

The main drivers of the cost of ownership, as revealed by the output from TWO COOL® software, are displayed in Table II below.

Dominant COO Components	Photolithography	S-FIL/R	Cost savings with S-FIL/R
Mask & Materials	$35.83	$14.67	59%
Equipment Depreciation	6.72	4.03	40%
Maintenance[2]	0.21	0.26	-24%
Labor	0.20	0.24	-20%
Total COO per wafer[3]	**$43.10**	**$19.37**	**55%**
COO (5,000 wafers/wk)	$44.96	$21.28	53%

Table II: COO drivers for 90nm contacts in DRAM metal layer 1

It is clear that the mask & materials costs and the equipment depreciation are the principal cost components of each technology. They are also the clear differentiators between S-FIL/R and photolithography. The above analysis shows a 55% reduction in cost using step and flash imprint lithography as opposed to photolithography.

A key advantage of imprint technology is its elimination of the “forbidden pitch” rule. Imprint lithography allows relaxation of some of the 2,000 additional design rules that must be implemented for reticle enhancement techniques and optical proximity correction that allow optical lithography to meet technology requirements [7]. These design rules add complexity, which in turn, add time and cost to chip designs and increase the probability of manufacturing problems. The design rules also increase the physical size of the chip, which leads to fewer die per wafer, lower yield and higher cost per chip. As an example, design rules that increase the die area 15% from 140 mm^2 to 150 mm^2 reduce the gross die per wafer by 7%, lower yield by 0.8%, and increase die cost by 8%.

Dual Damascene Process at the 90 nm Node

S-FIL/R also raises some very exciting possibilities for cost savings in the dual damascene process. By using a 2-tier template, S-FIL/R can imprint via and trench in a single lithography step. This provides a dual advantage in process cost and template cost. A cost of ownership analysis for dual damascene was conducted using TWO COOL® from WWK.

Except for the template cost, all assumptions remain the same as in Table I.

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[2] Assumes same Maintenance and Labor costs for each type of system

[3] At 100% utilization

Parameter	Photolithography	S-FIL/R
Tool Price ($)	20 M	10 M
Installation Cost ($)	1 M	0.5 M
Mask/Template Price ($)	**62,500 (1 for via and 1 for trench)**	**75,000 (2-tier template)**
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
Wafer Size	300 mm	

Table III: Assumptions underlying the COO study for the 90 nm node dual damascene process

Note: In both tables above tool Price for photolithography equipment does not include resist coating/baking/developing equipment. Installation cost is estimated at 5% of equipment purchase costs and transportation costs are not included.

A COO analysis for just the lithography steps using the TWO COOL software validates the significant cost advantage of the S-FIL/R for the dual damascene process over conventional photolithography. Nearly 50% reduction in cost is observed for the lithography steps as shown in Table IV below.

Photolithography		S-FIL/R	
Masking Step	COO	Imprint Step	COO
Metal Mask	$43.10	Metal/Via Imprint	$47.58
Via Mask	$43.10	--	--
Total Masking Costs	$86.20	Total Imprint Cost	$47.58

Table IV: COO for the masking/ imprinting steps in a 90nm node dual damascene process

While the above analysis considers only the lithography steps, it is essential to examine the impact of integrating imprint lithography into the complete dual damascene process. To compare process costs, WWK's Factory Commander® was used to examine the Metal 1/Metal 2/Via 2 sequence for 5,000 wafers per week from an example process.

Developed with Sandia National Laboratories, Factory Commander® is a Cost and Resource Evaluation software platform that can be applied to any discrete manufacturing or assembly operation. It performs high-level cost analyses of overall factory and individual product costs, manufacturing capacity, and revenues. Note, all measurement and inspection steps have been excluded in this comparison between photolithography and S-FIL, but building depreciation has been included, which was excluded in the previous TWO COOL® COO examples. Table V compares processes and Table VI compares COO cost drivers.

Photolithography Process	COO	S-FIL/R Process	COO	Comments
Deposit ILD	$9.29	Deposit ILD	$10.62	
		BARC	3.70	Photolithography may not require BARC
Backside Clean	3.50	Backside Clean	3.63	
Metal 1 Mask	51.16	Metal 1 Imprint	31.99	Includes resist coat and develop
		Spin Silicon	8.27	S-FIL/R specific process step
Etch Channel	4.21	Etch Channel	4.48	
Ash	1.48	Ash	2.16	
Barrier/Liner/Seed	20.53	Barrier/Liner/Seed	21.57	
Cu Deposit	4.68	Cu Deposit	4.91	
CMP	11.26	CMP	11.66	
Post CMP Clean	2.23	Post CMP Clean	2.35	
Low K Dielectric Deposit	9.29	Low K Dielectric Deposit	10.62	
Etch Stop	20.53			
ILD	9.29	BARC	3.70	Photolithography process may require BARC (not shown)
Backside Clean	3.50	Backside Clean	3.63	
Metal 2 Mask	51.16	Metal 2 Imprint	51.74	S-FIL/R uses 2-Tier template
		Spin Silicon	8.27	S-FIL/R specific process step
Etch Channel	4.21	Etch Channel	4.48	
Ash	1.48	Ash	2.16	
Backside Clean	3.50	Backside Clean	3.63	
Via 2 Mask	51.16			Photolithography process step
Etch Nitride	8.76			
Etch Via	5.97	Etch	9.30	
Ash	1.48			
Backside Clean	3.50			
Barrier/Liner/Seed	20.53	Barrier/Liner/Seed	21.57	
Cu Deposit	4.68	Cu Deposit	4.91	
CMP Cu	11.26	CMP Cu	11.66	

Table V COO for 90nm node dual damascene with complete process steps

Note: The extra masking step and related differences imply that the photolithography process has different equipment utilization factors than the S-FIL/R process. This may result in a lower COO per step, but with more steps, the process has a higher total COO.

Driver	Photolithography	S-FIL/R	Cost savings advantage with S-FIL/R
Mask & Materials	$127.33	$83.63	34%
Equipment Depreciation	117.49	94.70	19%
Building Depreciation	47.27	47.23	0%
Maintenance	22.18	12.12	45%
Labor	4.38	3.33	24%
COO (5,000 wafers/wk)	**$318.64**	**$241.02**	**24%**

Table VI: COO Drivers for complete 90nm node dual damascene Process

For the 90 nm node dual damascene process, due to the reduced difference between the costs of the template and photo mask, the impact on COO of S-FIL/R is diluted but still delivers an improvement of 24%.

S-FIL/R vs. 193nm Immersion Photolithography at the 65nm node
S-FIL/R offers a larger COO advantage at the 65nm node than at the 90nm node because template price is less sensitive to changes in the feature sizes for the contacts/via/trench. As explained earlier, S-FIL/R templates do not require any optical proximity corrections, since the S-FIL/R process exactly replicates the templates. On the other hand, photo masks do need OPCs and other correction factors that significantly increase the cost of the photo mask in moving from a 90 nm to a 65 nm process.

As shown in Tables VII and VIII below, at the 65nm node, the COO savings are even greater with the S-FIL/R process, which exhibit a 68% savings for contacts and 61% savings for the dual damascene process. This improvement is primarily driven by the lower template costs.

Contacts at the 65 nm Node

Parameter	**Photolithography**	**S-FIL/R**
Tool Price ($)	25 M	10 M
Installation Cost ($)	1 M	0.5 M
Mask/Template Price ($)	100,000	27,500
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
Wafer Size	300 mm	
COO	**$65.86**	**$20.78**

Table VII: Assumptions underlying the COO study for the 65 nm node

Dual Damascene Process at the 65 nm Node

Parameter	**Photolithography**	**S-FIL/R**
Tool Price ($)	25 M	10 M
Installation Cost ($)	1 M	0.5 M
Mask/Template Price ($)	**100,000 (1 for via and 1 for trench)**	**82,500 (2-tier template)**
Effective Throughput (WPH)	60	50
Mask/Template Usage	2000 wafers	2000 wafers
Wafer Size	300 mm	
COO	**$131.72**	**$51.81**

Table VIII: COO for 65nm node dual damascene with complete process steps

Note: In both tables above tool Price for photolithography equipment does not include resist coating/baking/developing equipment. Installation cost is estimated at 5% of equipment purchase costs and transportation costs are not included.

Sensitivity Analysis
One primary issue in calculating COO is the assumptions associated with materials and template/mask costs, throughput, and process life of an emerging technology like imprint lithography. While a strong effort has been made in this paper to accurately represent the COO of S-FIL/R that is consistent with the current state of the technology, it is prudent to investigate the sensitivity of the COO model, with respect to certain key factors including imprint template price, template usage, and tool throughput.

Sensitivity Analysis: Varying S-FIL/R Template Price for 90nm node Contacts
A sensitivity analysis varying the template price from $ 5000 to $ 100,000 is conducted for the contacts scenario (i.e. single template scenario).

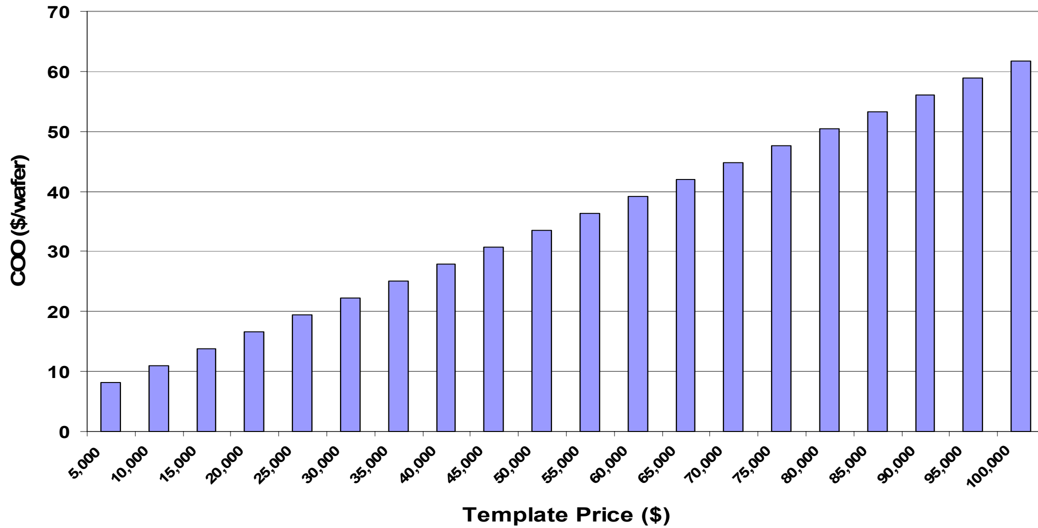

Figure 7 Impact of template price variation on COO of S-FIL/R for 90nm node contacts

It is clear that the template cost plays a crucial role in the COO of S-FIL/R. However the above illustration raises several interesting possibilities. At low template pricing (e.g. assuming minimal inspection), the possibility of using S-FIL/R for generating prototypes of new chip designs for validation as well experimenting with new devices at smaller node levels would be immense. Quick turnaround of prototype designs at low cost can considerably shorten time to market for new products. This could result in significant benefits to companies, in terms of competitive advantages not accounted for in the COO calculation.

Sensitivity Analysis: Varying S-FIL/R Template Usage for 90nm node Contacts

A sensitivity analysis varying the template usage from 500 wafers to 3000 wafers is conducted for the 90 nm contacts scenario (i.e. a single tier template).

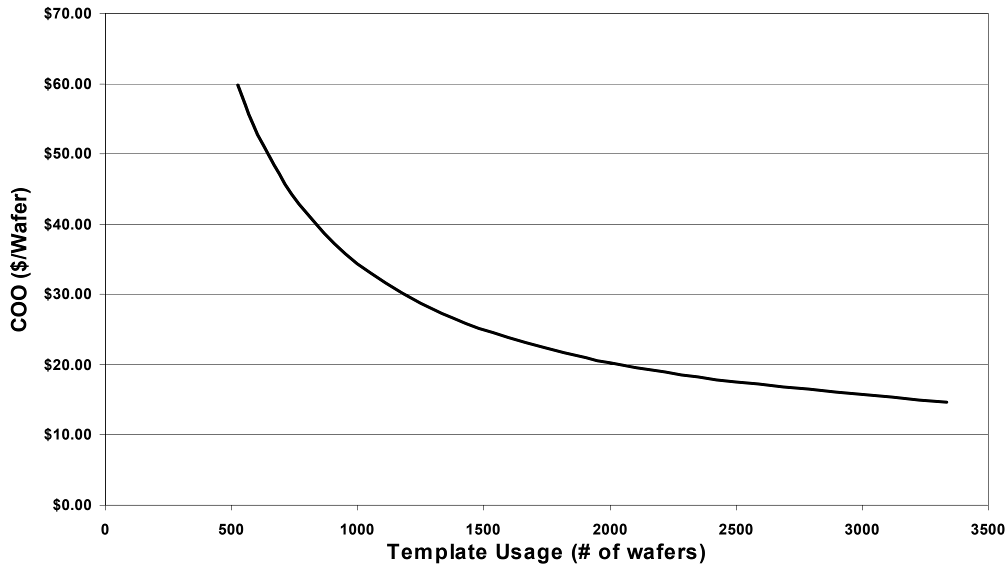

Figure 8: Effect of template usage on COO of S-FIL/R for the 90nm contacts

Even at low template usage estimates, the COO of imprint technology is very attractive. In recent years, low volume applications such as ASICs have lost ground to more standardized designs such as FPGAs and hybrid ASICs. The primary reason for the decrease in ASICs is attributed to the high non-recurring engineering costs coupled with the high cost of manufacturing, such as the high cost of masks and photo tools. However, disruptive lithography technologies like S-FIL/R can make such applications attractive once again.

Sensitivity Analysis: Varying S-FIL/R Tool Throughput for 90nm node Contacts

A sensitivity analysis varying the SFIL/R tool throughput from 5 WPH to 100 WPH is conducted for the 90nm node contacts scenario (assuming 300mm wafer size). As the S-FIL/R tool throughput is varied, the tool price is also adjusted to reflect any additional cost of satisfying the required throughput specification.

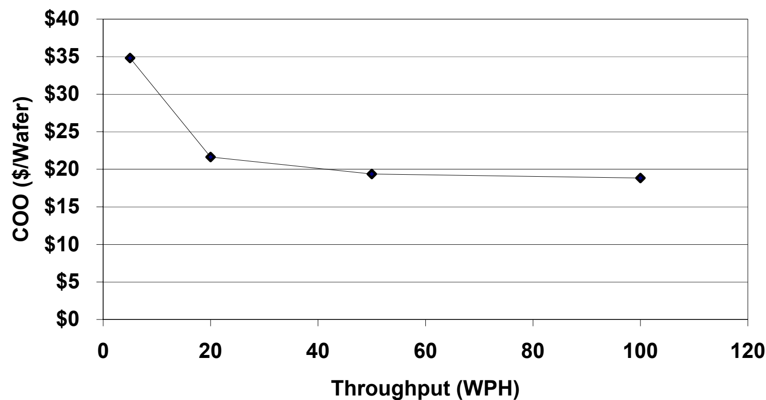

Figure 9 Influence of S-FIL/R tool throughput on COO for 90nm node Contacts

The COO of S-FIL/R is still very attractive at low throughputs, thus providing a significant advantage for applications such as chip prototyping and R&D. Also, at higher S-FIL/R tool throughputs (>20 WPH), the COO savings is significant. The results in the above plot demonstrate that S-FIL/R can provide immense value as it evolves from lower throughput, prototyping-oriented tools to higher throughput, production ready tools.

Conclusions

The paper demonstrates the advantage that step and flash imprint lithography provides in terms of COO over competing photolithography techniques, especially in the sub-90 nm node regime for applications such as contacts and dual damascene processes. Using COO sensitivity analyses around uncertain cost parameters, the authors show that S-FIL is an attractive lithography technology for high-resolution applications.

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