Imprint Lithography: Lab Curiosity or the Real NGL?

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ABSTRACT

The escalating cost for Next Generation Lithography (NGL) tools is driven in part by the need for complex sources and optics. The cost for a single NGL tool could exceed $50M in the next few years, a prohibitive number for many companies. As a result, several researchers are looking at low cost alternative methods for printing sub-100 nm features. In the mid-1990s, several research groups started investigating different methods for imprinting small features. Many of these methods, although very effective at printing small features across an entire wafer, are limited in their ability to do precise overlay. In 1999, Willson and Sreenivasan discovered that imprinting could be done at low pressures and at room temperatures by using low viscosity UV curable monomers. The technology is typically referred to as Step and Flash Imprint Lithography (S-FIL). The use of a quartz template enabled the photocuring process to occur and also opened up the potential for optical alignment of the wafer and template. This paper traces the development of nanoimprint lithography and addresses the issues that must be solved if this type of technology is to be applied to high-density silicon integrated circuitry.

Keywords: Step, Flash, Imprint, Lithography, NIL, UV-NIL

1. INTRODUCTION

In the fields of micro and nanolithography, major advancements in resolution have historically been achieved through use of shorter wavelengths of light. Using phase shift mask technology, it has already been demonstrated that 193 nm photolithography can produce sub-100 nm features. Along this path, such improvements come with an ever increasing cost for photolithographic tools. It is interesting to note that the cost of photo tools has kept pace with data density, as depicted in Figure 1. As conventional projection lithography reaches its limits, Next Generation Lithography (NGL) tools may provide a means to further pattern shrinks, but are expected to have price tag that is prohibitive for many companies.

The development of both light sources and optics to support the sources are primarily responsible for the rise in the cost of an NGL tool. 157 nm lithography, for example, requires the use of CaF_2 as a lens material. In the case of extreme ultra violet lithography (EUVL), no source with sufficient output has yet been identified that will meet the industry's throughput requirements.

Imprint lithography is essentially a micromolding process in which the topography of a template defines the patterns created on a substrate. Investigations by this group and others in the sub-50nm regime indicate that imprint lithography resolution is only limited by the resolution of the template fabrication process. It possesses important advantages over photolithography and other next generation lithography (NGL) techniques since it does not require expensive projection optics, advanced illumination sources, or specialized resist materials that are central to photolithography and NGL technologies. There are three basic approaches to imprint lithography. Each technique is depicted in Figure 2 and is briefly described below.

Soft Lithography generally refers to the process of transferring a self-assembled monolayer using a flexible template (see Figure 2a). Whitesides et al. have formed a template by applying a liquid precursor to polydimethylsiloxane over a

master mask produced using either electron beam or optical lithography.[1] The liquid is cured, and the PDMS solid is peeled away from the original mask. The PDMS template can then be coated with a thiol solution, which is subsequently transferred to a substrate, coated with a thin layer of gold. To prevent adhesion between the master and daughter masks, the master surface is passivated by the gas phase deposition of a long-chain, fluorinated alkylchlorosilane $(CF_3(CF_2)_6(CH_2)_2SiCl_3)$. The fluorosilane reacts with the free silanol groups on the surface of the master to form a Teflon-like surface with a low interfacial free energy. The passivated surface acts as a release layer that facilitates the removal of the PDMS stamp from the master.
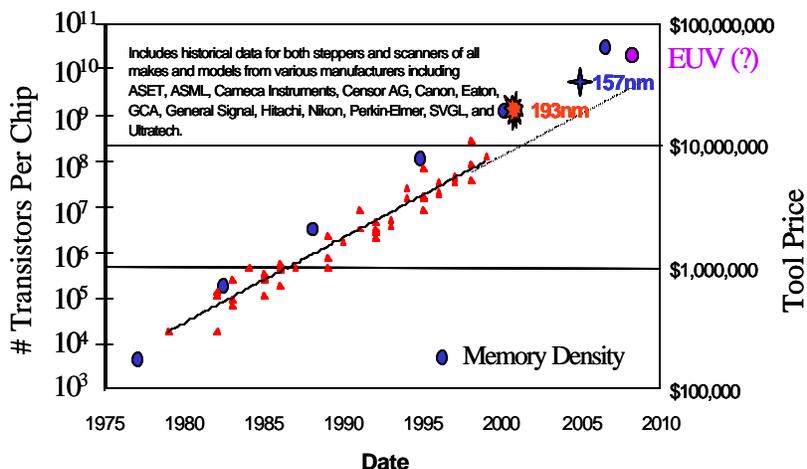

Figure 1. Transistor density and tool cost as a function of time.

Because the PDMS is easily deformable, the technology is not well suited for devices requiring precise pattern placement. Nanoimprint Lithography (NIL), developed by Chou et al. uses a solid mold, such as silicon or nickel.[2] The imprint process is accomplished by heating a resist above its glass transition temperature and imparting a relatively large force to transfer the image into the heated resist (see Figure 2b). To minimize adhesion between the resist and the mold, a fluorinated material is typically added to the resist. Features as small as 10 nm have been imaged using NIL. In addition, a variety of different devices have been fabricated by a number of different researchers using this approach.
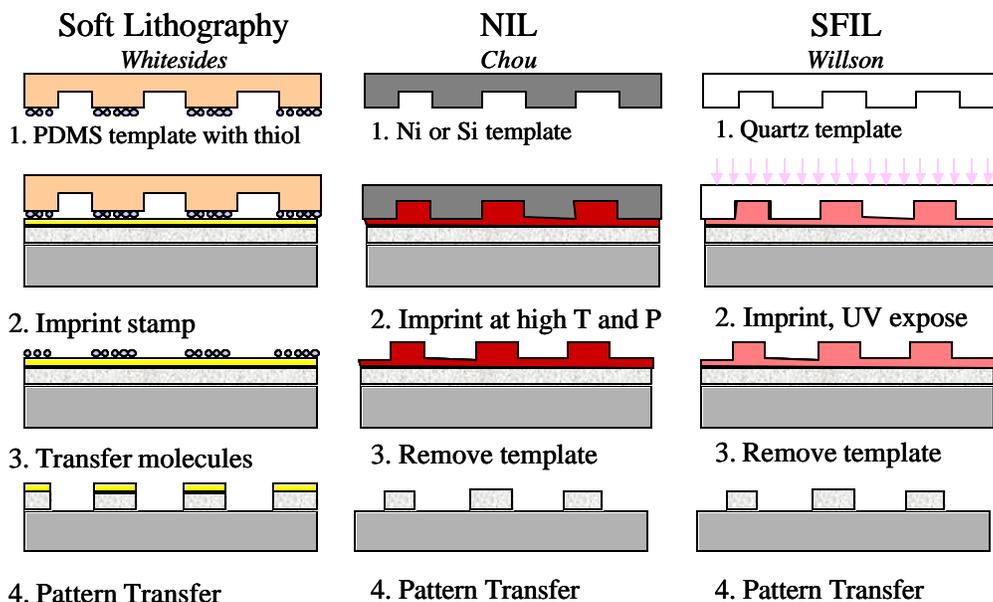

Figure 2. Fabrication sequence for three different varieties of imprint lithography.

Devices that require several lithography steps and precise overlay will need an imprinting process capable of addressing registration issues. A derivative of NIL, ultra violet nanoimprint lithography (or UV-NIL) addresses the issue of alignment by using a transparent template, thereby facilitating conventional overlay techniques (see Figure 2c). In addition, the imprint process is performed at low pressures and at room temperature, which minimizes magnification and distortion errors. Two types of approaches are being considered for UV-NIL. The first method uses conventional spin-on techniques to coat a wafer with a UV curable resist.[3] Although it is possible to uniformly coat the wafer, there are concerns that the viscosity of the resist will be too high to facilitate the formation of very thin residual layers. If the residual layer is too thick, the critical dimension (CD) uniformity may suffer as a result of the subsequent pattern transfer process. This problem is addressed by locally dispensing a low viscosity resist in a single stepper field. This second approach was first disclosed by Willson et al. in 1999 and is generally referred to as Step and Flash Imprint Lithography, or S-FIL.[4]

S-FIL appears to be the most suitable imprint technique for fulfilling the stringent requirements of silicon IC fabrication. The purpose of this paper is to summarize the progress made in S-FIL. Because a tool, a template , and a resist are necessary for the fabrication process, each of these subjects is discussed in detail. Following this discussion, open issues, such as defects, overlay, and planarization are discussed.

2. THE S-FIL TOOL

Imprint lithography relies on the parallel orientation of imprint template and substrate. Inaccurate orientation may yield a layer of cured etch barrier that is nonuniform across the imprint field. It is thus necessary to develop a mechanical system whereby template and substrate are brought into co-parallelism during etch barrier exposure. This was originally achieved in S-FIL by way of a two-step orientation scheme. In step one, the template stage and wafer chuck are brought into course parallelism via micrometer actuation. The second step uses a passive flexure-based mechanism that takes over during actual imprint.[5,6]

The first step-and repeat system was built at the University of Texas in Austin by modifying 248 nm Ultratech stepper that was donated by IBM (see Figure 3a). Key system attributes include:

- ?? a micro-resolution z-stage that controls the average distance between the template and the substrate and the imprinting force

- ?? an automated x-y stage for step-and-repeat positioning

- ?? a pre-calibration stage that enables parallel alignment between the template and substrate by compensating for orientation errors introduced during template installation

- ?? a fine-orientation flexure stage that provides a highly accurate, automatic parallel alignment of the template and wafer to the order of tens of nanometers across an inch

- ?? a flexure-based wafer calibration stage that orients the top of the wafer surface parallel with respect to the plane of the x-y stage

- ?? an exposure source that is used to cure the etch barrier

- ?? an automated fluid delivery system that accurately dispenses known amounts of the liquid etch barrie r; and load cells that provide imprinting and separation force data.

A commercialized version of an S-FIL tool is now available from Molecular Imprints Inc (MII). It is interesting to note that although nanoimprint lithography is still in the early stages of development, there are several vendors that are now offering imprint tools. In addition to Molecular Imprints, EVGroup (Austria), Nanonex (U.S.), Obducat (Sweden), and Suss Microtec (Germany) have systems ready for purchase. This is quite different from previous NGL development efforts in which a vendor only becomes interested in building a system after the technology matures to some degree.

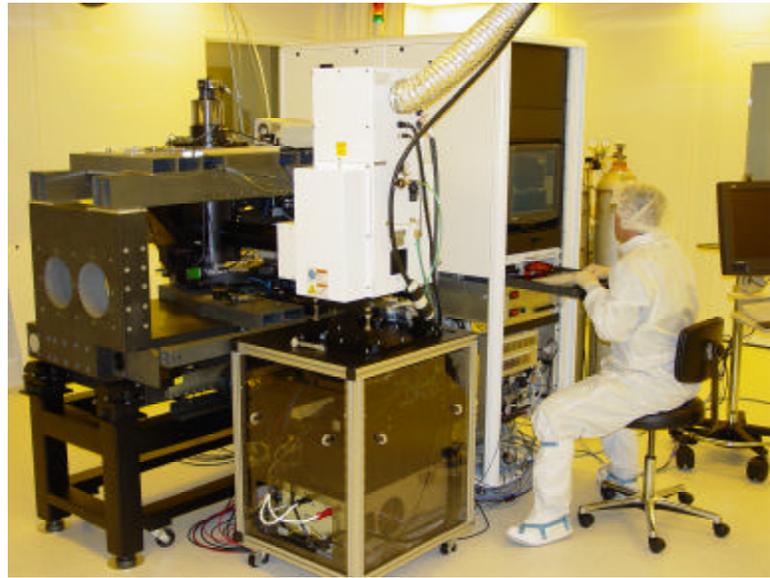Figure 3a. The first step-and-repeat UV- based nanoimprint tool

Figure 3b. The Imprio 100, from Molecular Imprints, Inc. The system is designed to pattern wafers as large as 200 mm in diameter.

Although the Imprio 100 from MII is a substantial improvement relative to the first University tool, it has neither the throughput nor the overlay specifications necessary for silicon IC fabrication. Instead, the system was primarily designed and manufactured to address the compound semiconductor and photonics markets. These markets require high-resolution features but are typically less sensitive to defects. They also operate at low volumes of wafers and are hence more sensitive to costs; particularly tool costs. The tool has a throughput capacity of approximately six, 200mm, wafers per hour. As a result it will be possible to collect enough statistical information of performance characteristics of S-FIL to allow the design of a fully engineered high volume-manufacturing tool in the future.

The Imprio 100 was developed in partnership with several key OEM suppliers for the stage technology, the UV source, and the control architecture. The extremely complicated and costly imaging optics, source, and step and scan mechanical systems associated with other NGL techniques are not required in S-FIL technology. It is essentially a precise mechanical system with specialized fluid mechanics sub-systems and a mercury arc lamp as its source. Therefore, it is a much simpler system with significantly smaller footprint, and its cost structure has the potential to be an order of magnitude lower than high-end lithography tools. Of particular interest is the resist delivery system, which incorporates a microsolenoid nozzle capable of dispensing drops less than 5 nl in volume. This type of control is essential for the control of the residual layer formed during the imprint process. Currently the residual layer has a mean thickness of approximately 100 nm.

3. THE S-FIL TEMPLATE

Early template fabrication schemes started with a 6" x 6" x 0.25" conventional photomask plate and used established Cr and phase shift etch processes to define features in the glass substrate.[7] Although sub-100 nm geometries were demonstrated, critical dimension (CD) losses during the etching of the thick Cr layer etch make the fabrication scheme impractical for 1X templates. It is not unusual, for example, to see etch biases as high as 100 nm.[8]

More recently, two methods have been employed to fabricate templates.[9,10] The first method uses a much thinner (15 nm) layer of Cr as a hard mask. Thinner layers still suppress charging during the e-beam exposure of the template, and have the advantage that CD losses encountered during the pattern transfer through the Cr are minimized. Because the etch selectivity of glass to Cr is better than 18:1 in a fluorine based process, a sub-20 nm Cr layer is also sufficient as a hard mask during the etching of the glass substrate. The second fabrication scheme attempts to address some of the

weaknesses associated with a solid glass substrate. Because there is no conductive layer on the final template, SEM and defect inspection are compromised. By incorporating a conductive and transparent layer of indium tin oxide (ITO) on the glass substrate, charging is suppressed during inspection, and the transparent nature of the final template is not affected. Flows for each fabrication process are shown in Figure 4. The experimental details of the processes have been covered in previous publications.[10,11]
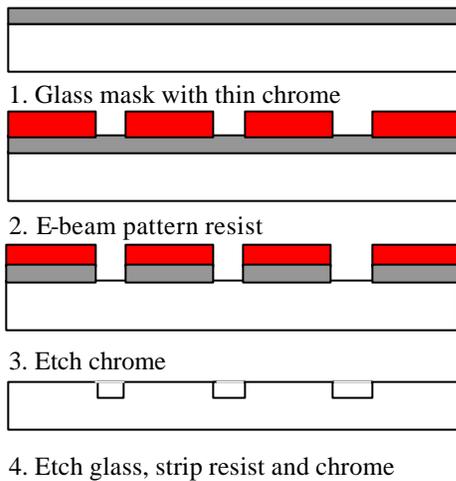
1. Glass mask with thin chrome

2. E-beam pattern resist

3. Etch chrome

4. Etch glass, strip resist and chrome

Figure 4a. Conventional template process, using 15 nm of Cr as a hard mask.

SiO_2
ITO

1. Glass mask with ITO/SiO_2

2. E-beam pattern resist
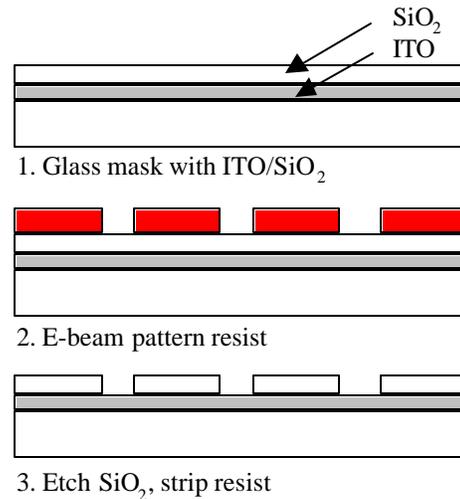
3. Etch SiO_2, strip resist

Figure 4b. Template process flow incorporating an ITO charge dissipation and etch stop layer

The template pattern transfer exposure process shown in Figure 4a consisted of an exposure in a Leica VB6 and development of the ZEP-520 positive resist, followed by an oxygen descum, Cr etch, resist strip, quartz etch and a Cr wet etch. It is interesting to note that it was necessary to remove the resist prior to the quartz etch. If left in place during the CHF_3 based quartz etch, the amount of polymer deposited during the etch process is substantial enough to impact the fidelity of the quartz features. Additional amounts of oxygen may be necessary to minimize polymer formation. The process sequence for 30 nm features is depicted below.

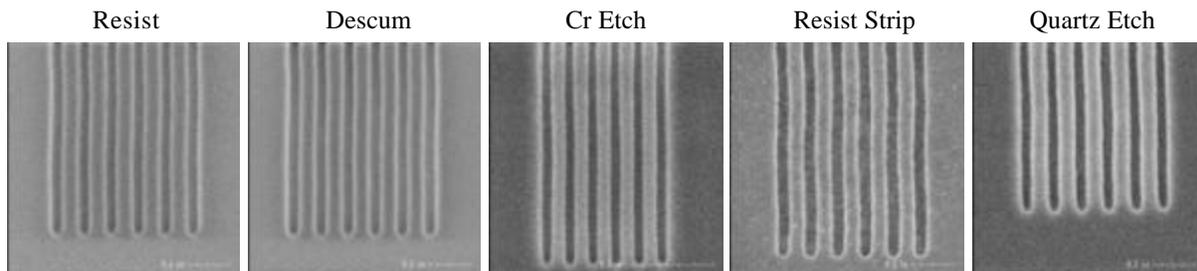| Resist | Descum | Cr Etch | Resist Strip | Quartz Etch |

Figure 5. Pattern transfer sequence for 30 nm trenches. Lines between the trenches are 100 nm. At higher exposure doses, the 20 nm features were also resolved, although defects were observed in the final quartz etch.

Previous work has noted that the fabrication process seemed to be uniform.[10] In order to test this assumption, a template was designed, placing a small resolution test pattern in an 8 x 8 array, covering a 25 mm x 25 mm area. The first set of measurements on 100 nm dense trenches is shown in Figure 6. The mean trench size was 105.2 nm with a 3 variation of only 6.2 nm. More recent work has demonstrated that a 3 variation of 4.3 nm is possible.[12]

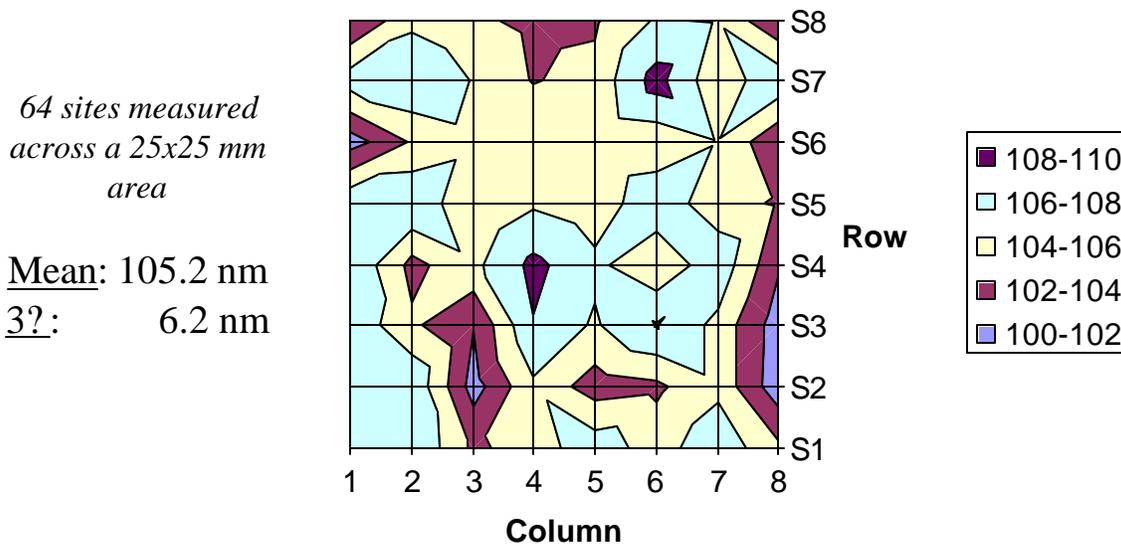*64 sites measured across a 25x25 mm area*

Mean: 105.2 nm
3?: 6.2 nm

Figure 6. Uniformity plot of 100 nm dense trenches across a 25 x 25 mm template.

Widespread use of imprint lithography will require that the template be both inspectable and repairable. For applications requiring sub-100 nm lithography, it will likely become necessary to inspect the templates using electron beams. If this is the case, the template will need a charge reduction layer to dissipate charge during the inspection process. Figure 4b depicts a fabrication scheme that incorporates a transparent conducting oxide, such as indium tin oxide (ITO), into the final template. A thin layer of PECVD oxide is deposited over the ITO and defines the thickness of the imprinted resist layer. Features are formed on the template by patterning an electron beam resist, transferring the pattern via reactive etching into the oxide, and stripping the resist.

The ITO must have sufficient conductivity to avoid charging effects first during resist exposure and later during template inspection. The resistivity of the as-deposited ITO film is on the order of 2.0×10^6 ohms/sq. The resistivity decreases substantially, however, after the films are annealed at a temperature of 300 °C. In its annealed state, the ITO film resistivity is about 3.5×10^2 ohms/sq. Charge dissipation during e-beam writing and SEM inspection is realized at this conductivity level. The ITO must be also be very transparent at the actinic wavelength used during the SFIL exposure process (365 nm). It is possible to achieve transmission well above 90% at 365 nm.[13] The ITO has the additional attribute of performing as an excellent etch stop during the pattern transfer of the PECVD oxide layer. Examples of final template features formed using this process are shown in Figure 7.
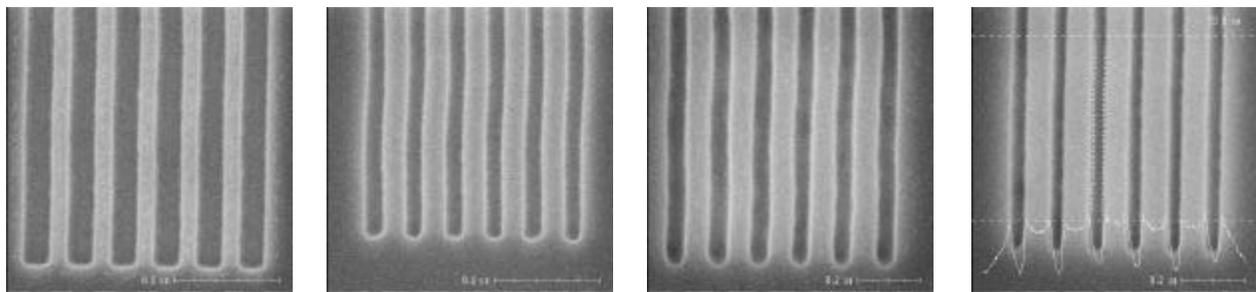

Figure 7. 100, 60, 30, and 20 nm features defined using the ITO-based process.

An even simpler way to make a template is to use an electron beam sensitive flowable oxide, such as hydrogen silsequioxane (HSQ). While the primary use of HSQ is as a low-k dielectric, several investigators have demonstrated its usefulness as a high-resolution electron beam resist. In its cured state, HSQ becomes a durable oxide making it a very convenient material for direct patterning of SFIL template relief structures. Processing of HSQ as an electron beam

resist is less complicated since it is not chemically amplified, and can be developed in the standard tetramethyl ammonium hydroxide (TMAH) based developers used commonly for conventional resists. All that is required to make a template is to coat and bake the HSQ directly on the ITO layer, and then expose and develop the HSQ.[14]

It is interesting to note that the methods described in this section can also be used sequentially to form multilayer structures that can be used to fabricate devices such as T-gates or optical grating couplers.[15] SEM pictures depicting two-tiered and three-tiered structures are shown in Figure 8. Figures 8a and 8b are tiered structures produced using alternating layers of ITO and PECVD oxide. Figure 8c was produced by patterning a bottom oxide film and subsequently coating, exposing and developing an HSQ layer.

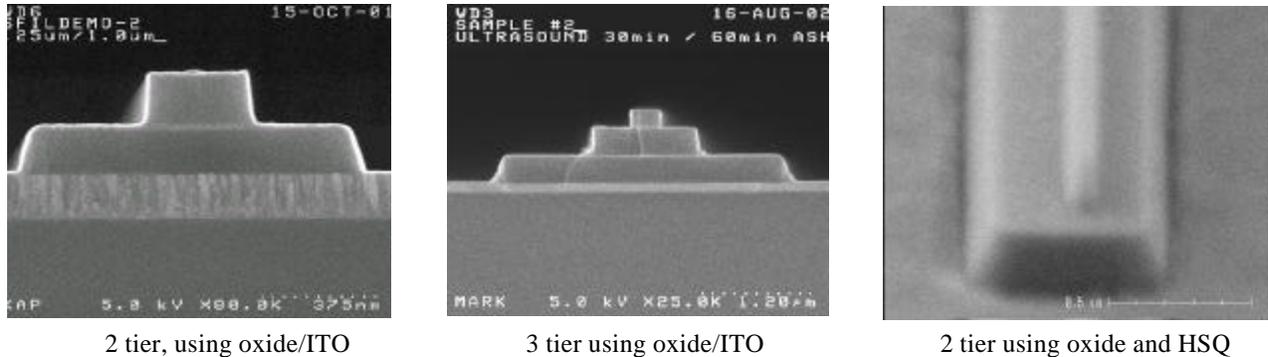| 2 tier, using oxide/ITO | 3 tier using oxide/ITO | 2 tier using oxide and HSQ |

Figure 8. Multi-tiered structures formed by iterating the fabrication process.

The final step in the template fabrication process is a treatment designed to lower the surface free energy. Alkyltrichlorosilanes form strong covalent bonds with the surface of fused silica, or SiO_2. In the presence of surface water they react to form silanol intermediates which undergo a condensation reaction with surface hydroxyl groups, and adjacent silanols to form a networked siloxane monolayer. When this functional group is synthetically attached to a long fluorinated aliphatic chain, a bifunctional molecule, suitable as a template release film is created. The silane terminated end bonds itself to a template's surface, providing the durability necessary for repeated imprints. The fluorinated chain, with its tendency to orient itself away from the surface, forms a tightly packed comb-like structure and provides a low energy release surface. Annealing further enhances the condensation creating a highly networked, durable, low surface energy coating.

4. RESIST

The resist stack typically consists of a silicon containing etch barrier over an antireflective coating (also referred to as the transfer layer). The etch barrier is patterned via the imprint process. The subsequent pattern transfer process involves an etch of the remaining residual layer (~ 100 nm in thickness), followed by an anisotropic etch of the transfer layer.

The etch barrier material is subject to several design constraints. The etch barrier liquid must be dispensable from an automatic fluid dispense system, and must not change significantly in composition between dispensing and imprinting by, e.g., component evaporation. It must be readily displaced during the imprint step and photopolymerize rapidly during exposure. Shrinkage due to polymerization must be controlled. The polymer must release from the template while adhering to the transfer layer, and it must exhibit sufficient rigidity to avoid feature collapse It must exhibit some level of temperature stability to withstand the etching temperatures, and it must exhibit sufficient etch selectivity during the O_2 RIE step to allow for high aspect ratios to be generated in the transfer layer.

The S-FIL process relies on photopolymerization of a low viscosity, acrylate-based solution. Acrylate polymerization is known to be accompanied by volumetric shrinkage that is the result of chemical bond formation. Consequently, the size, shape, and placement of the replicated features may be affected. Volumetric shrinkage was found to be less than 10% (v/v) in most cases.[16]

The current etch barrier liquid is a multicomponent solution that has been previously been described in detail.[16] The silylated monomer provides etch resistance in the O_2 transfer etch. Crosslinker monomers provide thermal stability to the cured etch barrier and also improve the cohesive strength of the etch barrier. Organic monomers serve as mass-persistent components and lower the viscosity of the etch barrier formulation. The photoinitiators dissociate to form radicals upon UV irradiation, and these radicals initiate polymerization. The various components of the etch barrier are shown in Figure 9.

| Silicon containing | cross-linker | thinner | photo initiator |

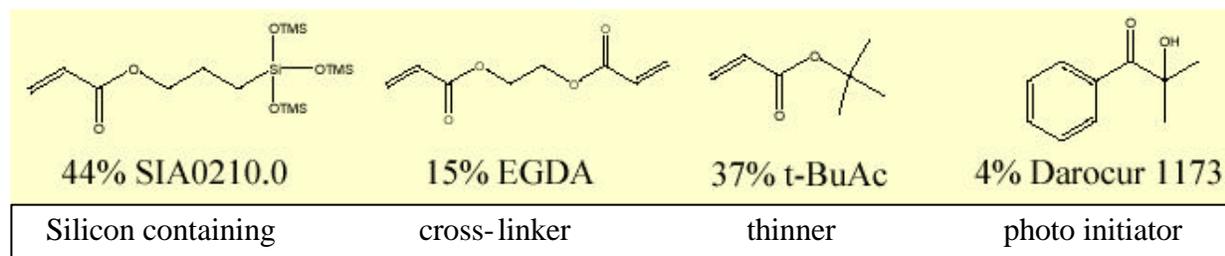44% SIA0210.0   15% EGDA   37% t-BuAc   4% Darocur 1173

Figure 9. Current etch barrier components.

SEMs of this etch barrier are shown in Figure 10a. 20 nm features have been resolved with both types of templates described earlier. Cross sectional images are shown in Figure 10b. The profiles closely replicate the relief image in the template for both single and multi-tiered structures. Critical dimension uniformity studies have also been performed. As expected, there is only a small additional variance in the CD caused by the printing process.[14]

a   80 nm   60 nm   30 nm   20 nm

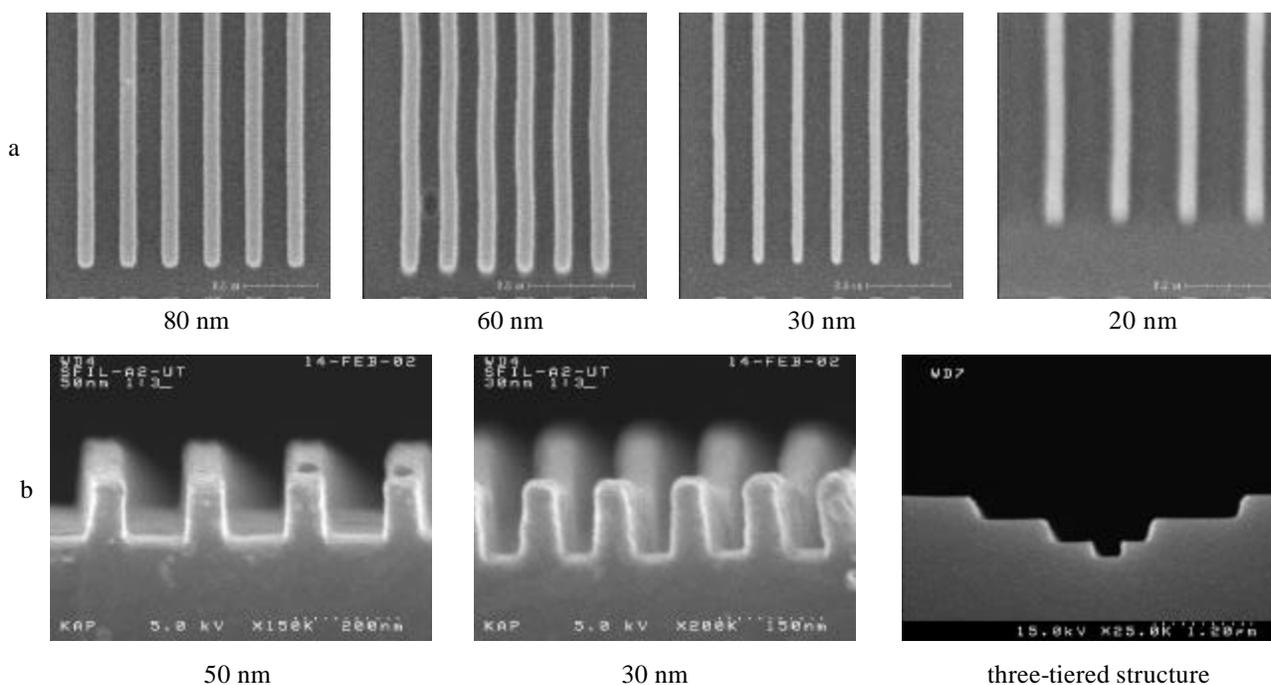b   50 nm   30 nm   three-tiered structure

Figure 10. Printed features in the acrylate-based etch barrier. Figure 10a depicts top-down SEMs. Figure 10b shows cross-sectional images of both single tier and multi-tiered features.

Prior to etching the underlying transfer layer, it is necessary to remove the residual etch barrier material formed during the imprint process. Because the silicon content is at least 12%, best selectivity between the etch barrier and the transfer layer is achieved by using a combination of CF_4 and oxygen. Once the transfer layer is exposed, the gas chemistry is

comprised only of O_2. Recent studies indicate that selectivities greater than 6:1 may be possible for both etches. Figure 11 shows the pattern transfer sequence. More details on this process can be found in this Proceedings.[17]
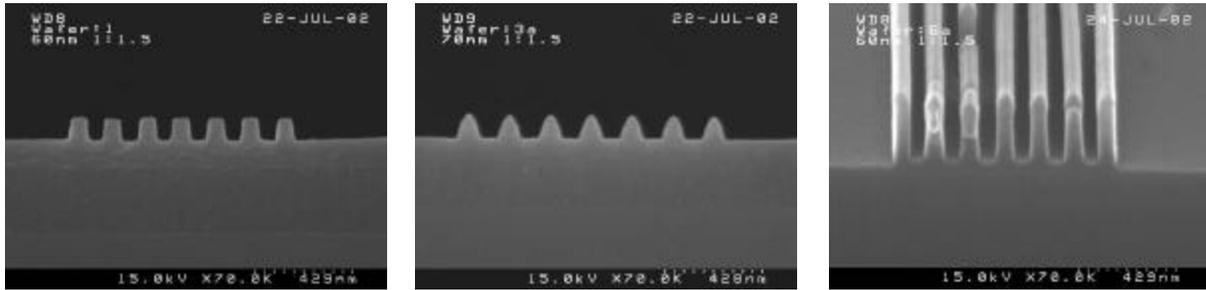

Figure 11. Pattern transfer sequence showing the etch barrier over the transfer layer, the residual layer etch, and the etch of the transfer layer.

It is interesting to note that the presence of oxygen dissolved in the etch barrier and in the ambient environment causes two undesirable effects on the curing of the acrylate etch barrier. Oxygen dissolved in the etch barrier consumes photoinitiated radicals, resulting in an inhibition period before polymerization begins. Furthermore, oxygen diffusion into the etch barrier limits the curing reaction around the perimeter of the template. While it may be possible to modify the ambient, other chemistries, such as vinyl ethers may be more suitable for the imprint process. This approach eliminates the oxygen inhibition effect and may also further reduce the viscosity of the etch barrier, thereby further reducing the residual layer formed during the imprint process.

5. ISSUES

Several other issues need to be addressed before S-FIL can be considered as a viable technology for silicon IC fabrication. Because imprint lithography is a "contact" lithography, there are concerns associated with defects generated during the process. As a 1X technology, there are also concerns relative to template to wafer alignment. Finally, a planar surface is required for imaging, and the issue of how planarization can be accomplished must be reviewed. Each of these topics is discussed below.

a. Defects

The low surface energy monolayer applied to the template acts effectively as a self cleaning agent. This attribute is depicted in Figure 12. A dirty template was used to imprint several die on a silicon wafer. The progression of pictures indicates that defects that start on the template embed themselves in the etch barrier, and by the seventh imprint, there are no detectable particles. It is also interesting to note that there does not appear to be any degradation of the release layer over time. Contact angles measurements show no change after more than two months.[4]
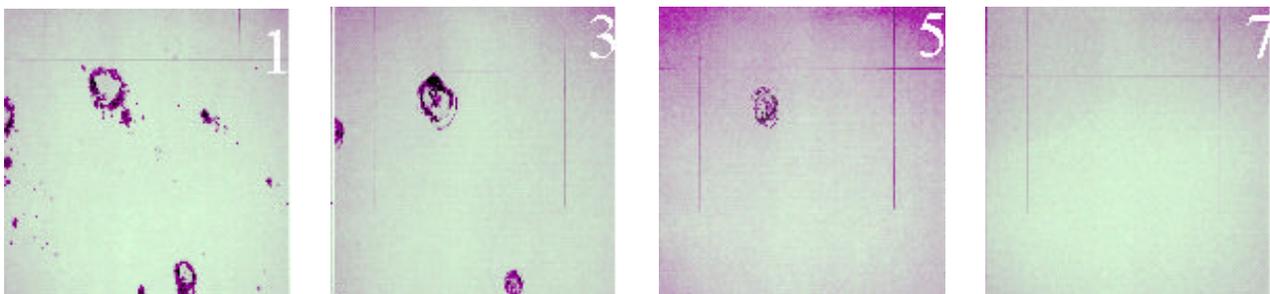

Figure 12. Optical micrographs depicting the defects remaining after seven imprints. The self-cleaning effect removes defects on the template surface, and by the seventh imprint, the template is defect-free.

While the data clearly illustrates a self-cleaning effect, this is not sufficient evidence to prove that defects are not added after many imprints. A more convincing study involves printing wafers, and having the defects tracked using an inspection tool. An initial set of 14 imprints were inspected with a KLA 2132 inspection system in array mode. The data for these imprints is shown in Figure 13. Although the data is noisy and the number of defects is relatively large, there does not appear to be an increase in defects. Clearly, a larger data set is required to be able to make a definitive statement about defect levels.
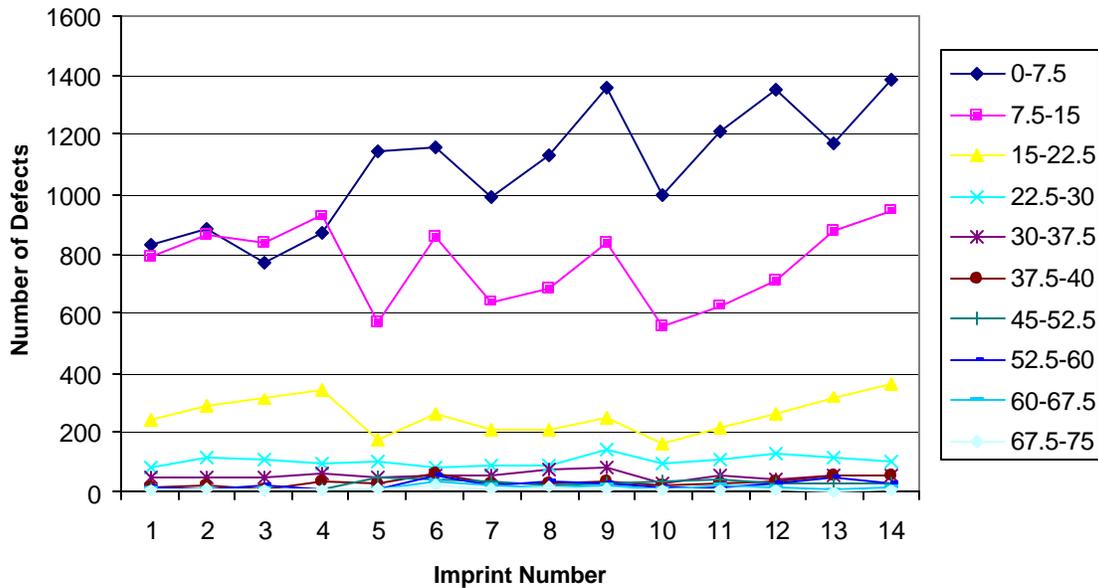

Figure 13. Defect levels vs. imprint number.

b. Image Placement and Overlay

Two concerns worth addressing are: 1.) does the template fabrication process result in image placement errors that cannot be removed using conventional correction techniques such scale and orthoganality corrections, and 2.) if image placement is good, can the imprint tool align and make the corrections necessary to meet the stringent requirements for silicon processing.

To examine image placement, a 6025 photoplate was patterned over a 5' x 5" area with alignment marks. Image placement was measured using a Leica LMS 2020 during each step of the Cr/Quartz template fabrication process described in a previous publication.[9] The resultant image placement errors has a maximum error of approximately 15 nm. This error can be attributed to the stress of the chromium film. The image placement errors experimentally observed agree very well with finite element models.[18] A typical distortion map is shown in Figure 14a.

To determine what type of overlay error would result from the patterning process, a second plate was written, using an opposite tone resist. The center 1" x 1" (a typical field size) areas of both plates were then compared. The result, after correcting for scale and orthoganality are shown in Figure 14b.[19] The displacement vectors are typically less than 10 nm and are randomly directed, indicating that the error vectors are mostly limited to the sensitivity of the LMS 2020.

The issue of overlay comes down to the capabilities of the imaging system and the method used for imprinting. Because S-FIL is a room temperature and low pressure (~2 psi) process, the real concern becomes the ability of the tool to overlay different mask levels. Tool capability has two major components: the first is related to the alignment method and alignment optics. The second is the ability to correct for distortion errors such as magnification and orthoganality. The current method of alignment on the Imprio 100 takes advantage of the transparent template, and a through the template

alignment system is used to align marks on both the wafer and template. This type of system may actually be advantageous relative to reduction systems, since distortion errors from the lens elements are eliminated. It should be a straightforward task, therefore, to align within a few hundred nanometers.

The real challenge, then, is to be able to correct for distortion between the template and wafer. One possible way to accomplish this is to set a series of piezos around the template. Wood et al. have presented this model and have been able to theoretically demonstrate distortion correction.[20] To date, no experimental verification has been done and remains a piece of the puzzle still to be solved.
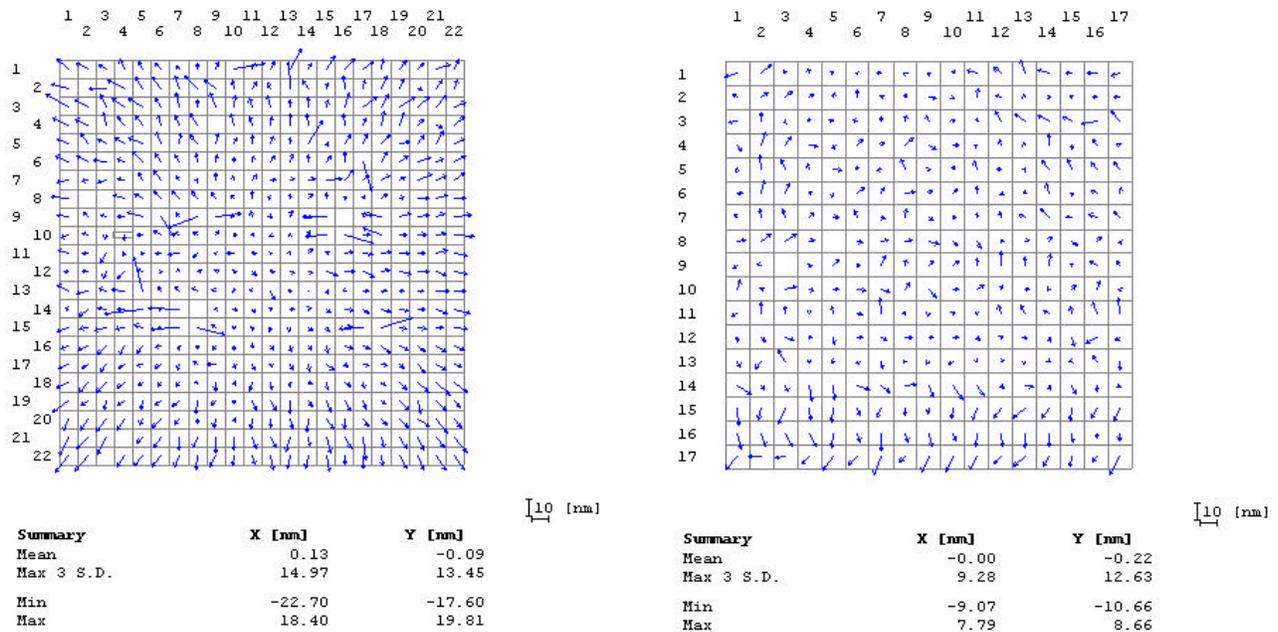
Figure 14. (a) Distortion map after the chromium layer has been removed from the template. (b). Distortion map comparing the center 1" x 1" areas from two different templates.

c. Planarization

Neither the chucked silicon wafer nor the template are very compliant, requiring a flat or planar surface for imprinting. There are a number of different methods for planarizing the wafer surface, but the easiest method may be to employ the S-FIL process using a template with no relief images. A demonstration of this approach has been already been published.[9] Two examples are shown below. Relative to the defect and overlay issues, planarization is a minor concern at this point.
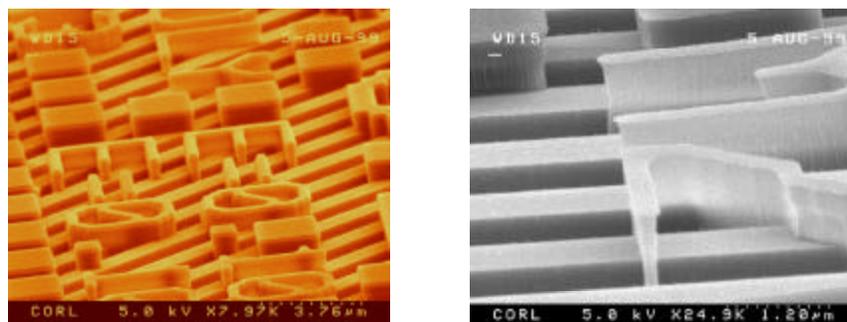
Figure 15. Two examples of imprinting over a planarized surface.

CONCLUSIONS

Nanoimprint lithography has come a long way in a very short period of time. Resolution seems limited to the ability to form a relief image in the template and sub-10 nm printing has already been demonstrated. To be considered as a method for fabricating silicon integrated circuits, several concerns still need to be addressed. UV-NIL, and in particular S-FIL, seem the best imprinting option for meeting the stringent requirements of future generations of silicon-based circuitry. Tools, templates and resists are readily available to start exercising the technology and will be used to answer the open issues such as defectivity and overlay. If these issues can be solved, imprint lithography may be the right NGL, since extendibility to at least 10 nm seems viable. The last consideration, then becomes the supporting infrastructure. Reduction lithography has been in the mainstream now for over 20 years, and the ability to write, inspect and correct a 1X template will need to be developed.

ACKNOWLEDGEMENTS

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