32 nm imprint masks using variable shape beam pattern generators

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Abstract

Imprint lithography has been included on the ITRS Lithography Roadmap at the 32, 22 and 16 nm nodes. Step and Flash Imprint Lithography (S-FIL ®) is a unique method that has been designed from the beginning to enable precise overlay for creating multilevel devices. A photocurable low viscosity monomer is dispensed dropwise to meet the pattern density requirements of the device, thus enabling imprint patterning with a uniform residual layer across a field and across entire wafers. Further, S-FIL provides sub-100 nm feature resolution without the significant expense of multi-element, high quality projection optics or advanced illumination sources. However, since the technology is 1X, it is critical to address the infrastructure associated with the fabrication of templates.

For sub-32 nm device manufacturing, one of the major technical challenges remains the fabrication of full-field 1x templates with commercially viable write times. Recent progress in the writing of sub-40 nm patterns using commercial variable shape e-beam tools and non-chemically amplified resists has demonstrated a very promising route to realizing these objectives, and in doing so, has considerably strengthened imprint lithography as a competitive manufacturing technology for the sub 32nm node. Here we report the first imprinting results from sub-40 nm full-field patterns, using Samsung's current flash memory production device design. The fabrication of the template is discussed and the resulting critical dimension control and uniformity are discussed, along with image placement results. The imprinting results are described in terms of CD uniformity, etch results, and overlay.

Keywords: S-FIL, template, imprint lithography, full field, overlay, pattern transfer, NAND Flash

1. Introduction

Small feature imprint lithography has existed for several years. The original technique involved the use of a patterned template which is impressed onto a thermo plastic material and, with the combination of heat and pressure, the pattern in the template was transferred to the substrate. Recently the technique has been significantly improved with the development of Step and Flash Imprint Lithography (S-FIL ®).[1] This technique involves the deposition of a low viscosity monomer on the substrate, lowering a template into the fluid which then flows into the patterns of the template. Following this fill step, the monomer is exposed to UV light to cross-link it and convert it into a solid, and the template is removed leaving the solid pattern on the substrate.[2] The advantages of this development make it uniquely capable for CMOS applications.

Critical to the success of the technology is the commercial availability of 1X templates (imprint masks). Recently, there have been several publications addressing the fabrication of templates with 32nm and sub 32nm half pitch dimensions using high resolution Gaussian beam pattern generators.[3,4] Examples of features imprinted with these templates are shown in Figure 1. Several commercial mask shops now accept orders for 1X templates made by Gaussian beam tools. Currently, these systems are proving useful for unit process development and device prototyping purposes.

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resulting critical dimension control and uniformity are discussed, along with image placement results. The imprinting results are described in terms of CD uniformity, etch results, and overlay.

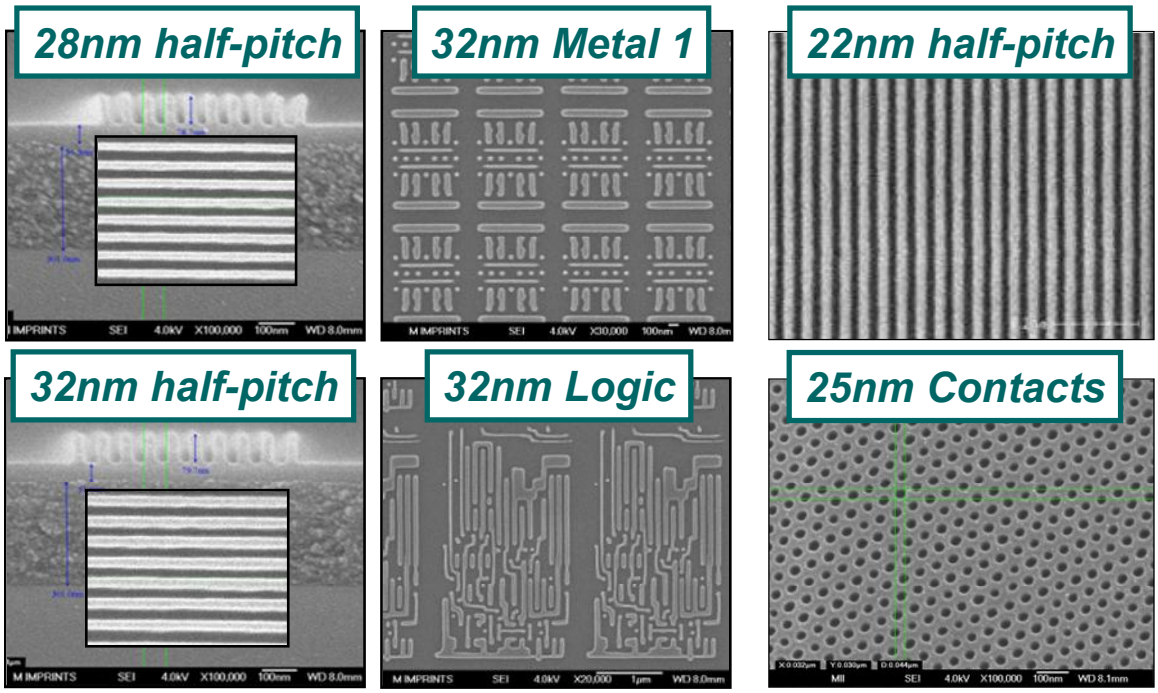


Figure 1. High resolution imprints generated with templates written with a Gaussian beam pattern generator. Pictured are 22nm, 28nm, and 32nm dense lines, 32nm Metal-1 and Logic test patterns, and 25nm half pitch contacts.

2. Experimental Details

To generate the template, patterns were exposed using 50 keV variable shaped beam pattern generators. ZEP520A resist was chosen as the positive imaging resist. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process, followed by a dice and polish step were employed to create a finished 65 mm x 65 mm template.[5]

The initial pattern chosen to evaluate the potential of VSB technology consisted of small arrays of lines, holes, Metal-1, and Logic patterns. The layout is shown in Figure 2.

The pattern chosen for full field evaluation was a 38nm half pitch NAND Flash gate layer. The patterned area consisted of repeating core, a repeating periphery and non-repeating test chips. The approximate device size was 18 mm x 30 mm. Key elements of the repeating core are the dense 38nm lines and the transition regions to larger pitches at right angles to the primary pattern. This is best illustrated in the lower right hand corner of Figure 3. Write time of the imprint mask was approximately 10 hours.

Imprinting of the template pattern was performed by using a Molecular Imprints Imprio 250 imprint tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 200 mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process have previously been reported.[6]

CD and LWR measurements were performed two different ways. In the first case, high resolution SEM images were taken with a JEOL JSM-6340F field emission cold cathode SEM equipped with a tungsten emitter. The accelerating voltage can be varied from 0.5 to 30 kV. The system has intrinsic 1.2 nm resolution capability at 15 kV accelerating voltage, and 2.5nm at 1 kV. Critical dimension (CD), line width roughness, and line edge roughness (LER) data were then extracted offline using the SIMAGIS® automated image metrology software suite from Smart Imaging Technologies.[7] For the analysis of within wafer uniformity and wafer-to-wafer uniformity, an AMAT NanoSEM was

used to collect information on CD, LWR and LER. The beam accelerating voltage was 500V. The length of a line scan was 1 μm, and 512 scans were performed.

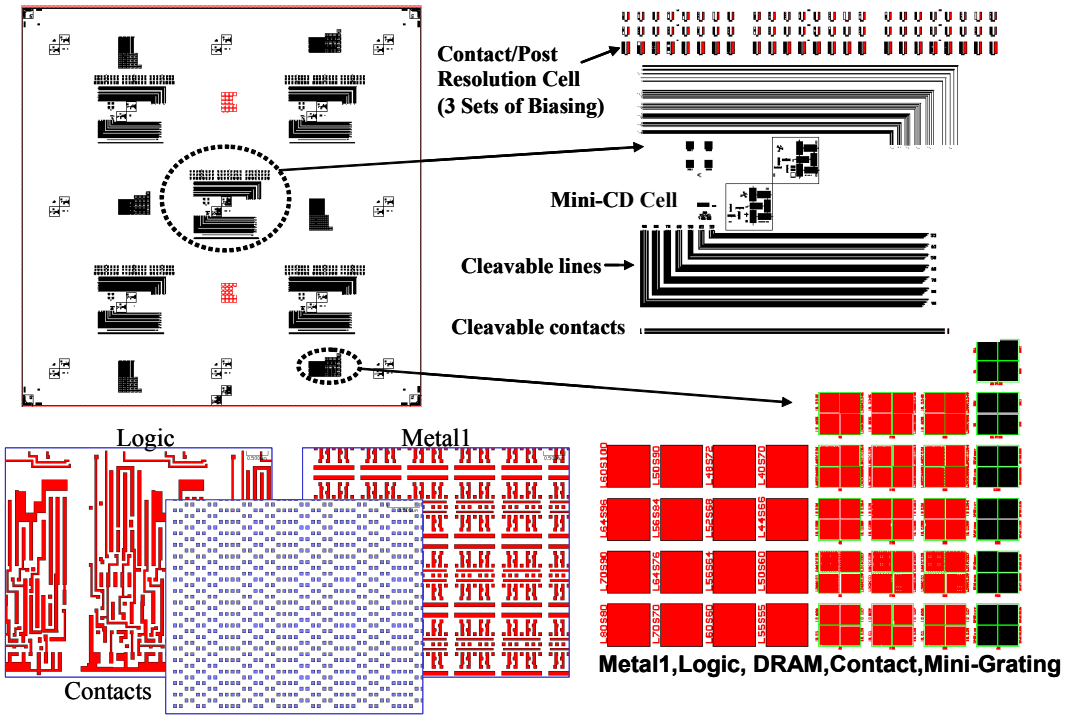


Figure 2. Test pattern used to analyze the resolution of the exposure and pattern transfer processes. The test pattern includes dense lines, contact holes, and CMOS-like structures.

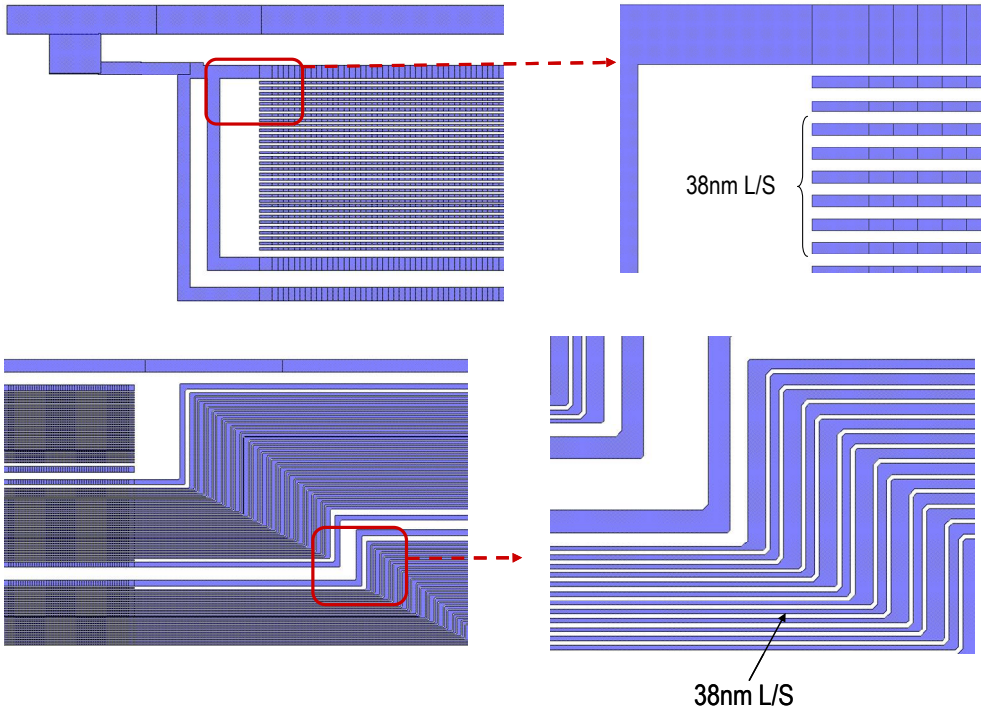


Figure 3. Key elements of gate layer, including the dense 38nm lines and the transition regions to larger pitches at right angles to the primary pattern

3. Results

a. Test Pattern Characterization

Images from the test template are shown in Figure 4. The Cr hardmask was not removed at this step in order to more clearly observe the features in the SEM. In a previous study performed with a 100 kV Gaussian beam system, better resolution and improved process latitude was obtained by introducing negative feature biasing to the coded pattern, and then overexposing the pattern during the writing process.[8] In this study, biases as large as -18nm were applied, resulting in improvements in process latitude of better than 3x.

The same approach was also evaluated for the test plate. The smallest lines resolved were 32 nm. The 35 nm Metal1 patterns resolved, as did the 40 nm DRAM contact arrays. These results were obtained with the writing and pattern transferring of only two plates. While there is still room for process optimization the results were very promising. As a result, the decision was made to move on to the full field gate layer.

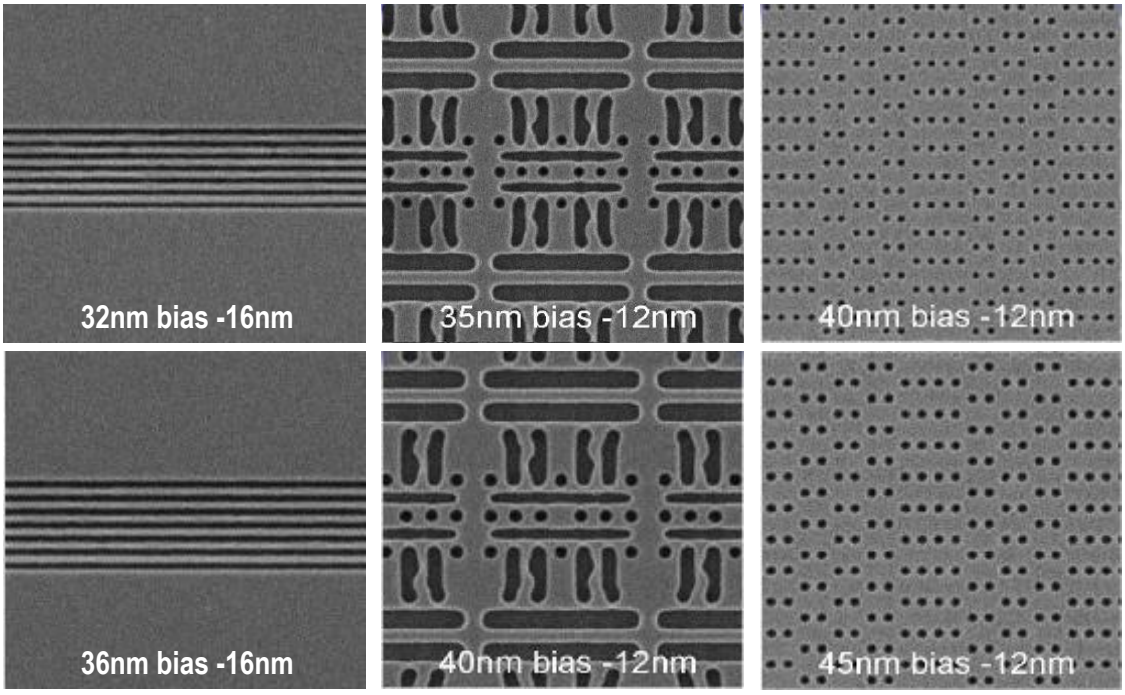


Figure 4. Template images with feature bias. Feasibility for 32 nm half pitch resolution is demonstrated.

b. Full Field Template Fabrication and Characterization

The template was written using a high resolution ZEP520A resist process. A multipass writing strategy was employed to compensate for the low resist sensitivity. It is important to note that the write times were still reasonable (~ 10 hours) when compared with a 4x photomask counterpart. This an expected result, due primarily to the reduced writing area and no requirement for optical proximity correction (OPC). Previously published results on two different 32 nm patterns have demonstrated a reduction in write time (relative to a 4x photomask) of 1.2x to 3x.[8]

A brief analysis of the template was done after the fused silica etch, but before the chromium was stripped. Pattern fidelity is illustrated in Figure 5. The 38 nm half pitch lines are well resolved. The spaces measure 33.1 nm and the 3σ variation for five locations was 2.2 nm. The line width roughness measurements on the template ranged from 3.9nm to 5.1 nm, 3σ. It should also be noted that, although no pattern optimization was done in the non-repeating test areas,

several of the test patterns were resolved below 38 nm. Pictured in Figure 6 are line space pairs at 32 nm and 35 nm, respectively.

A set of nine metrology marks were also included in the pattern, in order to determine image placement. An LMS IPRO II metrology system was used to read the nine marks. The 3 sigma variation in x and y, was extremely low: 1.6 nm and 2.6 nm, respectively.

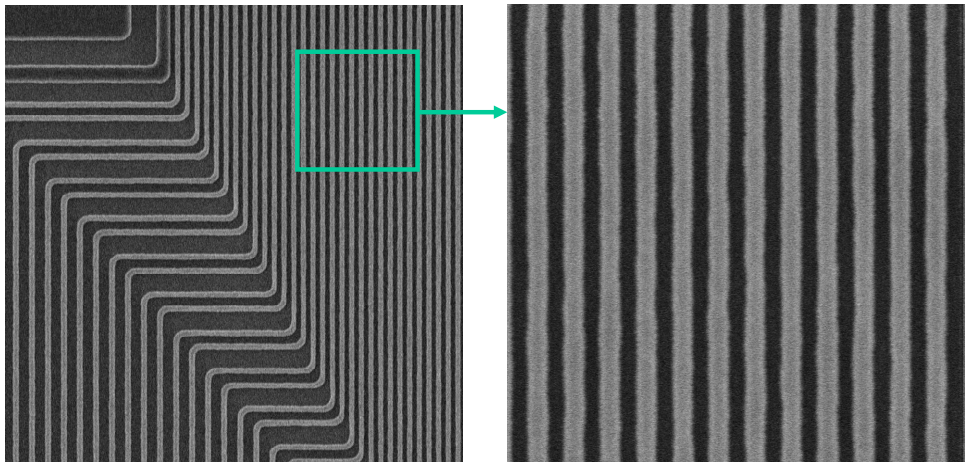


Figure 5. Primary pattern of the 38nm NAND Flash Gate layer. The 38 nm half pitch lines are well resolved and the right angle transition regions are characterized by good fidelity in the corner areas.

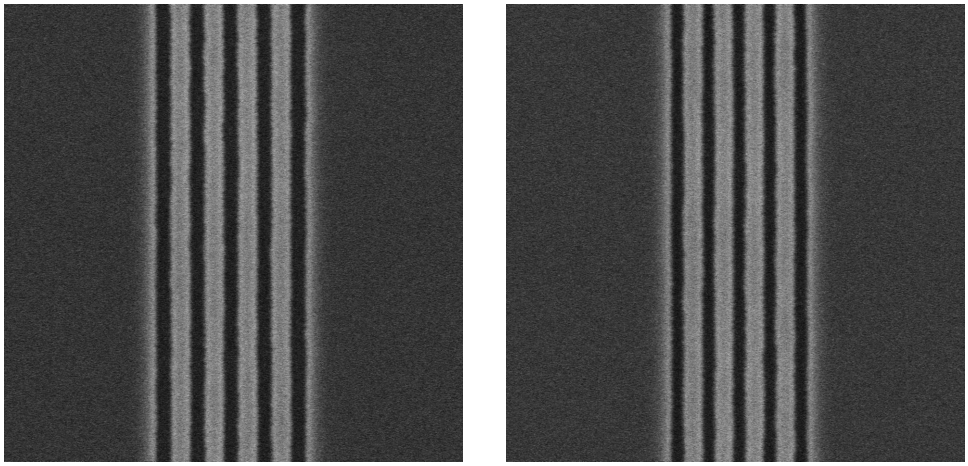


Figure 6. 35nm and 32nm half pitch features in the template.

c. Imprint Results

The template was used to imprint the device on 300 mm wafers. The resulting imprints are shown in Figure 7. Figure 7a depicts a low magnification image of the gate layer. All patterns were clearly resolved, including both the 38 nm half pitch lines and the right angle transition regions. Figure 7b shows a larger magnification of the same region. 30 degree tilted views show the resolution of both regions described above. The 38nm lines have a profile close to 90 degrees, and there is very little line width roughness observed. A SIMAGIS calculation of the features in Figure 7c yields a CD of 39.6nm and LWR of only 3.7 nm, 3σ. Figure 7d depicts a magnified view of the well defined corner regions. SIMAGIS software was also used to measure in field CD uniformity. Eighteen locations were measured in the core area. Each location used eleven lines to determine CD. As a result a total of 198 lines were measured. The mean CD was 41.9 nm with a three sigma variation of 2.13 nm. LWR was 3.56 nm, 3σ (Figure 8).

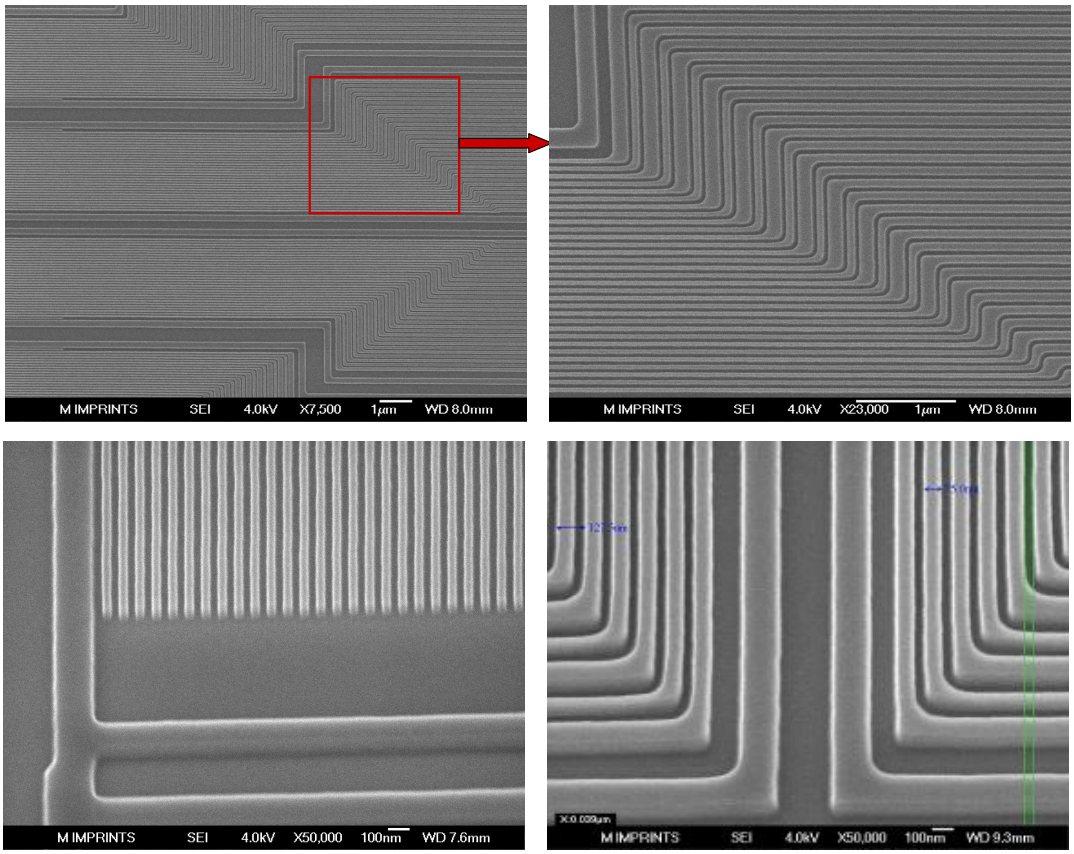
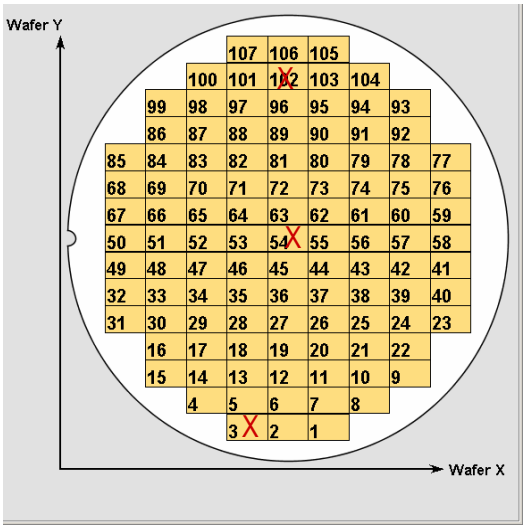
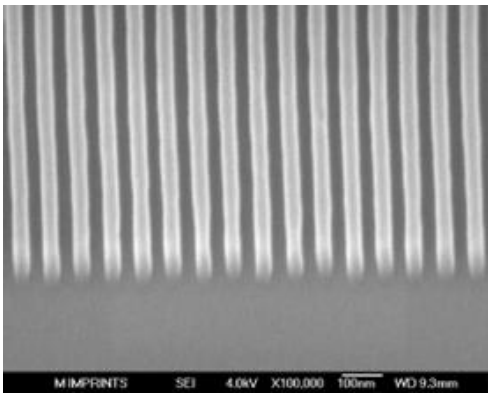


Figure 7. Imprinted 38 nm half pitch lines are resolved and feature fidelity is excellent in the transition regions.



18 measurements/field
3 fields/wafer
4 wafer set



Within Field 3 sigma:	3.17 nm
Within Wafer 3 sigma:	3.62 nm
Wafer-to-Wafer 3 sigma:	0.51 nm
LWR = 3.76 nm	
LER = 2.39 nm	

Figure 8. In order to determine field-to-field and wafer-to-wafer variations, 18 measurements were made within a field, at three field locations, across a four wafer set.

Field-to-field and wafer-to-wafer uniformity was measured using an AMAT CD SEM. Nine measurements were made per repeating device core, for a total count of 18 measurements per field. Three fields were measured per wafer across a four wafer set (See Figure 6). The field-field 3σ variation was only 3.17 nm and corresponding wafer-to-wafer variation was only 0.37 nm. The average LWR and LER values were 3.76 nm and 2.39 nm, respectively.

Image resolution was further explored by examination of the non-repeating test areas. Shown in Figure 9 are Metal-1 and dense lines resolved at 32nm. The 30 nm patterns did not completely resolve, and will require some additional process optimization.

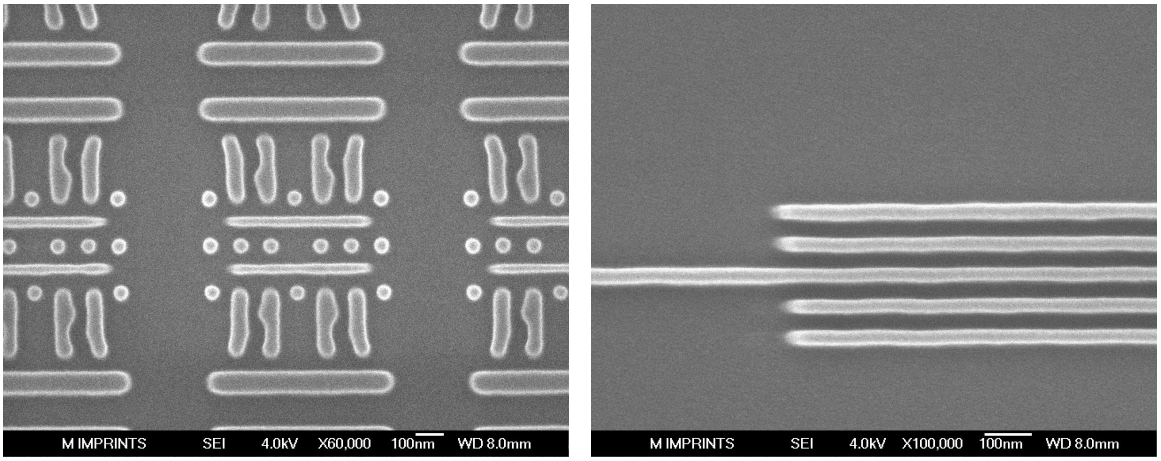


Figure 9. 32nm Metal-1 and 32nm half pitch lines

d. Overlay Results

All imprint tools for CMOS applications must be designed to mix and match with existing 193nm optical lithography tools. The Imprio-250 uses a field by field alignment system.[9] This method does not add to the imprint time since the alignment occurs during the time that the fluid is filling the template features. Since the template and substrate are in close proximity (<10μm) during the alignment process, it is practical to capture the relative positioning error between two matching alignment marks using a Moiré image based technique[9,10]

Magnification correction is achieved by mechanically compressing the template. Positive magnification can be achieved by writing the template 5ppm oversize and releasing the compression. In this way the required +/- 5ppm can be obtained. Since the distortion is this small, well within the elastic regime of the material, it is perfectly reversible. A multi-point forcing mechanism was developed[(19)] that can induce optimized vectors of correction forces along the periphery of the template.

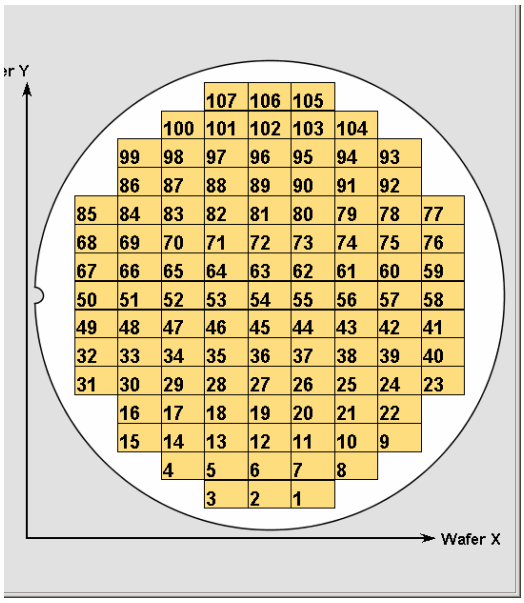
The efficacy of the alignment and magnification control systems were tested by performing a mix and match test. The 38 nm NAND Flash gate level was overlayed to a zero level applied with a scanner. By performing a send ahead measurements and inserting an offset, a mean plus 3 sigma overlay of 34 nm in x and 21 nm in y was achieved. The data set, picturing overlay results accumulated in 30 fields is displayed in Figure 10. A second send ahead wafer yielded values of 28 nm in x and 27 nm in y. Other printed wafers yielded overlay values ranging from 24 nm to 57 nm. The major sources of the error are thought to be from thermal distortions, placement errors on the template and image field distortions from the 193nm scanner. Further improvements are expected to reduce the overlay errors down to less than 10 nm.

	X (mm)	Y (mm)	MagX (ppm)	MagY (ppm)	Theta(mrad)	Skew(mrad)
F1 Overlay:	0.000012	0.000004	1.0000005	1.0000004	-0.000300	-0.0000002
F3 Overlay:	0.000015	0.000005	1.0000005	1.0000001	-0.000664	-0.0000005
F5 Overlay:	0.000012	0.000013	1.0000004	1.0000004	-0.000323	-0.0000002
F7 Overlay:	0.000015	0.000002	1.0000004	1.0000003	-0.000286	-0.0000001
F9 Overlay:	0.000013	0.000003	1.0000004	1.0000004	-0.000305	-0.0000001
F11 Overlay:	0.000012	-0.000000	1.0000004	0.9999999	-0.000449	-0.0000003
F13 Overlay:	0.000015	0.000007	1.0000002	1.0000002	-0.000429	-0.0000003
F15 Overlay:	0.000013	0.000005	1.0000005	1.0000003	-0.000279	-0.0000003
F17 Overlay:	0.000009	0.000001	1.0000002	1.0000004	-0.000155	-0.0000005
F19 Overlay:	0.000006	-0.000004	1.0000003	1.0000001	-0.000047	-0.0000002
F21 Overlay:	0.000010	-0.000002	1.0000002	1.0000003	-0.000480	-0.0000002
F23 Overlay:	0.000009	0.000002	1.0000000	1.0000001	-0.000226	0.0000000
F25 Overlay:	0.000014	0.000003	1.0000004	1.0000006	-0.000397	-0.0000005
F27 Overlay:	0.000007	-0.000001	1.0000000	1.0000004	-0.000175	-0.0000004
F29 Overlay:	0.000009	-0.000006	1.0000003	1.0000003	-0.000510	-0.0000003
F31 Overlay:	0.000012	0.000004	1.0000003	1.0000004	-0.000413	-0.0000002
F33 Overlay:	0.000003	-0.000002	1.0000002	1.0000000	-0.000364	0.0000001
F35 Overlay:	0.000009	-0.000003	1.0000004	1.0000000	-0.000393	-0.0000002
F37 Overlay:	0.000005	-0.000001	1.0000003	1.0000002	-0.000312	-0.0000001
F39 Overlay:	0.000012	0.000001	1.0000004	1.0000000	-0.000561	-0.0000002
F41 Overlay:	0.000008	-0.000000	1.0000003	0.9999998	-0.000197	0.0000000
F43 Overlay:	0.000007	-0.000000	1.0000003	0.9999999	-0.000451	-0.0000003
F45 Overlay:	0.000002	-0.000009	1.0000001	0.9999997	-0.000254	-0.0000002
F47 Overlay:	0.000007	-0.000001	1.0000003	1.0000000	-0.000334	-0.0000001
F49 Overlay:	-0.000007	0.000001	1.0000001	1.0000004	-0.000110	-0.0000001
F51 Overlay:	-0.000003	0.000003	1.0000001	1.0000002	0.000014	-0.0000000
F53 Overlay:	0.000004	-0.000005	1.0000005	0.9999996	-0.000218	-0.0000003
F55 Overlay:	0.000002	-0.000005	1.0000004	0.9999997	-0.000407	-0.0000001
F57 Overlay:	0.000004	-0.000006	1.0000002	0.9999992	-0.000592	-0.0000003
F59 Overlay:	-0.000000	-0.000007	0.9999995	0.9999992	0.000098	0.0000001

Overall Results

	X (mm)	Y (mm)	MagX (ppm)	MagY (ppm)	Theta(mrad)	Skew(mrad)
Mean (mm):	+0.000008	+0.000000	+1.000000	+1.000000	-0.000317	-0.000000
3Sig (mm):	+0.000016	+0.000014	+0.000001	+0.000001	+0.000523	+0.000000

	X (mm)	Y (mm)
Raw Mean (mm):	+0.000008	+0.000000
Raw 3Sig (mm):	+0.000026	+0.000021



X = 34nm, Y=21nm (μ+3σ) corrected

Figure 10. Mix and Match overlay results. The right hand image shows the print layout of the gate layer for a 300 mm wafer. The mean plus 3 sigma values in x and y were 34 nm and 21 nm, respectively.

e. Etch Results

Etch properties of the imprint resist were determined using a test template consisting of arrays of dense lines with half pitches ranging from 32 nm to 44 nm. The imprinted features are shown in Figure 11a. The feature profiles are nearly vertical, and the residual layer thickness is less than 15 nm. Pattern transfer consisted of a descum step to remove the thin residual layer, a hardmask etch, and an etch into the pattern transfer layer. Figures 11b and 11c show the final result. Cross section images are depicted in Figure 9b. CD is maintained, and aspect ratios of better than 4:1 were achieved. Top down SEMs (Figure 11c) show minimal line width roughness. Measured values of LWR ranged from only 1.8 nm to 2.6 nm, 3σ.

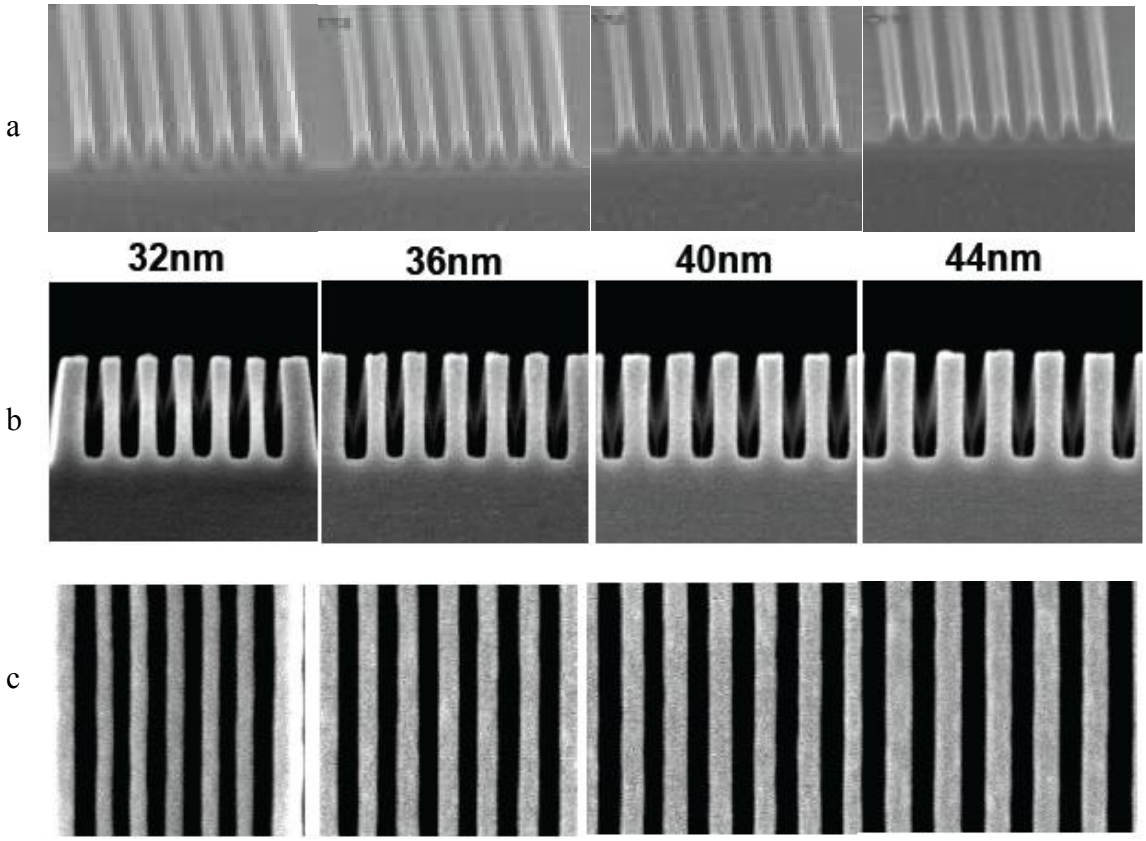


Figure 11. Pattern transfer process for dense features. a) Imprinted lines b) Cross section images after etch c) Top down images after etch. The final LWR ranged from only 1.8 nm to 2.6 nm, 3σ.

4. Conclusion

Previous results in fabricating imprint masks using variable shape beam generators were limited in resolution, primarily through the use of fast chemically amplified resists. By applying a high resolution ZEP520A resist process, a 38 nm half pitch NAND Flash gate level template was successfully fabricated. Resolution, CD uniformity, and image placement were excellent across the full field. The template was then used to imprint the device on 300 mm wafers using an Imprio 250 from Molecular Imprints. The pattern quality was excellent, and test features down to 32 nm half pitch were resolved. Mix and Match tests demonstrated overlay better than 30 nm, 3 sigma. Further reductions in overlay errors can be achieved by better control of thermal budgets and reductions in image placement and lens distortions. Pattern transfer experiments clearly resolved high aspect ration 32 nm half pitch lines with minimal line width roughness. Next steps include further improvements in both resolution and overlay in order to address 22 nm half pitch circuitry.

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