Step and Flash Imprint Lithography Templates for the 32 nm Node and Beyond

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Imprint lithography has been shown to be an effective technique for replication of nano-scale features (1). When the imprint material is a photocurable liquid, it is possible to perform the patterning process at low temperature and ambient pressure, which enables accurate overlay and reduces process defectivity (2). The resolution of the imprint approach is strictly dependent on the ability to create a 1X master template, and improvements in resolution can be achieved without new optical systems or photoresist materials. In this sense, imprint lithography is a multi-generational technique that can be used to facilitate device and process prototyping at several upcoming lithography nodes. This paper will provide a detailed description of processes that have been used to create imprint templates for patterning features relevant to semiconductor lithography at the 32 nm node. The prospects for extending the template fabrication process to 22 nm and below will also be discussed.

Step and Flash Imprint Lithography (S-FIL™) makes use of templates that can be fabricated with the same patterning and etch transfer processes that are used for manufacturing phase-shifting photomasks. Several commercial mask houses now accept orders for S-FIL templates, which are generally patterned at 1X using shaped-beam pattern generators. While shaped-beam tools achieve high throughput, Gaussian-beam tools offer a significant improvement in resolution. In this study, Gaussian beam tools were used to expose both ZEP positive resist and HSQ negative resist at 100 kV. The targeted feature types were chosen to be representative of a range of structures that are found in semiconductor devices, and were sized to meet the anticipated requirements of future lithography nodes. These features were patterned over large areas, and proximity effect corrections were applied.

Resolution in ZEP520A was enhanced by thinning the resist to 70 nm and applying a negative bias to the critical features. The improvement in process latitude is readily observed in Figure 1. 40 nm critical dimension control is enhanced by applying biases as large as 20 nm. The methodology was applied to 32 nm features and the results are depicted in Figure 2.

To fabricate a template, etch processes similar to those employed in a phase shift mask process are employed. Imprinted 32 nm features from templates made using a combination of an enhanced ZEP520A resist process and the template pattern transfer process described above are shown in Figure 3. The critical features are clearly resolved and little line edge roughness is observed in the Metal 1 and dense line patterns.

Further enhancements to the template fabrication process are possible by either improving the resolution of the ZEP520A or by using a high resolution HSQ negative resist. In Figure 4, well defined 20 nm patterns defined on a chromium on glass substrates are shown.

References:
Figure 1. Exposure latitude of ZEP520A resist as a function of feature bias.

Figure 2. 32 nm Metal 1 and 32 nm HP lines defined in ZEP520A.

Figure 3. 32 nm Metal 1 and 32 nm half pitch lines imprinted using the S-FIL process.

Figure 4. 20 nm half pitch lines, Metal 1, and Logic features formed in HSQ resist on a thin chromium and glass substrate.