Image placement issues for ITO-based step and flash imprint lithography templates

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Step and flash imprint lithography (SFIL) is an attractive, low-cost method for printing sub-100 nm geometries. The imprint process is performed at low pressures and room temperature, which minimizes magnification and distortion errors. Since SFIL is a 1× lithography technology, the template will require precise image placement in order to meet overlay specifications for multiple level device fabrication. In order to simplify the template fabrication process and facilitate post fabrication scanning-electron-microscope-based inspection, an integrated charge dissipation layer, such as indium tin oxide (ITO), is desired that is transparent to the SFIL exposure wavelength. The use of low-stress dielectric films such as SiON for the image relief layer minimizes the pattern distortions (<9 nm, mean$+3\sigma$) that occur after the pattern transfer process. Although ITO uniformity was also significantly improved by switching the ITO deposition process to an MRC sputter deposition system, image placement results were adversely affected. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1667512]

I. INTRODUCTION

Step and flash imprint lithography (SFIL) is an attractive imaging technology due to its potential for low cost and high throughput.[1–3] An added benefit comes from the use of optically transparent templates that can facilitate alignment. It is conceivable that SFIL will be entertained as a next generation lithography. For initial demonstration of the capabilities, SFIL can first be used for the nanofabrication of emerging market devices for which high resolution is required. Most of these applications either require only one level of printing or have relaxed overlay budgets for devices requiring multiple levels of printing. Examples of such devices include filters, waveguides, and photonic crystals. Most emphasis has been to fabricate single-layer devices or multiple-layer devices that have large layer-to-layer overlay budgets. For high-density silicon, there is concern that the requirements for positional accuracy are more stringent than reduction-based technologies. 1× SFIL templates will require high-resolution e-beam lithography systems to produce the relief images. State-of-the-art e-beam systems are capable of resolution to <20 nm and are typically specified to produce positional accuracy in the sub-30 nm ($m+3\sigma$) regime. The 2002 International Technology Roadmap for Semiconductors requires the wafer device layer-to-layer overlay specification in 2013 (32 nm node) to be 11 nm, and for the 22 nm node in 2016 to be 7.7 nm. These specifications create a significant challenge for SFIL template-to-template overlay requirements.

Early attempts at the fabrication of SFIL templates[4] entailed the use of 6 in.×6 in.×0.25 in. (6025) photomask substrates and leveraged mask shop knowledge of chrome and quartz phase-shift etch technology to create relief patterns directly in the quartz substrates. The chrome layer provides charge dissipation during the e-beam writing and is also used as an etch mask to define the final quartz features. However, once the pattern has been etched in quartz, the chrome is stripped and is no longer available for charge dis-

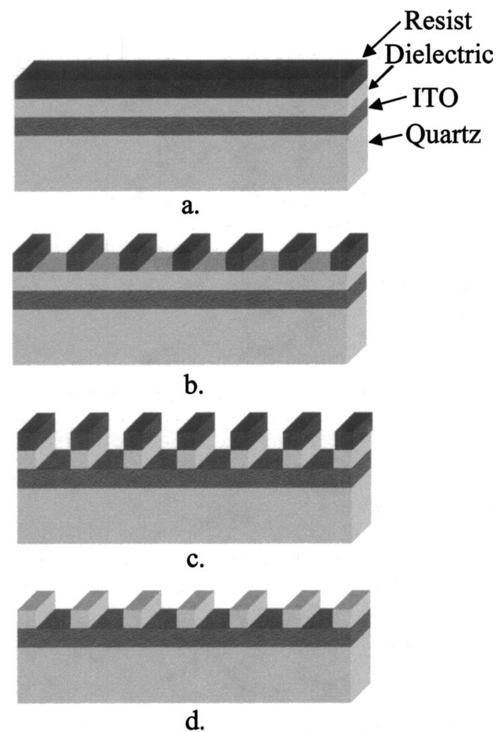

FIG. 1. Fabrication sequence for dielectric/ITO/quartz SFIL template. (a) Coat e-beam imaging resist, (b) expose and develop resist, (c) etch resist pattern into dielectric (SiO_2, Si_3N_4, SiON), and (d) strip resist.

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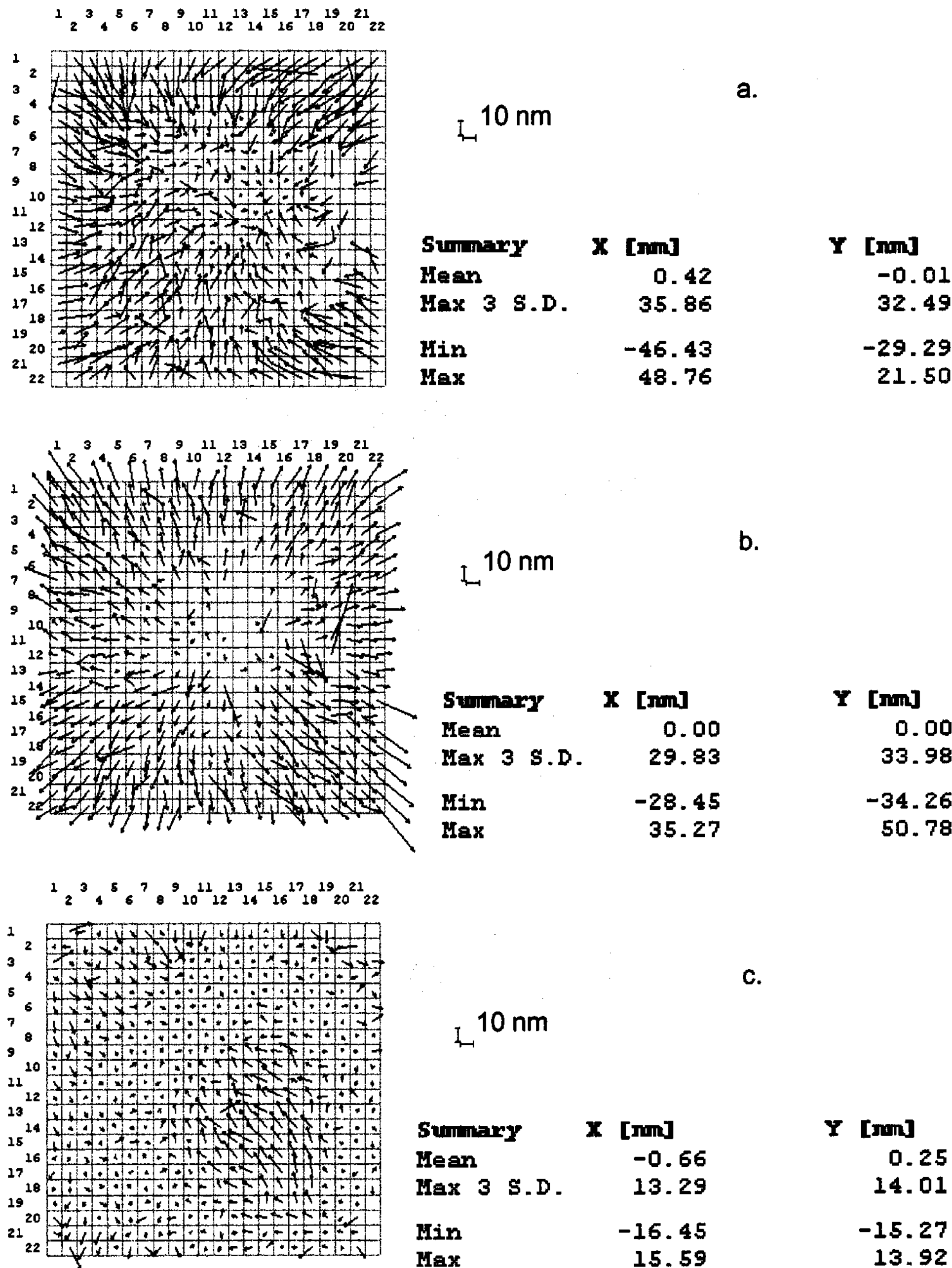


FIG. 2. LMS 2020 uncorrected 5 in.×5 in. (22×22 marks) image placement plots comparing final etched vs resist features for three dielectrics over 60 nm ITO on 6025 quartz: (a) 100 nm SiO_2, (b) 100 nm Si_3N_4, and (c) 100 nm SiON.

sipation purposes. Since the features on a typical SFIL template will be sub-50 nm, any post-fabrication inspection will most likely require scanning-electron-microscope-based instruments. This presents the problem of charge dissipation on the quartz template without providing additional conductive coatings. A solution to this problem would be to have an integrated charge dissipation layer, such as a transparent conducting oxide that is integral to the template structure, as illustrated in the fabrication sequence of Fig. 1.

Although there are many conductive oxides available for consideration, one prime candidate is indium tin oxide (ITO). Very recently, the concept of employing an oxide/ITO/6025 plate structure has been presented.[5,6] This form factor is advantageous, in that it provides for charge dissipation during e-beam writing, facilitates inspection, and offers the potential for high selectivity of oxide to ITO during a dry etch process. Many physical properties need to be addressed for the ITO film to comply with all the requirements for use with an SFIL template. These have been analyzed and characterized in an earlier study by Dauksher *et al.*[6] The typical depth of the relief features on a final SFIL template is 80 to 100 nm. This would require the top patterned relief layer coated over the ITO to be of comparable thickness: much thicker than the 15 nm chrome on the Cr/quartz template fabrication method. This thicker layer and the associated stress may be problematic when trying to control stress-induced image placement errors during the pattern transfer process.

Previous work with 15 nm chrome on quartz templates has shown that, although chrome stress has an effect on image placement before and after its removal from a 6025

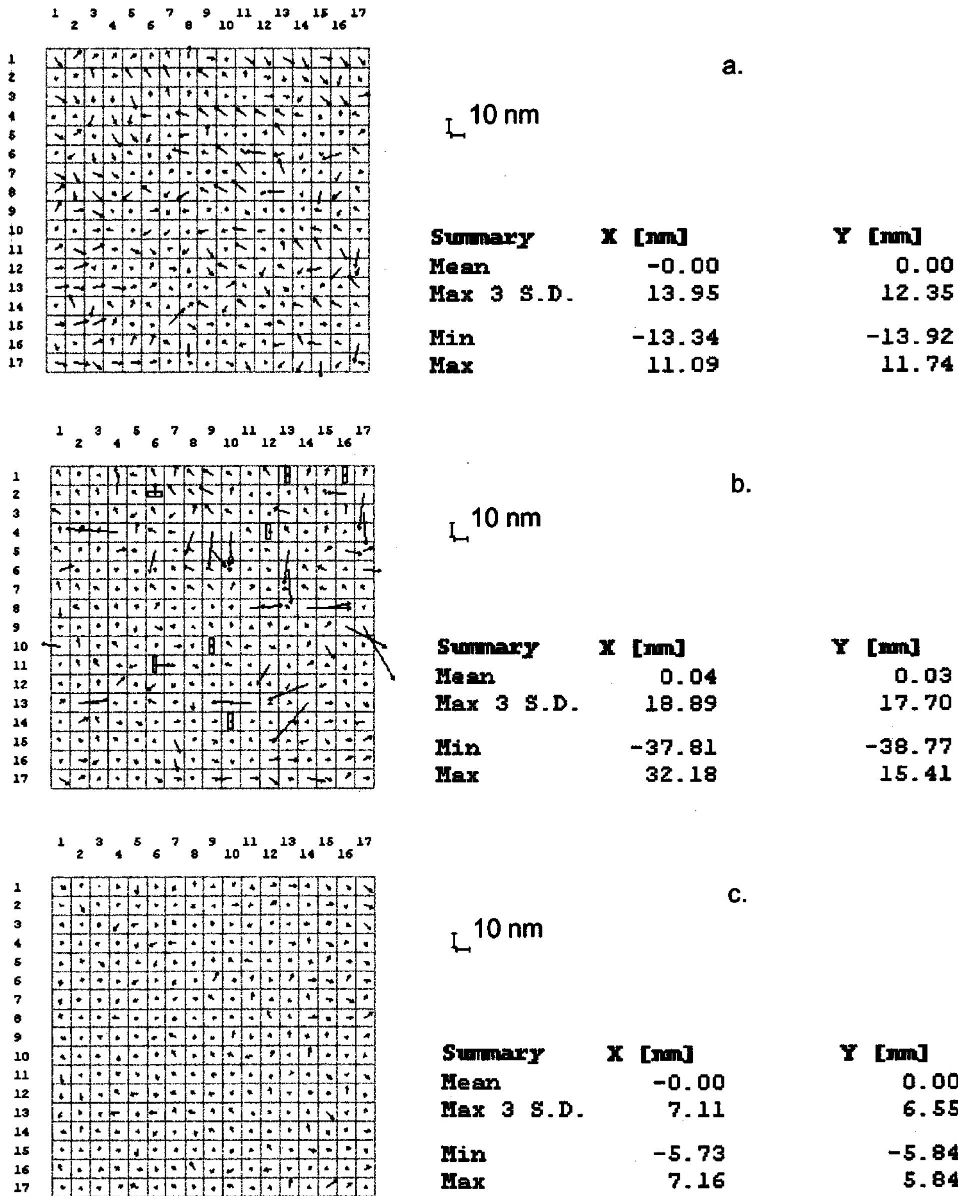


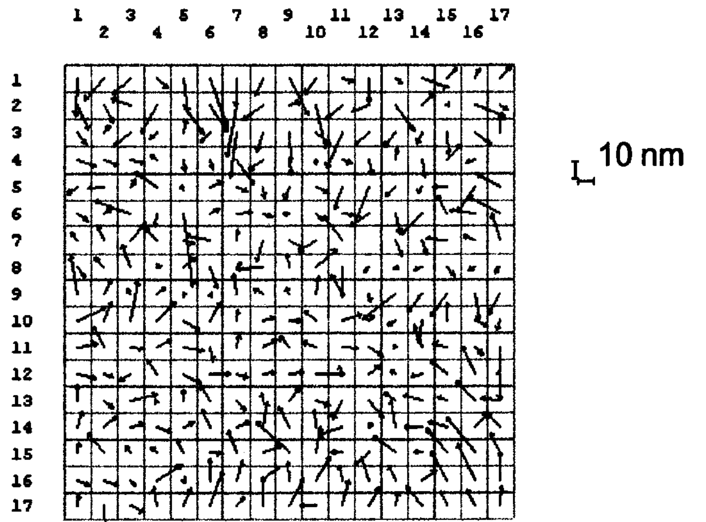
FIG. 3. LMS 2020 uncorrected 1 in.×1 in. (17×17 marks) image placement plots comparing final etched vs resist features for three dielectrics over 60 nm ITO on 6025 quartz: (a) 100 nm SiO_2, (b) 100 nm Si_3N_4, and (c) 100 nm SiON.

plate, the best template-to-template overlay can be accomplished by fabricating a single 1 in.×1 in. SFIL template at the center of the 6025 substrate.[7] The purpose of this work is to investigate the stress induced image placement errors of various dielectric materials that could be used on a dielectric/ITO/quartz template structure.

II. EXPERIMENT

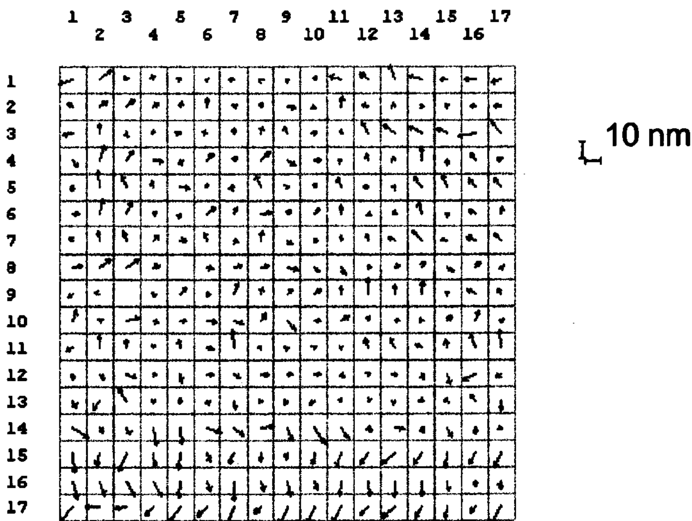
The tool used for template exposure for this study is a Leica VB6HR electron-beam system. The VB6 has a 100 keV thermal field-emission electron source and utilizes a 780 nm IR laser height sensor to measure and compensate for variations in substrate surface topology. The height compensation is necessary in order to correct for major field butting errors that can occur with surface nonplanarity, particularly from "sag" due to gravity effects on a 6025 plate. In order to reduce the contribution from interfield distortions, the 30 μm image placement marks were placed at the center of the major field. The masks were coated on an EV Group Inc. EV150 coater track system configured to handle the 6025 substrates in an automated cassette-to-cassette mode. An EV160 developer track configured for aqueous base development was used to develop the template imaging resist. Image placement accuracy was measured on a Leica LMS 2020 metrology system calibrated to the Leica quartz standard. The LMS consistently produces long-term measurement repeatability of 12 nm and short-term repeatability of $<$10 nm. All image placement data results are from the average of at least five readings for each array configuration, and all marks exhibiting poor mark detection were either eliminated from the datasets or indicated on the error plots by an error box. The resulting error numbers are determined from multipoint analysis. The LMS system also has a plate bow compensation algorithm that takes out the effects of plate sag.

The registration array consists of 25 1 in.×1 in. arrays



Summary	X [nm]	Y [nm]
Mean	0.00	0.16
Max 3 S.D.	20.25	26.76
Min	-19.38	-38.46
Max	16.07	20.77

a.



Summary	X [nm]	Y [nm]
Mean	-0.00	-0.22
Max 3 S.D.	9.28	12.63
Min	-9.07	-10.66
Max	7.79	8.66

b.

FIG. 4. LMS uncorrected image placement overlay plots comparing completed 1 in.×1 in. SFIL templates from two separate 6025 plates. (a) Two etched SiO_2/ITO/quartz templates and (b) two Cr/quartz templates.

(17×17 marks) in a 5×5 configuration filling a 5 in.×5 in. area centered on a 6025 plate. The array configuration was arranged to analyze the effects of film stress over the full 5 in.×5 in. area (22×22 marks) of the plate and also to analyze the effects of the smaller 1 in.×1 in. arrays that closely match the typical SFIL template format. Each 1 in.×1 in. SFIL array was written to completion before going to the next array, and they were sequenced from lower left of the 5×5 array to the upper right in a serpentine pattern. A negative chemically amplified resist, Sumitomo Chemical NEB22, was used to image the marks on the substrate. The pattern density of the full registration array was less than 1%, so that the pattern transfer process to image the relief layer effectively removes the bulk of the dielectric film, exacerbat-

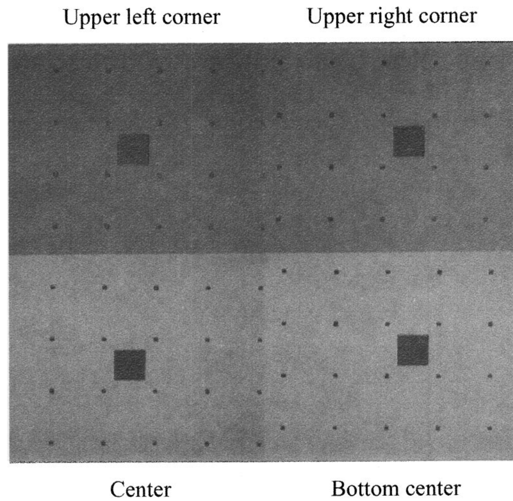


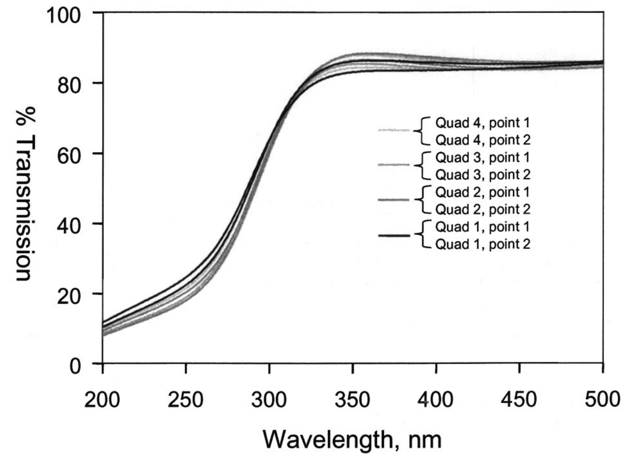
FIG. 5. Images of 4 and 30 μm registration marks illustrating optical contrast variations at four specified locations on a single oxide/ITO 6025 plate.

ing the effects of image placement errors due to film stress.

The substrates were 6025 fused silica quartz blanks polished on the image side to a 2 μm flatness. The ITO was deposited and annealed, followed by the deposition of the dielectric film into which the relief image will be etched (Fig. 1). The ITO layer on the initial samples consisted of a 60 nm film deposited by a Motorola-designed, manually operated, three-cathode (4 in.) sputtering system. The deposition pressure was maintained at 8×10^{-7} with an rf power of 100 W at 3 mT with Ar/O_2 and no pre-sputter surface preparation. The system, having been set-up for a 4 in. diameter target, provides a "sweet spot" at the center 4 in. of the 6025 plate, with progressively worsening uniformity out to the edge. This results in a poor overall film uniformity across a 6025 plate of $\pm40\%$. However, for a 60 nm annealed ITO film, the film resistivity measured approximately 270 ohms/sq and the optical transmission measured 85% at 365 nm. These values are satisfactory for charge dissipation and SFIL exposure tool wavelength transparency, respectively. After anneal, the 60 nm ITO film reached a stress of 200 MPa, tensile. The stress of the ITO film should not be a significant contributor to this analysis since the film remains intact during the entire process. The dielectric films selected for comparison were SiO_2, Si_3N_4, and SiON deposited with a low temperature (<250 °C) plasma-enhanced chemical vapor deposition process to a thickness of 100 nm. These three films were deposited on 6 in. Si wafers and measured on an FSM film measurement system resulting in values of 300 MPa (compressive) for the SiO_2, 300 MPa (tensile) for the Si_3N_4, and the SiON film stress was below the accuracy of the FSM measurement tool of ±30 MPa.

TABLE I. Comparison of ITO deposition tool parameters and characteristics.

Source to substrate	R&D 4.5 in.	MRC 603 1.5 in.
Deposition	Static	Dynamic
Target	4.5 in. diam	5 in.×15 in. rect.
RF power	100 W	500 W
Substrate loading	Air to air	Load lock
Film stress (800 Å, annealed)	−7.6e9 dynes/sq·cm	−8.1e9 dynes/sq·cm
Film uniformity	±40%	±5%
Film resistivity (800 Å)	200 Ω/□	350 Ω/□



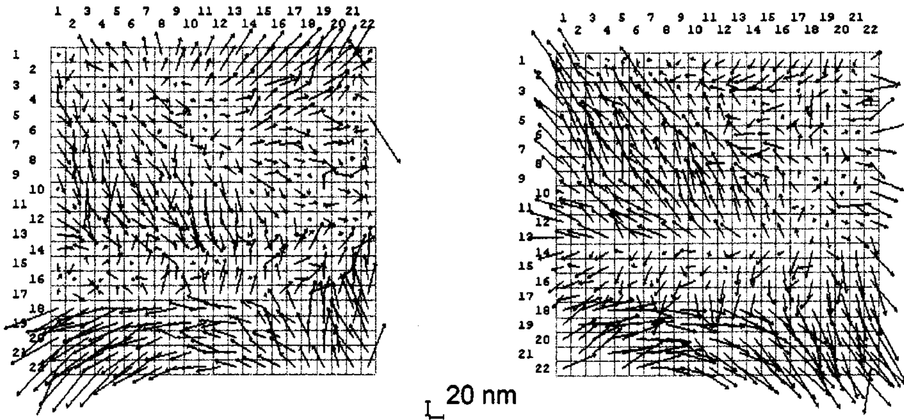
Quad	%T@365nm*
1	85%
2	87%
3	87%
4	86%

FIG. 6. UV/Vis spectrometer plot and 365 nm wavelength transmission table checking 80 nm ITO film uniformity on 6 in. quartz wafer coated by MRC 603 system.

III. RESULTS

Measurements using an LMS 2020 image placement system have been taken over a 5 in. area to investigate the effects of material stress before and after relief image etch for all three dielectric materials [Figs. 2(a)–2(c)]. Although the oxide- and nitride-coated plates had 3σ error values much higher that the oxynitride-coated plate, by putting in linear scaling corrections to compensate for the stress of the individual films, the 3σ error values for all three dielectric coated plates fell to within 12–17 nm. The scaling corrections applied to the data for the SiO_2-coated plate are 0.27 and 0.23 ppm in x and y, respectively; to the Si_3N_4-coated plate are −0.22 and −0.25 ppm in x and y, respectively; and to the SiON-coated plate are 0.04 and 0.03 ppm in x and y, respectively. The SiON-coated plate produced the minimum amount of film stress-induced image placement error. The 3σ values in x and y were 7.11 and 6.55 nm, respectively, less than the short-term repeatability of the LMS 2020. The difficulty in measuring transparent features on a transparent template with an optical metrology system is evidenced by the number of dropped sites and high individual site errors.

The 1 in.×1 in. SFIL templates at the center of the plates had high numbers of measurement errors due to the poor

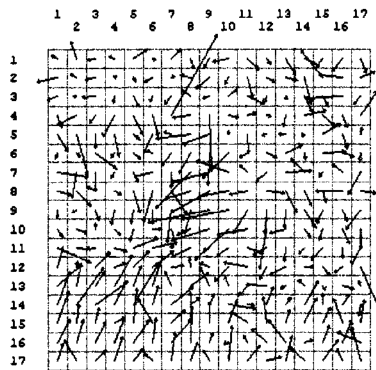


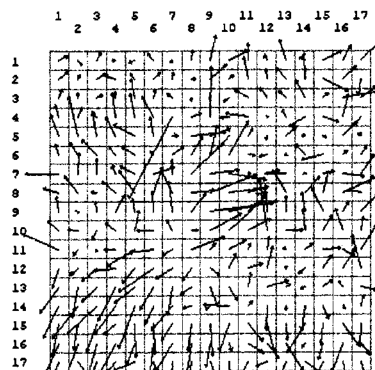
Summary	X [nm]	Y [nm]
Mean	0.00	0.00
Max 3 S.D.	72.42	76.46
Min	-79.63	-80.57
Max	46.90	73.72

a.

	X [nm]	Y [nm]
Mean	-0.00	0.02
Max 3 S.D.	82.58	89.34
Min	-52.41	-94.29
Max	65.62	82.04

b.





Summary	X [nm]	Y [nm]
Mean	-0.00	0.00
Max 3 S.D.	31.38	36.72
Min	-45.90	-41.40
Max	34.12	60.35

c.

	X [nm]	Y [nm]
Mean	-0.00	0.00
Max 3 S.D.	32.04	40.23
Min	-32.84	-60.45
Max	46.36	37.97

d.

FIG. 7. LMS uncorrected image placement error plots comparing final etched vs resist features for two 100-nm-thick dielectrics over 60 nm MRC 603 ITO on 6025 quartz: (a) 5 in.×5 in., Si_3N_4, (b) 5 in.×5 in., SiON, (c) 1 in.×1 in., Si_3N_4, and (d) 1 in.×1 in., SiON.

image contrast and difficulty for the LMS 2020 to detect the edges of the marks. For that reason, the SFIL array patterned just 1 in. to the lower left of the center of the 6025 substrate was selected, and the results of the before and after pattern transfer comparison are detailed in Figs. 3(a)–3(c). The Si_3N_4-coated plate produced the highest number of bad measurements, with the oxide-coated plate giving much lower errors when comparing the arrays before and after pattern transfer. The SiON-coated plate has the lowest image placement errors from the pattern transfer process. Comparing 1 in. SFIL arrays from two different oxide/ITO/quartz plates, shown in Fig. 4(a), reveals significantly larger magnitude random error vectors than those found on previously fabricated templates using the Cr/quartz process. The Cr/quartz template data were taken from the center arrays on two different 6025 plates.

There was great difficulty in measuring the ITO SFIL templates. The low signal contrast on the dielectric/ITO/quartz plates created difficulty when measuring the registration marks. This was due primarily to the poor ITO film uniformity from the R&D deposition tool. Although many of the primary characteristics of the ITO film were met, the film optical uniformity was hindered by the small target size of the tool. This optical nonuniformity was evident when measuring the marks across the 5 in.×5 in. array when the mark contrast varied from center to edge (Fig. 5). To improve film uniformity, an MRC 603 computer-controlled, vertical, three-cathode sputtering system was configured for an ITO

deposition process. A comparison of the two systems and the resulting film uniformity is detailed in Table I. Although the visual uniformity of the film was observed under reflected broadband light to be noticeably improved, the film still requires the proper transmission to ensure proper SFIL tool exposure uniformity. Ultraviolet/visible (UV/Vis) transmission analyses of the MRC ITO film were performed using a Perkin Elmer Lambda 18 UV/Vis spectrometer on four quadrants (two points/quadrant) of a 6 in. quartz wafer, and the results can be observed in Fig. 6. The transmission results reveal very good uniformity at the 365 nm wavelength. The ITO films from this system have met or exceeded all characteristics of the films deposited from the R&D sputter tool except for film resistivity (which was higher for the MRC-deposited film) and surface roughness. The increase in surface roughness is attributable to the polycrystalline nature of the as-deposited MRC 603 films. The rms surface roughness increased from 0.24 nm for the R&D tool to 0.59 nm for the MRC system, but was acceptable for this study.

Although the MRC has shown ITO film improvement in many areas, the adverse effects on pattern placement accuracy before and after the pattern transfer process are not well understood. The LMS error plots in Fig. 7 show the large 5 in.×5 in. array pattern before and after the dielectric layer etch for a Si_3N_4/ITO/quartz [Fig. 7(a)] and a SiON/ITO/quartz plate [Fig. 7(b)]. There are significant image placement distortions on the 5 in.×5 in. array that far exceed any stress related effect of dielectric material. The 1 in.×1 in. array plots show large random error vectors for both the Si_3N_4- and SiON-coated plates, much higher than samples from the R&D ITO deposition tool. The errors associated with the MRC ITO film were unexpected and need to be investigated further.

IV. CONCLUSION

Using low-stress materials for the top relief image layer on ITO/quartz SFIL templates is crucial for ensuring good image placement accuracy through the pattern transfer process. Specifically, the use of SiON as the top relief image layer provides the best approach for mitigating film stress-induced image placement error. ITO thickness uniformity was drastically improved by switching the deposition process to an MRC 603 sputter deposition system. However, there is evidence that the ITO layer also has an indirect but equally important role in maintaining good image placement control. The MRC ITO appears to be inducing a stress gradient either alone, or in conjunction with, the dielectric film that is exacerbated by the etch process. The shorter substrate-to-source distance coupled with the higher rf power during the MRC deposition may result in higher deposition temperatures and may effect the as-deposited film composition. The cause of this stress gradient is unknown and will be a subject for further investigation.

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[1]T. Bailey, B. J. Choi, M. Colburn, M. Meissl, S. Shaya, J. G. Ekerdt, S. V. Sreenivasan, and C. G. Willson, J. Vac. Sci. Technol. B **18**, 3572 (2000).
[2]M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S. V. Sreenivasan, J. Ekerdt, and C. G. Willson, Proc. SPIE 379 (1999).
[3]M. Colburn, T. Bailey, B. J. Choi, J. G. Ekerdt, and S. V. Sreenivasan, Solid State Technol. 67 (2001).
[4]M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S. V. Sreenivasan, J. Ekerdt, and C. G. Willson, Proc. SPIE **3676**, 171 (1999).
[5]T. C. Bailey *et al.*, Microelectron. Eng. **61**, 461 (2002).
[6]W. J. Dauksher *et al.*, J. Vac. Sci. Technol. B **20**(6), 2857 (2002).
[7]K. J. Nordquist, D. P. Mancini, W. J. Dauksher, E. S. Ainley, K. A. Gehoski, D. J. Resnick, Z. S. Masnyj, and P. J. Mangat, Proc. SPIE **4889**, 1143 (2002).