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Abstract. Acceptance of imprint lithography for manufacturing will require demonstration that it can attain defect levels commensurate with the defect specifications of high-end memory devices. Defects occurring during imprinting can generally be broken into two categories; random defects and repeating defects. Examples of random defects include fluid phase imprint defects, such as bubbles, and solid phase imprint defects, such as line collapse. Examples of repeater defects include mask fabrication defects and particle induced defects. Previous studies indicated that soft particles cause nonrepeating defects. Hard particles, on the other hand, can cause either permanent resist plugging or mask damage. In a previous study, two specific defect types were examined; random nonfill defects occurring during the resist filling process and repeater defects caused by interactions with particles on the substrate. We attempted to identify the different types of imprint defect types using a mask with line/space patterns at dimensions as small as 26 nm. An Imprio 500 twenty-wafer per hour development tool was used to study the various defect types. The imprint defect density was reduced nearly four orders of magnitude, down to ~4/cm^2 in a period of two years following the availability of low defect imprint masks at 26-nm half-pitch. This reduction was achieved by identifying the root cause of various defects and then taking the appropriate corrective action. [DOI: 10.1117/1.JMM.11.3.031404]

Subject terms: jet and flash imprint lithography; imprint lithography; defectivity; semiconductor imprint lithography.

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1 Introduction

Imprint lithography has been shown to be an effective technique for replication of nanoscale features.[1,2] Jet and flash imprint lithography (J-FIL™) involves the field-by-field deposition and exposure of a low-viscosity resist deposited by jetting technology onto the substrate.[3–8]The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed leaving a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10 nm (Fig. 1), making the technology suitable for the printing of several generations of critical memory levels with a single mask.[9] In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there is no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single-level processing and zero waste, leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. On the mask side, there are stringent criteria for mask blank defectivity, critical dimension uniformity (CDU), image placement (IP), and imprint defectivity. The master mask blank, which consists of a thin (<10 nm) layer of chromium on the $6 \times 6 \times 0.25$ in. fused silica was recently reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50-nm sensitivity.[10] The remaining three criteria have targeted values of 2 nm, 3 nm, and 0.1/cm^2, respectively. Presently Dai Nippon Printing, Co., Ltd. (DNP) has exceeded the targets for both CDU and IP, and is rapidly approaching defect levels of 1/cm^2 as measured by an Hermes Microvision Incorporated electron beam mask inspection tool with a sensitivity of <20 nm, before any repair.[10]

With respect to the imprint stepper, both CDU and line-edge roughness meet the criteria of 2 nm. Toshiba has achieved overlay of 10 nm (with a target of 8 nm)[11] and resist fill time, which is the key parameter for addressing the throughput requirement of 20 wafers per hour (wph) for a single imprint module, is within 20% of meeting its target of 1 s.[12]

It is reasonable to conclude, therefore that the acceptance of J-FIL technology for the manufacturing of nonvolatile memory will require a demonstration that it can attain defect levels commensurate with the defect specifications of high-end memory devices. Typical defectivity targets are on the order of 0.10/cm^2.

Defects that occur during imprinting can generally be broken into two categories; random defects and repeating defects. Examples of random defects include plug defects, line collapse, line shearing, and nonfill defects. Examples of repeater defects include mask defects and particle induced defects. Previous studies indicated that soft particles tend to cause nonrepeating defects. Hard particles, on the other

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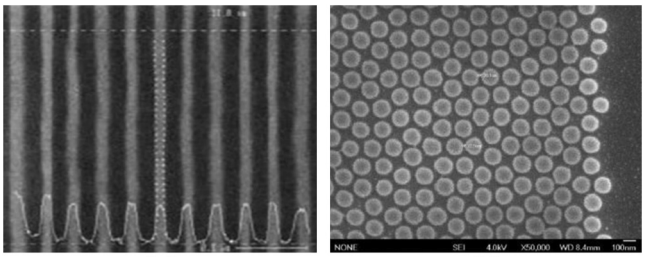


(a) (b)

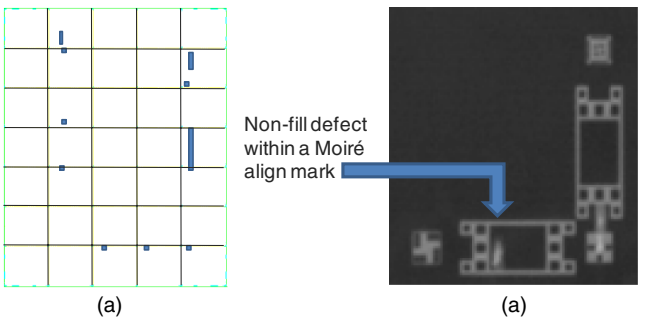
Fig. 1 (a) 11-nm half pitch lines. (b) Imprinted bit-patterned media pattern. Spacing between the bits is approximately 7 nm.

hand, can cause either permanent resist plugging or mask damage. In a previous study, two specific defect types were examined; random nonfill defects that occurred during the resist filling process, and repeater defects caused by interactions with particles on the substrate.

Nonfill defectivity must always be considered within the context of process throughput. Processing steps such as resist exposure time and mask/wafer separation, are well understood and typical times for the steps are on the order of 0.10 to 0.20 s. To achieve a total process throughput of 20 wph, it is necessary to complete the fluid fill step in 1.0 s, making it the key limiting step in an imprint process. A nonfill defect density of 1.2 def/cm^2 was demonstrated at fill times of 1.5 s. For longer fill times, the defectivity dropped to zero. More recently, defect densities of <1.0 def/cm^2 have been achieved at a fill time of 1.2 s by reducing resist drop size and optimizing the drop pattern. It is interesting to note that all of the nonfill defects occurred either at boundaries where pattern densities were significantly different or near the Moiré align marks (Fig. 2). Both defects can likely be addressed with specific imprint patterns (such as dense line dummy patterns) designed to enhance filling in these areas.

By performing an extended imprint run, repeater defects not attributable to the imprint mask were identified and examined, and all were found to contain nickel. It was noted that both the inkjet dispenser and the filter unit contained within the imprint tool both contain nickel parts.

Recent studies have marked excellent progress in reducing defects on the imprinted wafer. Sematech has demonstrated short-run imprint defectivity of only 0.09/cm^2 as measured by a KLA-T 28xx wafer inspection tool with sensitivity on the order of 30 nm.[13] However, this study



(a) (a)

Fig. 2 (a) Field defect map showing the locations of nonfill defects using a fill time of 1.5 s. (b) An example of a nonfill defect within a printed Moiré align mark.[12]

was limited to patterns with a minimum feature size of 100 nm.

Because of these studies, we attempted to identify the critical imprint defect types using a mask with NAND flash-like patterns at dimensions as small as 26 nm. The three key defect types identified were plug defects induced by small particulates, shearing defects resulting from different pattern densities with the field, and airborne contaminants which result in local adhesion failure. After identification, the root cause of the defect was determined, and corrective measures were taken to either eliminate or reduce the defect source. As a result, we have been able to reduce defectivity levels by three orders of magnitude in only 12 months. In the following sections we present the experimental details used to perform the experiments and discuss the fixes necessary to drive down defectivity.

2 Experimental Details

2.1 *Imprint Process*

To generate the inspection test masks, patterns were exposed by Dai Nippon Printing using a NuFlare EBM7000 shaped beam pattern generator. ZEP520A resist was chosen as the positive imaging resist. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process were employed to create a finished imprint mask for the Imprio 500 tool.

The mask patterns chosen for defectivity evaluation had an industry standard 26 × 33 mm field size. Die within the field consisted of 26 to 50-nm flash device-like gate patterns and dummy fill die surrounding the device die. The mask also included peripheral structures, such as align marks and metrology marks. A representative schematic of the mask layout is shown in Fig. 3.

Imprinting of the masks was performed using a Molecular Imprints Imprio® 500 imprint tool. A drop-on-demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across 300-mm silicon wafers. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process were previously reported.[14,15] Both wafer throughput and overlay are improved on the Imprio 500 system relative to the Imprio 300. Throughput and mix-and-match overlay are specified at 20 wph and

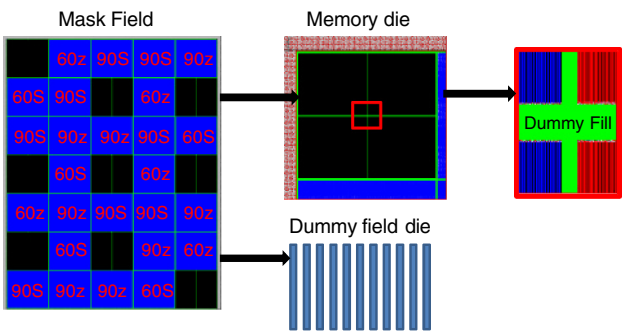


Fig. 3 Mask layout used for studying nonfill defects.

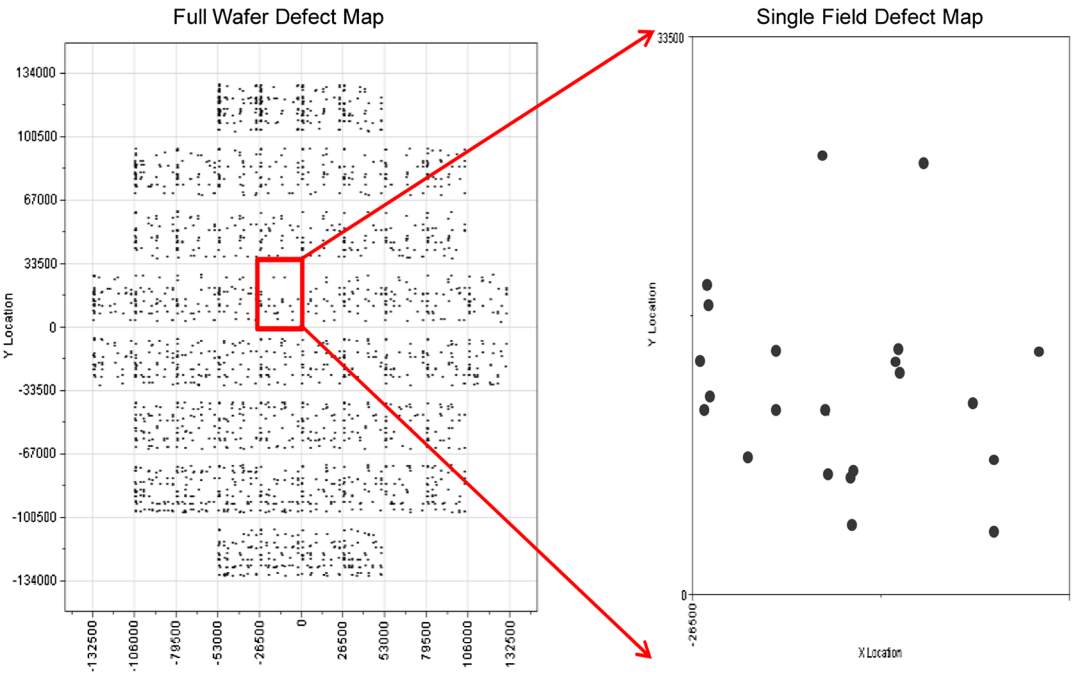


Fig. 4 (a) Defect map across an entire 300-mm wafer. (b) Defect map of a single imprint field.

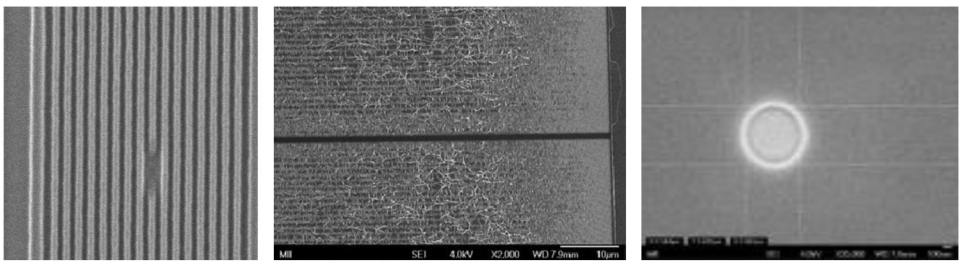


Fig. 5 (a) Line break defect, (b) feature shearing defect, and (c) contamination void defect.

15 nm, 3 sigma, respectively. The best overlay achieved to date was 10 nm and was reported last year by Toshiba.[11]

2.2 *Inspection Details*

Defectivity was measured on KLA-Tencor 28xx wafer inspection tools. All inspections were performed in array mode with a pixel setting of 0.23 μm. The tools were capable of detecting either line breaks or shorts in the 26 and 28-nm patterns. Typical imprint defect maps for the 26-nm patterns of an inspected wafer and an inspected field are shown in Fig. 4.

At the beginning of this study, imprint defectivity was as high as 10^4 defects/cm^2. Scanning electron microscope (SEM) review of the defects indicated that there were three primary defect types:

- Line break defects: This is the most common defect. Typical breaks in the pattern are generally limited to a single line, but are occasionally viewed across two or three lines.

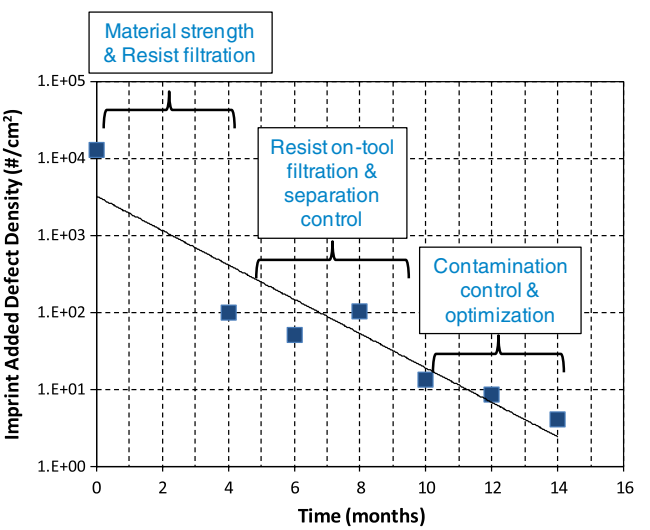


Fig. 6 Added defectivity as a function of time. A reduction of more than three orders of magnitude (best line fit) was realized within a 14 month time period.

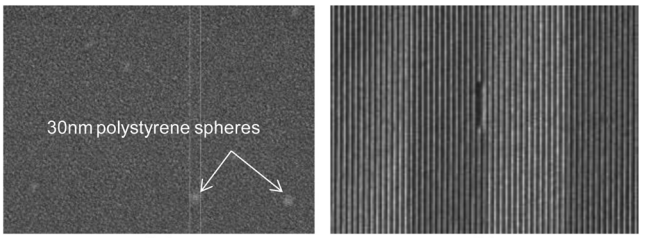


Fig. 7 (a) Polystyrene spheres introduced on to the wafer surface prior to imprinting. (b) Line break defect induced by a polystyrene sphere.

- Feature shearing: This defect type occurs during the mask and wafer separation process, and is typically seen in areas where there is a significant difference in pattern density.
- Contamination defect: This type of defect appears as either as an adhesion failure between the adhesion layer and the imprint resist or as an area where resist does not fill the mask. The affected area generally covers a diameter of a few 100 nm.

Examples of all three defect types are shown in Fig. 5.

3 Defect Results

Figure 6 shows the progress made in defectivity over the last 13 months. Defectivity has dropped by over three orders of magnitude. This was accomplished, first by identifying possible root causes, and then applying modifications to the imprint process. Possible root causes included material (resist) strength, particles deposited during the jetting process, anomalies in the mask to substrate separation phase of the imprint sequence, and local contamination of the adhesion layer prior to imprinting. Each potential defect mechanism is discussed in Sec. 3.1, 3.2, and 3.3.

3.1 *Resist Properties: Material Strength and Material Filtration*

J-FIL uses an acrylate-based liquid resist with components including a monomer, a crosslinking agent, and a free radical generator.[3,16] Resist strength, or modulus, plays a significant role during separation of the wafer and substrate. Table 1 shows the characteristic properties for the last three generations of resist. In 2011, the focus was primarily on etch resistance. In the latest generation, more attention was given to resist spreading velocity (hence the lower viscosity) and tensile modulus. These attributes help to minimize nonfill defectivity and increase material strength.

It was also believed that many of the defects were a result of insufficient filtering of the resist. It was noted that when 50-nm dense lines were printed, there was almost no occurrence of line break defects. At 28 nm, the number of line breaks increased significantly. To understand whether line breaks could be caused by very small particles, the number of particles residing on the silicon substrate was substantially increased by deliberately introducing ~30-nm diameter polystyrene spheres so that almost high resolution SEM image, with a field of view only a few microns, would contain polystyrene spheres (Fig. 7). The wafers were then imprinted and hundreds of SEM images were captured and inspected for line breaks. Every image contained line break defects. The majority of these defects were confined to a single line.

Table 1 Material properties of the imprint resist over the last three years of development.

Property	FT247A (2010 POR)	FT353A (2011 POR)	FT385A (2012 POR)
Viscosity	10 cPs	11 cPs	7 cPs
Tensile modulus	0.9 GPa	1.0 GPa	1.3 GPa
UV dose	100 mJ/cm^2	75 mJ/cm^2	75 mJ/cm^2
Separation force	Baseline	Baseline	10% lower
Etch (O_2/Ar)	Baseline	15%–20% slower	15%–20% slower

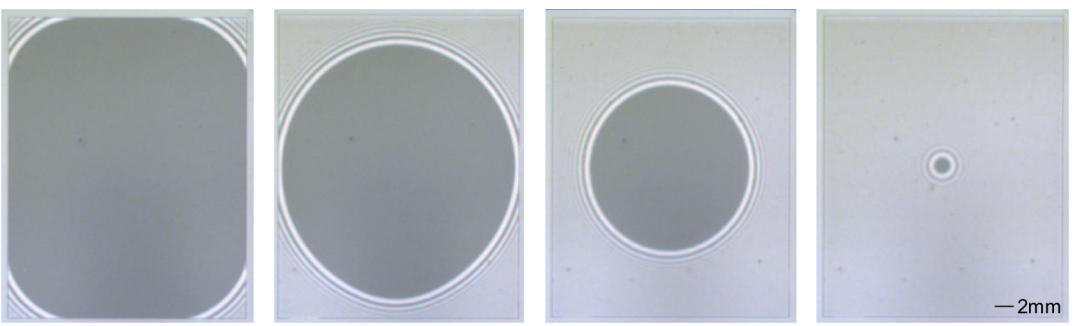


Fig. 8 Separation of the template and wafer over a period of 0.30 s, showing a uniform and symmetric separation front.

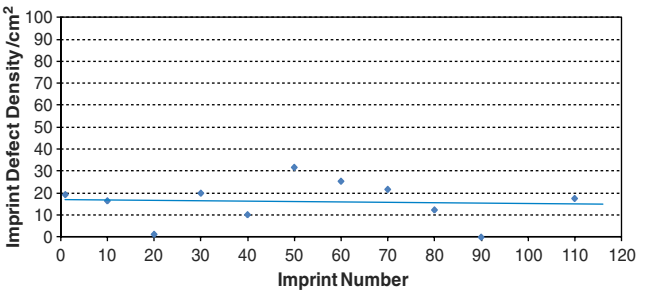


Fig. 9 Defect density is plotted as a function of the number of imprints. The defectivity slope (plotted as a best line fit) is essentially flat.

To remedy this, the first step taken was to filter the resist multiple times using a 10-nm filter. The combination of a 30% improvement in material strength and reduced particulates in the resist immediately reduced the number of line break defects, dropping the defect density by more than two orders of magnitude in only four months.

3.2 *On-Tool Particle Reduction and Separation Control*

With the defectivity reduced to $\sim 100/\text{cm}^2$, the possibility of particulates generated from within the imprint tool was examined. In addition the separation algorithm used to release the imprint mask from the resist was explored.

Again, the primary source of defects within the tool was attributed to the resist. Previous studies demonstrated that the movement within the imprint tool itself creates <0.1 defects per wafer pass. To further address defects generated in the dispensing process, a second filtration step was added to the imprint system. An on-tool 10-nm filtered recirculation system located adjacent to the inkjet dispenser was incorporated into the resist dispense system.

In addition to on-tool resist filtration, the separation algorithms of the Imprio 500 were upgraded to produce a uniform separation front. Inconsistent separation caused either by variations in pattern density or poorly controlled separation velocity is known to cause shearing defects, as shown earlier in Fig. 5(b). By modifying the tool algorithms, the separation velocity front is now well controlled (Fig. 8). Pictured is the release of the template field from silicon wafer over a period of 0.30 s. The combination of filtration and separation front control decreased defectivity by another order of magnitude to $\sim 10/\text{cm}^2$.

3.3 *Environmental Control*

The contamination voids referenced in Fig. 5 are believed to result from environmental factors that locally degrade the adhesive properties of the adhesion deposited prior to the imprint process. It is believed that moisture may be adsorbed on the surface of the adhesion layer, thereby causing local adhesion failure or disrupting the filling of the liquid resist. By taking precautions, such as storing wafers in a nitrogen environment prior to printing and by adding carbon filtration systems, these defects are virtually eliminated. After implementing these controls and further optimizing the drop pattern and the separation front, an additional reduction was achieved to bring the defect density down to $4.02/\text{cm}^2$.

3.4 *Next Steps*

From the previous work, nonfill defects contribute about $1/\text{cm}^2$ to the total. Further studies will be required to reduce the overall defectivity to $<1/\text{cm}^2$. Additional improvements in the resist, in filtering, and in separation control will also play a role in reducing defectivity. Once this is achieved, additional analysis will be required to identify the root cause of the remaining defects and put solutions in place to eliminate them.

The final challenge then becomes controlling soft and hard particles from either the wafer or the imprint tool, to allow imprinting for extended periods of time without adding to the overall defectivity. The target for this work is $>50,000$ imprints at defect densities $<1/\text{cm}^2$. Recent imprint runs show a defect slope that is essentially flat (Fig. 9). The noise in the data indicates that the majority of particles encountered are soft (and most likely due to contamination voids), and do not add to the overall permanent defect count.

It is also encouraging to note that this process is robust, as evidenced by the fact that even over a run of >1800 imprints, permanent defects do not cause either additional defects or cause the affected area to grow in defect size (Fig. 10).

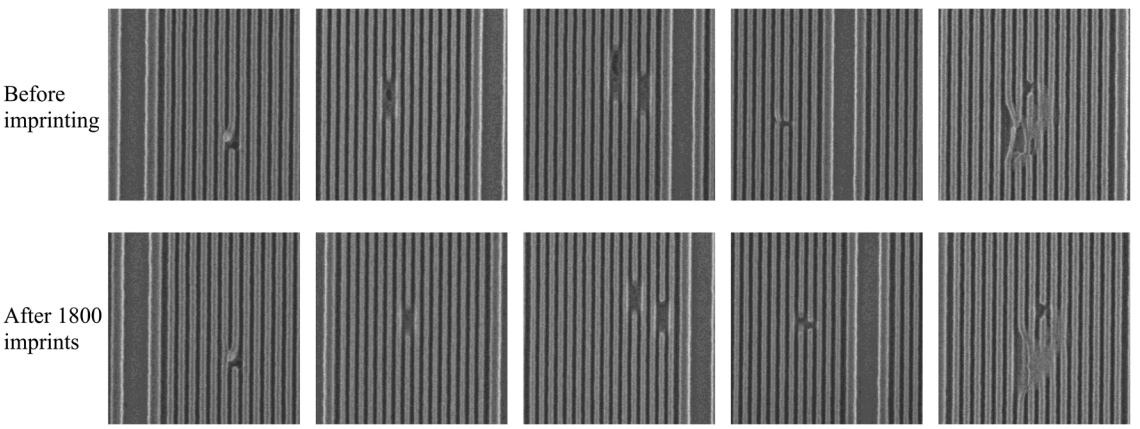


Fig. 10 Permanent defects at the start of an imprint run and after 1800 imprints.

4 Conclusions

Excellent progress was made on reducing defectivity. A mask blank defectivity of $0.04/\text{cm}^2$ has already been demonstrated and patterned mask defectivity has been reduced to less than $10/\text{cm}^2$ (without mask repair). In this work, substantial improvements were made to the resist, the resist filtration system, the algorithms used to separate the template and wafer, and wafer handling to control environmental effects. Imprint related defectivity is now $\sim 4/\text{cm}^2$ with a defect slope that is essentially flat. Toshiba recently completed electrical tests of 26-nm serpentine patterns and has demonstrated yields of ~65% for 10-m long test structures.[17] An additional order of magnitude is still required to move the process to production, however. Further refinements of the imprint process combined with the identification of the root cause of the last few defects will enable the production of low-cost lithography for the nonvolatile memory market.

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Biographies and photographs of the authors are not available.