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Tatsuhiko Higashiki
Tetsuro Nakasugi
Ikuo Yoneda

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Tatsuhiko Higashiki
Tetsuro Nakasugi
Ikuo Yoneda
Toshiba Research and Development Center
Device Process Development Center
8 Shinsugita-cho, Isogo-ku
Yokohama City 235-8522, Japan
E-mail: tatsuhiko.higashiki@toshiba.co.jp

Abstract. Nanoimprint lithography (NIL) has the potential capability of high resolution with critical dimension uniformity that is suited for patterning shrinkage, as well as providing a low cost advantage. However, the defectivity of NIL is an impediment to the practical use of the technology in semiconductor manufacturing. We have evaluated defect levels of NIL and have classified defectivity into three categories; nonfill defects, template defects, and plug defects. New materials for both the template and resist processes reduce these defects to practical levels. Electric yields of NIL are also discussed. [DOI: 10.1117/1.3658024]

Subject terms: nanoimprint; lithography; template; defectivity; overlay accuracy; critical dimension uniformity; lithography investment.

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1 Introduction

Circuit patterns of semiconductor devices require continuous pattern shrinking to keep up with Moore's law. Recently, argon fluoride (ArF) immersion lithography has been combined with double patterning and is one of the leading candidates for lithography with a half pitch of 30 nm (hp 30 nm) and beyond. However, ArF double patterning is a very complicated and expensive process. The minimum half pitch resolution of ArF immersion systems is 40 nm, thereby limiting the resolution limit of ArF double patterning to around 20 nm. As a result, new lithographic solutions will be required for half pitches less than 20 nm. Nanoimprint lithography (NIL) and extreme ultraviolet lithography (EUVL) with high numerical aperture will be candidates for these aggressive half pitches. Because the cost of lithography plays a critical role in semiconductor manufacturing, the lithographic solution for future nodes needs to be based on both technical innovation and economy. There are big challenges in implementing EUVL as a lithographic solution. Included in the list of issues to be addressed are source power, mask infrastructure, resist performance, and tool cost. In addition to addressing cost, NIL has already demonstrated both high resolution,[1] excellent critical dimension uniformity (CDU),[2] and low line width roughness.[3] The practical use of implementing imprint as a manufacturing solution is predicated on reducing defectivity and template lifetime to acceptable levels. In this work, we address the progress made in critical dimension (CD), overlay, template fabrication, and defectivity reduction specifically for the semiconductor market. The concept of desktop lithography is also discussed as a tool for studying tribology (see Fig. 1).

2 NIL in Semiconductor

2.1 *Exposure Tool*

The jet and flash imprint lithography (J-FIL) process used by Molecular Imprints Incorporated (MII) is schematically shown in Fig. 2.[4–8]

The process starts with a template made from a standard 6025 photomask blank. Patterns are written using advanced shaped beam pattern generators, and then etched into the glass using the same technology that is used for phase-shifting mask fabrication. The imprint resist is formed from an array of picoliter sized drops that are correlated with the pattern density on the template. The resist spreads across the imprint field as the template is lowered onto the drop array. When the surface tension of the liquid phase imprint resist has been broken, capillary action draws the resist into the template features. Once filling is completed, ultraviolet (UV) light is projected through the back side of the glass template, thereby driving a cross-linking action that converts the resist to a solid. The template can then be withdrawn and the process can be repeated on the next field. The J-FIL tool made by MII is the preferred imprint tool for semiconductor fabrication for the following three reasons:

1. The template and wafer do not make contact as a result of applying a low viscosity UV curable imprint resist.
2. Dispensed drops are arranged relative to the pattern density of the layout, thereby creating uniform residual layers.[9]
3. Intrafield overlay errors can be compensated by using a force feedback magnification actuator system and a highly sensitive Moiré alignment technique.[10]

Critical dimension uniformity is expected to be superior to more conventional projection lithography, since the patterned feature is not dependent on an aerial image. If the template has good CD control, then little change in CDU is expected as a result of the imprint process. Using a high resolution resist, it is possible to form high resolution patterns with a CDU of close to 1 nm (3σ). To test this premise, a dense array of 28 nm half pitch lines were formed on a template and then printed on a 300 mm wafer. Figure 3 shows the resulting CDU of the 28 nm patterns imprinted by the MII tool. The CDU for 240 measurements (12 sites/shot and 20 shots/wafer) was only 1.2 nm, 3σ.

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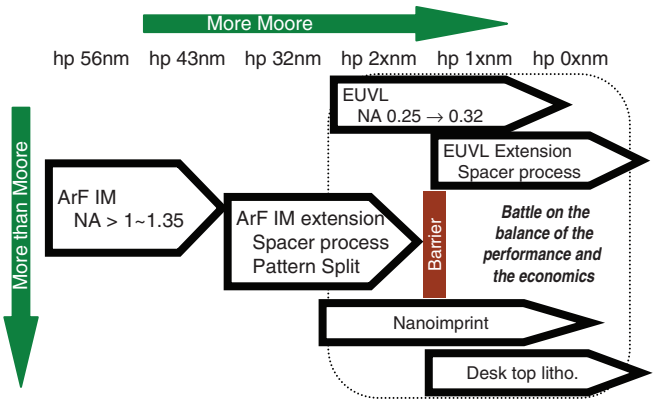


Fig. 1 Lithography roadmap.

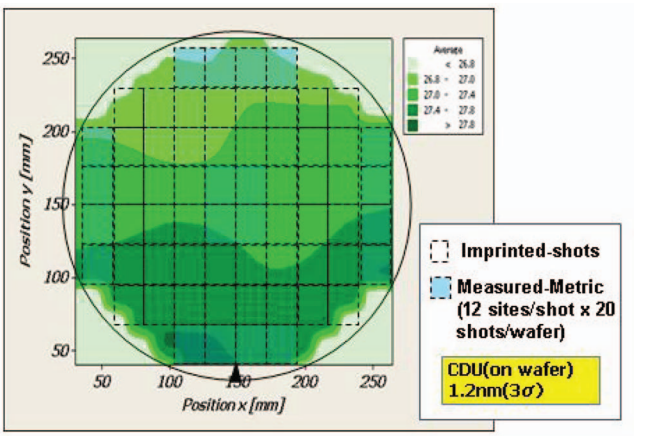


Fig. 3 CD uniformity of 28 nm half pitch dense patterns. CDU is 1.2 nm, 3σ.

Because imprint lithography does not require a projection lens, overlay accuracy cannot be influenced by any distortion caused by the aberration of the lenses. The concern for NIL is that the pattern magnification is 1 to 1. As a result, pattern placement errors on the template are limited to only a few nanometers. An analysis of the overlay errors after imprint indicates that the primary error source is in fact the registration errors introduced by the electron beam writer. Registration performance of the writers is improving however, and image placement errors of less than 5 nm (3σ) have been demonstrated,[11] as shown in Fig. 4.

By using templates with improved image placement, errors on printed wafers of only 10 nm have been demonstrated. The results of a recent test are shown in Fig. 5.[12,13] In this demonstration, two templates were fabricated independently using a NuFlare EBM6000, an electron beam writer.[14] These templates have a shot size of 15 mm × 15 mm and contain an overlay metrology mark set consisting of 92 locations per shot. The first layer template was used for the initial patterning of the 300 mm silicon wafers. After imprinting, the features were transferred to the substrate film by reactive ion etching. Then a second layer template was imprinted, using a die by die alignment to the underlayer marks utilizing MII's interferometric Moiré alignment technique.

Both layers were imprinted with the same Imprio-250 system which has a total magnification range of 7 ppm and resolution better than 0.1 ppm. The overlay performance was measured with an Archer AIM system at all 92 locations per shot, 5 shots per wafer. The resulting error vectors, as shown in Fig. 5, were 10.6 and 11.3 nm, respectively in x and y. The image placement error of each template was estimated to be around 5 nm 3σ. Assuming there is independency in image placement between the two templates, a simple root-mean-square analysis would indicate that the imprint process contribution to the distortion component is approximately 8 nm. It is important to note that this result was obtained with a prototyping tool. Further improvements overlay are expected through reduced image placement errors on the template, better thermal management in the imprint tool, and forced feedback control of the magnification actuators. Furthermore, because imprint lithography eliminates any lens aberration error typically encountered in optical projection lithography,[12] a target overlay error of 6 nm should be possible.

2.2 *Template*

NIL templates are fabricated with the same photomask materials and patterning processes that are used to create 4× reduction photomasks. The substrate format has dimensions of 6 in. × 6 in. × 0.25 in., and is typically referred to as 6025 mask. The choice of form factor is critical, since it enables a mask shop to utilize the same tools and infrastructure

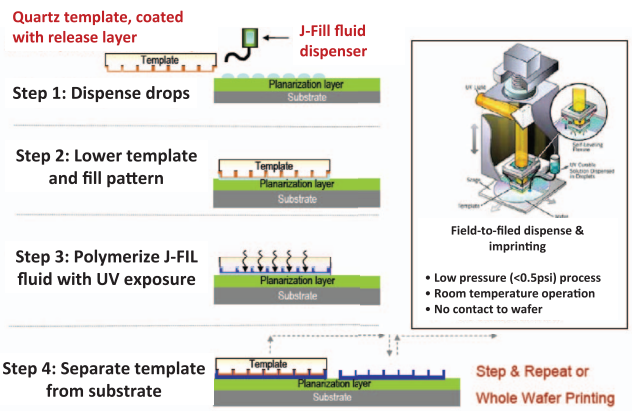
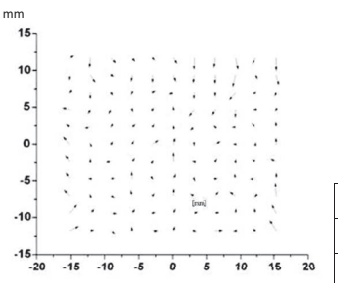
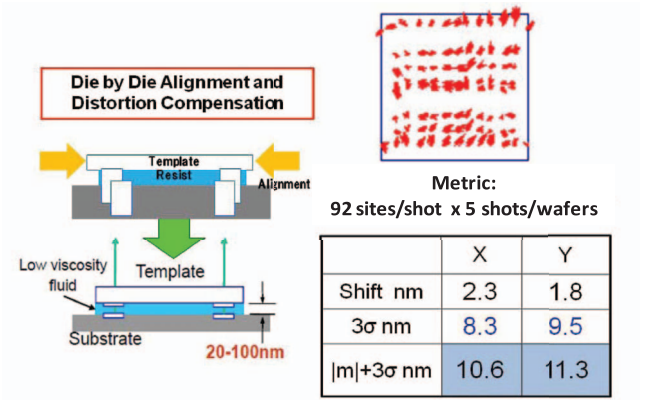


Fig. 2 Schematic of the J-FIL type process.



nm	X	Y
3s	2.9	4.2
Min	-2.0	-3.0
Max	2.0	4.4

Fig. 4 Image placement of a NIL template with a 30 mm × 26 mm field. An 11 × 11 array of image placement marks was used to calculate the placement errors.



	X	Y
Shift nm	2.3	1.8
3σ nm	8.3	9.5
|m|+3σ nm	10.6	11.3

Fig. 5 NIL overlay accuracy results. 10 nm overlay is obtained through improved tool performance and improved image placement on the imprint template.

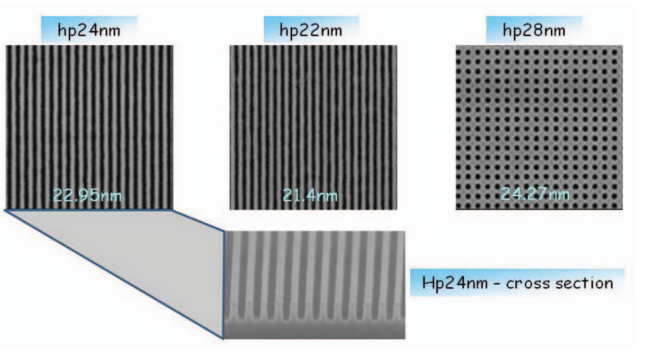


Fig. 6 Template resolution performance for NIL. Good fidelity is obtained down to 22 nm using variable shape beam writers.

necessary for the patterning processes, for metrology (such as CD measurement, image placement and defect inspection), and for defect repair.

Ultrahigh resolution patterns can be written with Gaussian beam direct write electron beam tools, and resolution as small as 14 nm has been demonstrated.[11] However, Gaussian beam systems cannot provide sufficient throughput (in general write times of less than 24 h are considered reasonable) and are therefore typically used only to write sparse patterns and provide information regarding the imprinting process. To achieve practical write times, variable shape beam (VSB) mask writers need to be employed. Although a 1× template requires the writing of features sized 4× smaller than a typical 4× photomask, it should be noted that the writing area of a template is reduced by a factor of 16 relative to a 4× mask. In addition, there is no need for optical proximity correction (OPC). Therefore the number of shapes that need to written is reduced for 1× writing. As a result, despite the fact that insensitive nonchemically amplified resists (such as ZEP-520A) must be employed to achieve the necessary resolution, the write time of a 1× template compares favorably with the write time of a 4× optical photomask. Yoshitake et al. simulated write times for two 32 nm patterns. In one case, where limited OPC was required, the template write time was reduced by 20% relative to the 4× photomask write time. In the second case, the 4× photomask required extensive OPC and the template had a 3× write time improvement over the 4× photomask. Interested readers are referred to Ref. 15 for more details.

Using commercially available VSB mask writers with accelerating voltages of 50 keV, line space patterns as small as 22 nm are possible. Both line/space resolution and contact resolution from a 50 keV VSB writer are shown in Fig. 6. The resolution limit for these systems is primarily a factor of the beam blur from the aperture, and it is expected that future generations of mask writers should be able to resolve sub-20 nm half pitch patterns. CDU from VSB mask writers is also excellent (Fig. 7). CDU for 32 nm half pitch lines across a 26 mm × 32 mm field was found to be 1.2 nm 3σ, comparable to the final CD on a printed wafer, again indicating that there is minimal contribution to overall CDU budget resulting from the imprint process.

A second consideration to the fidelity of the template is template lifetime. Recent estimates place the lifetime of a template at ~50,000 imprints. As a result, an inexpensive replica or working templates will be necessary to address cost of ownership considerations for long runner devices such as NAND Flash. Replication using imprint lithography has already been demonstrated for patterned media[16] and is now being developed for semiconductors. MII has recently introduced the Perfecta™ MR5000 mask replication tool developed specifically to pattern replica masks from an e-beam written master. Along with the tool, a new process has been developed to fabricate replicas with high contrast alignment marks so that designs for imprint can fit within current device layouts and maximize the usable printed area on the wafer. More details on template replication can be found in Ref. 17.

2.3 *Experimental Device Results with NIL*

NIL has been effectively used for prototyping to understand the performance of advanced devices. Figure 8 shows an example of the gate characteristics of a memory device using the J-FIL process. The gate capacitance depends on gate width. NIL patterning was applied by aligning three layers to create the test device. For this particular device structure, a degradation in capacitance was observed for features at or below 28 nm.

To understand the status of defectivity for the imprint process, an electrical open circuit was designed and tested and compared to EUVL. The test device was arranged with various electrical circuits that include several different half pitches, and several lengths of circuit patterns. The electric current does not flow into a circuit when a part of the circuit is disconnected. Figure 9 shows the open circuit yield results for a simple metal layer for both imprint and EUVL. CDs range from 50 nm down to 24 nm. For NIL, good yield is still obtained at 24 nm. In the case of EUVL, the yield is zero until the CD is increased to 28 nm. The EUVL yield is limited by resist resolution and linewidth roughness as well as some defectivity from the mask and resist. For imprint lithography, the electrical yield depends on the limit of pattern resolution on the template. This limitation is primarily driven by the electron beam writer and to a much lesser extent, the electron beam resist. Results of these electric yields were obtained from circuits with short wires of approximately

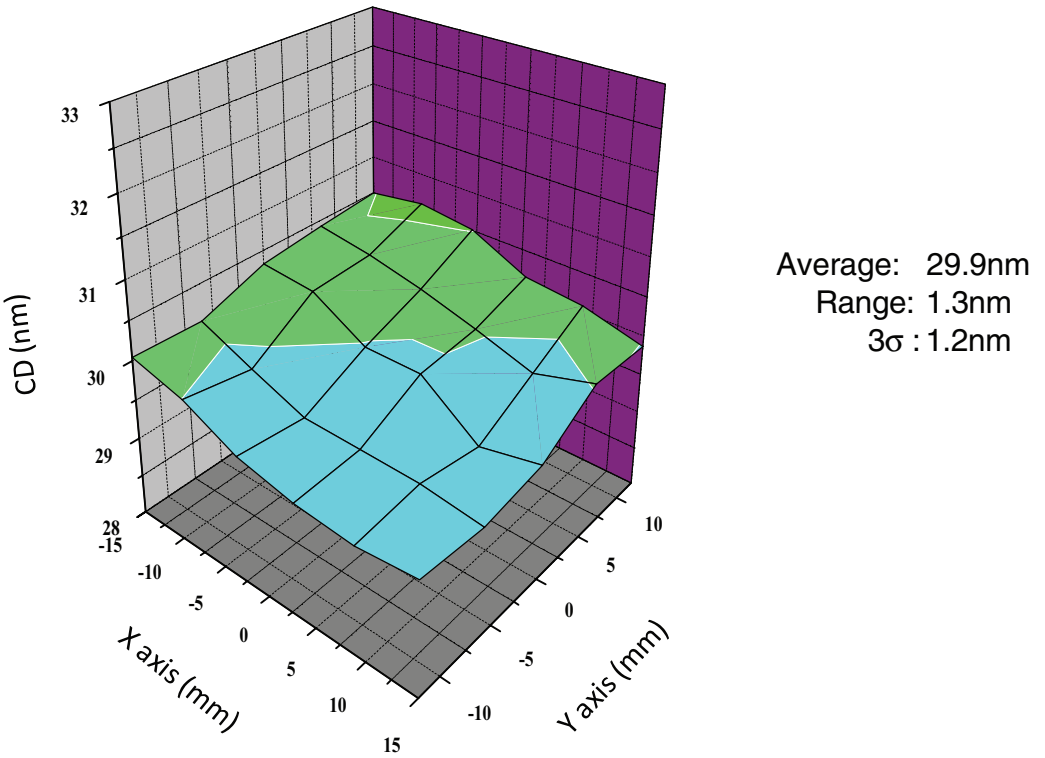


Fig. 7 Critical dimension uniformity across a 32 mm × 26 mm field.

1 mm. Evidence of yield on a circuit with longer wire length is the next key challenge.

3 Vision Toward Mass Production for NIL

3.1 *Classification of NIL Defects*

Unwelcome defects can be generated from both the template and imprint process. In order to reduce these defects, improvements will need to be made to the template, to the imprint process, and to the resist performance. Reduction of template defectivity is driven by 1× inspection capability. What is required is high throughput electron beam inspection of the full template field, preferably employing a die-to-database approach. Current e-beam inspection tools have the resolution but require a 10× improvement in throughput.[18]

Imprint defects tend to fall into two major categories: nonfill defects and plug defects. Examples of template, nonfill, and plug defects are shown in Fig. 10. In order to reduce total defectivity, it is important to establish a supporting infrastructure and continue the technical innovation which drives improvement for both the template and imprint process. In Secs. 3.2–3.4, we further explain the three different defect categories.

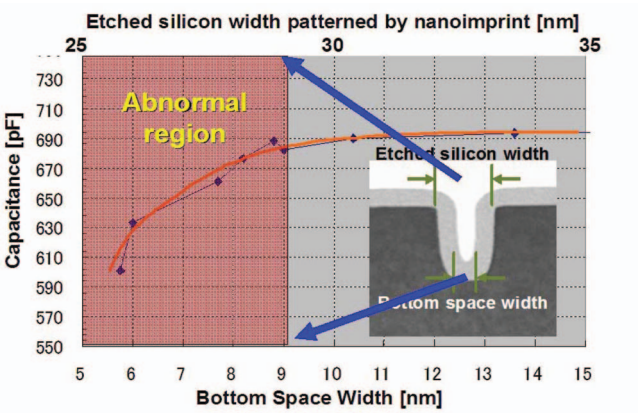


Fig. 8 NIL device application for gate performance.

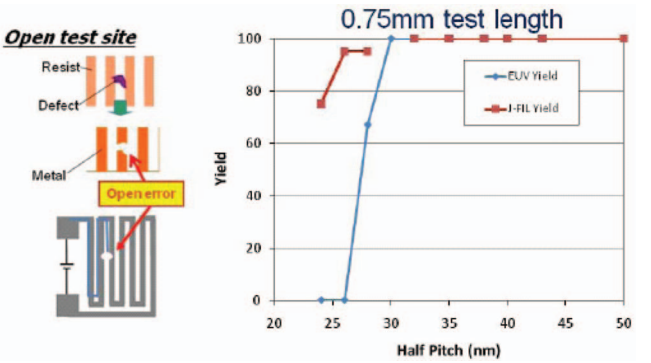


Fig. 9 NIL electrical open circuit yield test. Good yield is obtained down to 24 nm.

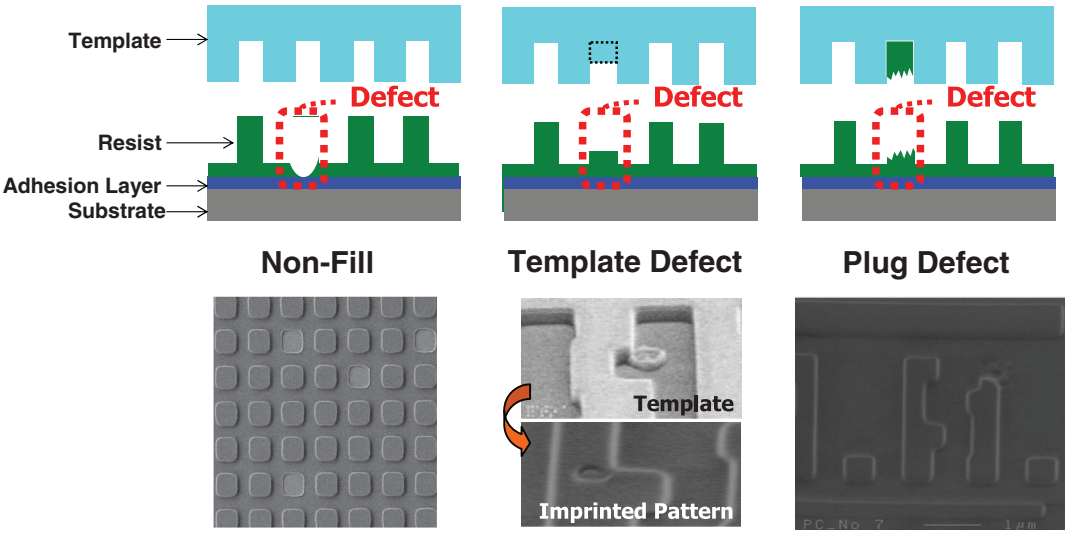


Fig. 10 Classification of NIL defectivity: The key defects are nonfill, template, and plug. A nonfill defect occurs when the liquid resist does not fill a template relief image. A template defect is an imperfection in the patterned template. A plug defect occurs when a particle embeds itself in a template relief image.

3.2 *Nonfill Defectivity*

A nonfill defect is generated when the liquid resist does not replace the ambient gas in a relief image on the template. The residual gas bubble defines an area where the resist does not fill the template and is therefore referred to as nonfill defectivity. Nonfill defectivity is a function of resist fill time. The key is to be able to meet a nonfill defectivity specification that also satisfies wafer throughput. Singh et al. have recently demonstrated defect densities of approximately 1 defect/cm^2 with a fill time of only 1.5 s.[19] Data depicting this result is shown in Fig. 11. Nonfill defectivity is influenced by material optimization, resist drop size, template pattern layout, drop pattern layout, and by controlling the resist fluid front as the resist spreads across the imprint field. Further reductions in drop size, along with tailoring of both the pattern layout and the drop pattern, will drive fill time to 1 s at defect densities less than 1.0 defect/cm^2.

3.3 *Plug Defectivity*

A plug defect is generated when, during separation of the template and wafer, the imprint resist adheres to the template rather than the adhesion layer. New imprint resist materials with higher mechanical strength are now available and have been used to reduce the plug defectivity density to less than 10 defects/cm^2.[2] In order to reduce defectivity to less than 0.1 defect/cm^2, it is important to understand imprint tribology by studying the lubricous performance of the resist on the surface of a template.

To better understand the tribology, we developed a NIL desktop lithography system called "PETAN#1."[20] A photograph of the system is shown in Fig. 12. PETAN#1 consists of a wafer chuck, a template stage, a manual UV light, and a weight gauge which is used when the template is separated from a wafer. Imprint resist material is dispensed on a wafer, and the template is brought into contact with the wafer. After the spreading of the resist, UV light is illuminated on the wafer through the template. The adhesion force is then measured by the weight gauge when the template is separated from the wafer.

PETAN#1 was fabricated as a NIL prototype tool for desktop lithography. PETAN#1 is designed with the dimensions of 300 mm × 300 mm × 250 mm, and has a weight of 12 kg. The tool accepts a template with dimensions of 70 mm × 70 mm. PETAN#1 provides an ability to study the behavior of simple critical patterns at a low cost.

In order to reduce plug defects, adhesive stress has to be made small. Adhesive stress is correlated to the frictional force between resist and template surface. To better

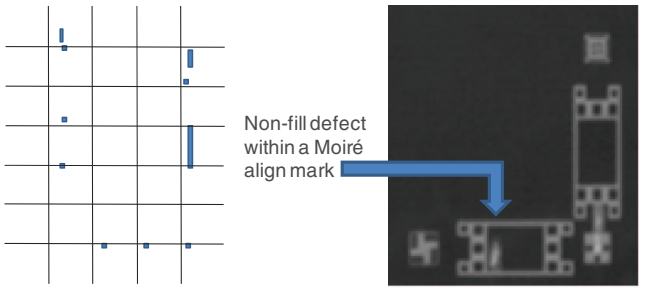


Fig. 11 (a) Field defect map showing the locations of nonfill defects using a fill time of 1.5 s. (b) An example of a nonfill defect within a printed Moiré align mark (Ref. 19).

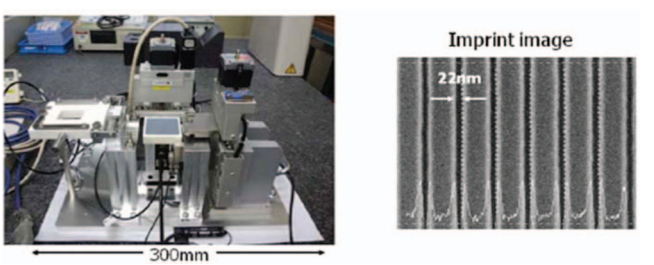


Fig. 12 PETAN#1 desktop imprint lithography tool.

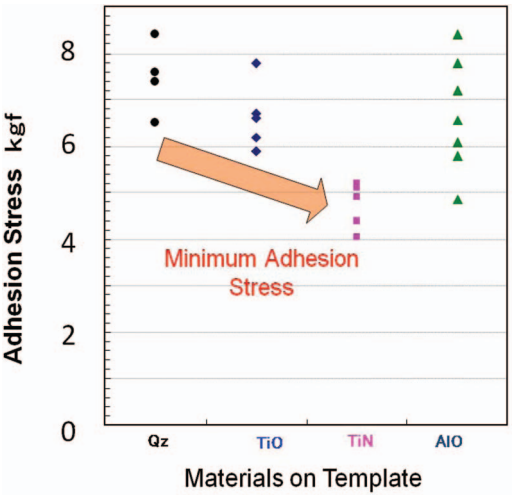


Fig. 13 Adhesive stress on quartz and CVD applied materials. The lowest adhesive stress was achieved with a TiN overcoat.

understand the effect, several materials were deposited on the surface of the template with chemical vapor deposition (CVD) to identify which provided the minimum frictional force. The materials studied included untreated fused silica, TiO, TiN, and AlO. The adhesion force at separation was measured by PETAN#1 for these coated templates. Figure 13 shows the experimental result of measured adhesion force as a function of material. It is clear that adhesion force can be influenced by the surface properties of the template. In this example, TiN on template surface had the smallest adhesion stress. In a future study we plan to investigate plug defects using a TiN coated template. It should be noted, however, that a reduction in plug defects is not a sufficient criteria to warrant a change in the construction of the template. Quite often, a reduction in adhesive stress (as a result of a lowered surface energy) is accompanied by slower resist fill and therefore increased nonfill defectivity. It is always important to characterize total defectivity and understand the trade-offs when changing the template surface.

3.4 *Template Defectivity*

Through improvements in both the mask blank and in the coating and developing of the electron beam resist, defectivity of a template has been substantially reduced. Mask blank defectivity as low as 0.04/cm^2 has recently been reported and the patterned defectivity (without the aid of template repair) has been reduced to approximately 10 defects/cm^2.[19] Defectivity on the template was measured using an NFT6000 optical inspection tool, with a sensitivity suitable down to the 20 nm node. For future nodes, optical inspection of the master mask will not be sufficient, and electron beam inspection will need to become the mainstream technology. The ultimate goal is to reach a defectivity of 0.10 defects/cm^2. It is important to note that the defectivity target cannot be achieved without the completion of an infrastructure that includes an electron beam writer, resist development, high resolution defect inspection, repair, and cleaning technology.

Current Status of NIL

Attribute	Target	Status
Template		
Master CDU	2.4nm	1.2nm
Image Placement	3nm	4nm
Master Defectivity	0.1/cm^2	10/cm^2
Replica Defectivity	1/cm^2	TBD
Imprint		
LER	2nm	2nm
Fill time	1 sec	2 sec
Overlay Accuracy	8nm	10nm
Defectivity	0.1/cm^2	10/cm^2

Fig. 14 Current status of jet and flash imprint lithography.

3.5 *Current Performances of NIL for Semiconductor Device*

Figure 14 describes the current lithographic performance of jet and flash imprint lithography. NIL has strengths in high resolution, CD control, and low line edge roughness (LER) The risk of overlay accuracy control becomes low by implementing the newest generation of electron beam pattern generators that provide excellent image placement performance. Throughput of the imprint systems continues to improve, further reducing the risk and lowering cost of ownership.[19] In this work we have demonstrated a reduction in defectivity for both the template and the imprint process. Further reductions will be required for advanced semiconductor manufacturing.

4 Conclusion

The defectivity of NIL has been analyzed and evaluated using both optical inspection and electrical yield testing. Electrical testing shows promising results at half pitches as small as 24 nm. The results are encouraging, and useful for early stage development work, but not yet sufficient for advanced semiconductor fabrication. Optical inspection, combined with SEM analysis, indicates that there are three primary defect categories; template defect, nonfill defect, and plug defect. Nonfill defectivity was improved through the use of new resist materials and improved imprint tool performance. Both the template defectivity and the plug defectivity are estimated to be about 10 defects/cm^2. In order to introduce the technology into a semiconductor factory, both defect levels will need to be reduced to 0.1 defects/cm^2. Improvements to the infrastructure, including the imprint tool, resist, template, and inspection, will help to drive down defectivity.

Finally, it should be noted that nanoimprint lithography is likely to impact markets other than semiconductor. New patterning technology including large area imprinting[21,22] and roll-to-roll imprint[23,24] can be applied to devices such as solar cells, light emission diodes, and patterned media for hard disk drives. Any new technology requires an extensive infrastructure, and the expertise and cooperation of the entire industry will be necessary to realize the next generation patterning revolution.

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Biographies and photographs of the authors are not available.