

Development of Template and Mask Replication Using Jet and Flash Imprint Lithography

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Abstract

The Jet and Flash Imprint Lithography (J-FIL™)¹⁻⁷ process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch pattern transfer. The technology is actively being used to develop solutions for memory markets including Flash memory and patterned media for hard disk drives. It is anticipated that the lifetime of a single template (for patterned media) or mask (for semiconductor) will be on the order of $10^4 - 10^5$ imprints. This suggests that tens of thousands of templates/masks will be required. It is not feasible to employ electron-beam patterning directly to deliver these volumes. Instead, a “master” template – created by directly patterning with an electron-beam tool – will be replicated many times with an imprint lithography tool to produce the required supply of “working” templates/masks. In this paper, we review the development of the pattern transfer process for both template and mask replicas.

Pattern transfer of resolutions down to 25nm has been demonstrated for bit patterned media replication. In addition, final resolution on a semiconductor mask of 28nm has been confirmed. The early results on both etch depth and CD uniformity are promising, but more extensive work is required to characterize the pattern transfer process.

Keywords: jet and flash imprint lithography, J-FIL, patterned media, semiconductor, template, mask, replication

1. Introduction

The Jet and Flash Imprint Lithography (J-FIL™)¹⁻⁷ process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch transfer. The technology is actively being used to develop solutions for memory markets including Flash memory and patterned media for hard disk drives. It is anticipated that the lifetime of a single template (for patterned media) or mask (for semiconductor) will be on the order of $10^4 - 10^5$ imprints. This suggests that tens of thousands of templates/masks will be required. It is not feasible to employ electron-beam patterning directly to deliver these volumes. Instead, a “master” template – created by directly patterning with an electron-beam tool – will be replicated many times with an imprint lithography tool to produce the required supply of “working” template/mask replicas.

Several issues need to be addressed when developing a replication process. In the case of the patterned media (PM), there are three main patterns that are of interest: 1) discrete track media (DTM) consisting of concentric lines, 2) bit patterned media BPM, consisting of pillars and 3) servo patterns. Examples of each of these feature types is shown in Figure 1. A replication process for PM must be capable of faithfully replicating all of these feature types, albeit with relatively relaxed pattern placement and defectivity requirements compared with mainstream lithography..

For the case of the semiconductor market, a variety of feature types must be resolved, although for most memory applications, the dominant feature set consists of 1:1 line/space patterns for critical front-end layers, particularly Flash. In the case of Flash memory, the most aggressive production designs are now pushing below half pitches of 25nm. For such designs, mask image placement must be well below 10nm and defectivity of the mask is required to be less than 1 defect/cm².

The first step in developing either a template or replication process is the imprinting of the Master. Previous work has demonstrated that the imprint process faithfully copies the relief image in the Master.⁸ Thus, the initial burden of critical dimension control and line width roughness falls back to the Master. In order to complete the replication process, a three step pattern transfer process is required. The first step involves the removal of the imprint residual

layer. Residual layer thickness is typically on the order of 10-15nm, with a range of approximately 5nm. The final two steps are identical to the process established for etching a Master. The chromium hard mask is first patterned using chlorine and oxygen gases, with the imprint resist as the etch mask. This etch is followed by transferring the features into the fused silica using fluorine-based chemistry. In this paper, we review the development of these pattern transfer processes for both templates and masks.

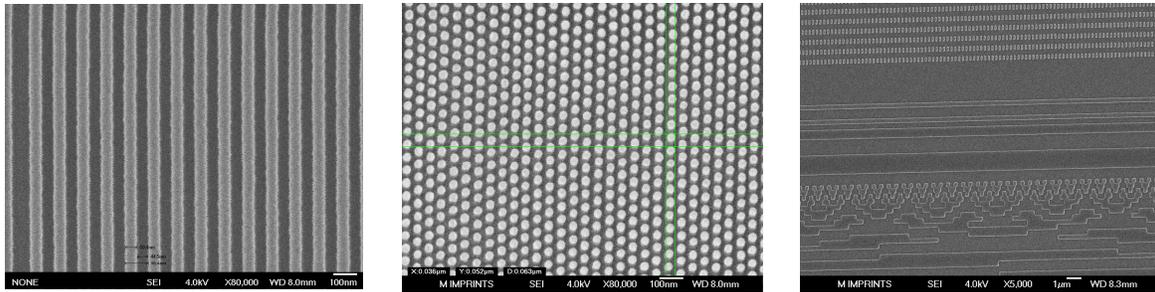


Figure 1.

2. Template Replication

a. Substrate Preparation

The form factor for both the master and replica template for PM applications is a fused silica wafer with a diameter of 150mm. After cleaning, the replica substrate is coated with a thin film (typically less than 15nm) of chromium. Prior to imprinting, an adhesion layer is applied. Good adhesion between the adhesion layer and the imprint resist is critical for maintaining low defectivity during the imprint process. Properties of this VALMat layer have been discussed in detail in previous publications.^{9, 10} Briefly, VALMat was specifically designed to have low molecular weight and high vapor pressure at room temperature. As a result, the material can be applied to a disk surface by using vapor deposition. This is a preferred method for coating, since vapor deposition processes can achieve excellent uniformity across template. The vapor deposition system was provided by Intevac. Defectivity of these films is quite low, and the adhesion layer film growth is self-limiting so that only a monolayer is deposited.

b. Process Flow

Two possible strategies can be used to create working replicas from a master. In the first case, the master is used to directly print on a substrate that will be used to create a working template. In the second case, a sub-master is first created. A limited number of sub-masters will then be used to print the replicas. This strategy is useful, as it limits the number of times the master will be printed, thereby minimizing the opportunity for damaging this high cost part. In either case, in addition to the preparation steps discussed above, the replica must be prepatterned in order to form template align marks and a mesa area on which the pattern media will be printed. One possible process flow is shown in Figure 2.

b. Pattern and Pattern Transfer

Replication of the master was conducted using a Perfecta 1100TR system (Figure 3a). The TR1100 uses Molecular Imprint's Jet and Flash™ Imprint Lithography (J-FIL™) technology. The system platform is based on three previous generations of Imprio tools and is specifically designed to produce templates meeting the requirements for patterned media disk imprinting systems. The TR1100 system capabilities include alignment, template automation, and the ability to handle 150mm fused silica substrates. The system can produce approximately ten templates per hour, more than two orders of magnitude more productive than today's leading edge e-beam template writers.

Pattern transfer of the template was done in an RIE etcher from Trion. The system consists of three etch chambers and a load lock chamber, and is configured for reactive ion etching. A photograph of the etcher is shown in Figure 3a. As mentioned in the introduction, a three step etch process is required to form the relief images in the fused silica replica. A schematic view of the required steps, along with SEM images is shown in Figure 4. Figure 4a depicts a line/space pattern after imprint. To remove the residual layer, one of two processes has been employed. Figure 4b shows the resist lines

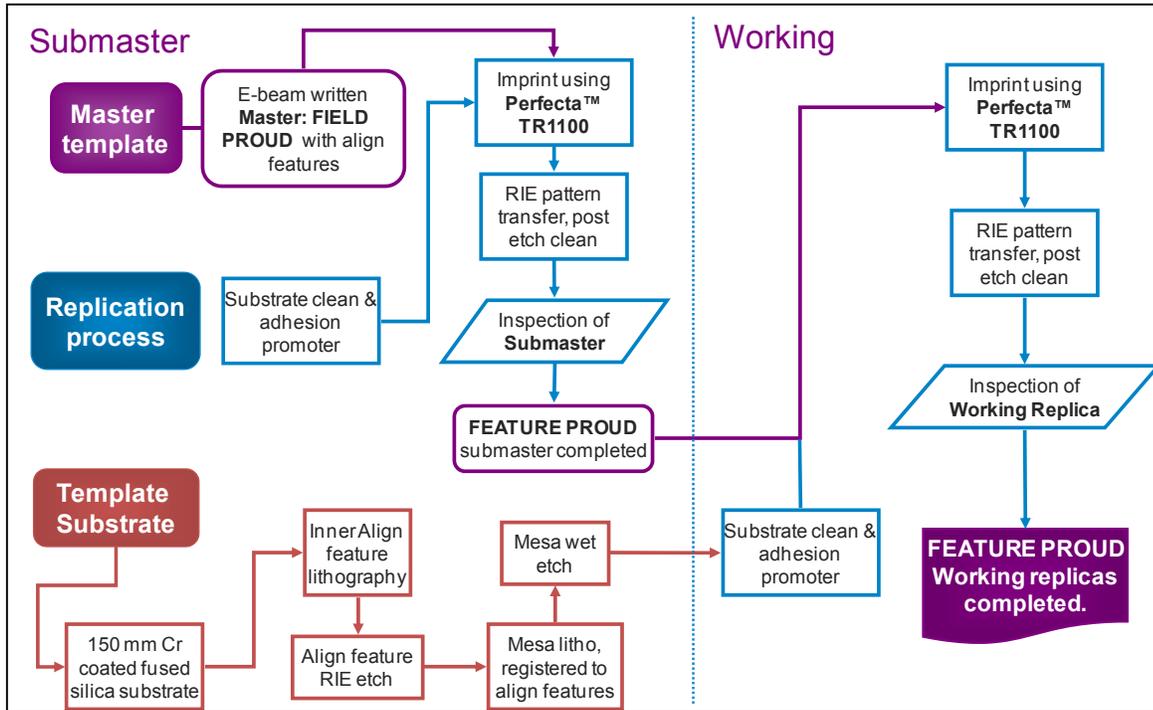


Figure 2. Process flow for creating both Submaster and working replica templates

after an anisotropic oxygen etch. It is essential to have a vertical feature in the imprint resist in order to avoid CD loss after etch. Alternatively, a fluorine chemistry can be used in order mitigate CD loss by depositing a polymer sidewall during the etch. Pictured in Figure 4c are lines after the etching of the chromium. Finally, the relief images are formed by etching in gases such as CF_4 .



Figure 3. a) Perfect TR1000 template replication tool. b) Trion three chamber RIE tool.

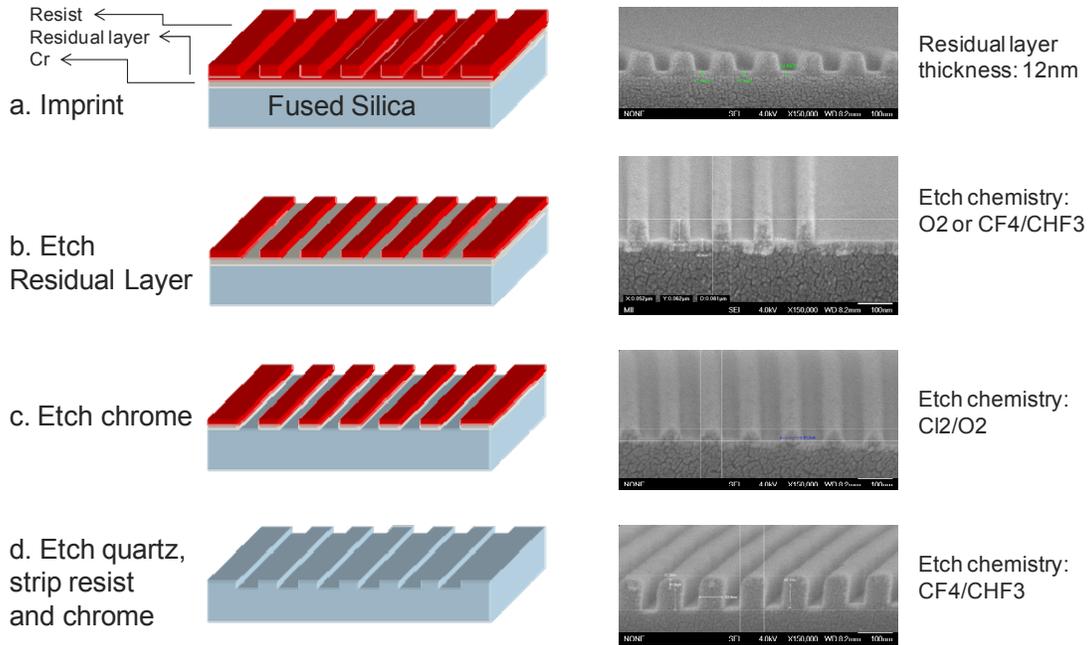


Figure 4. Key processing steps necessary for replica pattern transfer.

The pattern transfer process developed above was then applied to three different templates:

- 100nm pitch discrete track
- 70nm pitch discrete track
- 50nm bit pattern media

The results for the 100nm pitch template is shown in Figure 5. Depicted are the imprinted lines from the master, sub-master and working template. CD measurements were taken of the imprinted lines from both the master and working template. The CDs were the same to within 1nm.

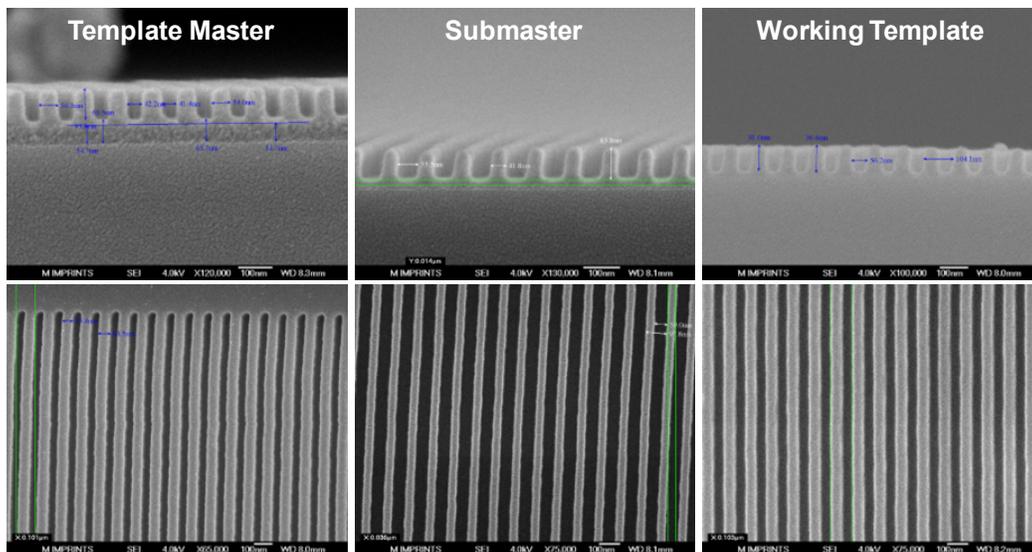


Figure 5. Imprinted lines from a master, sub-master and working template.

The etch process was next applied to the 70nm pitch tracks and the 50nm bit patterns. In these cases, a single replication was carried out to create the working template. The resulting imprints for both pattern types are shown in Figures 6a and 6b. Further work on the pattern transfer of full field replicas has also been performed. CD uniformity is generally well controlled with small excursions occurring at the inner and out diameters of the pattern. These excursions are primarily a result of proximity errors during the writing of the master.

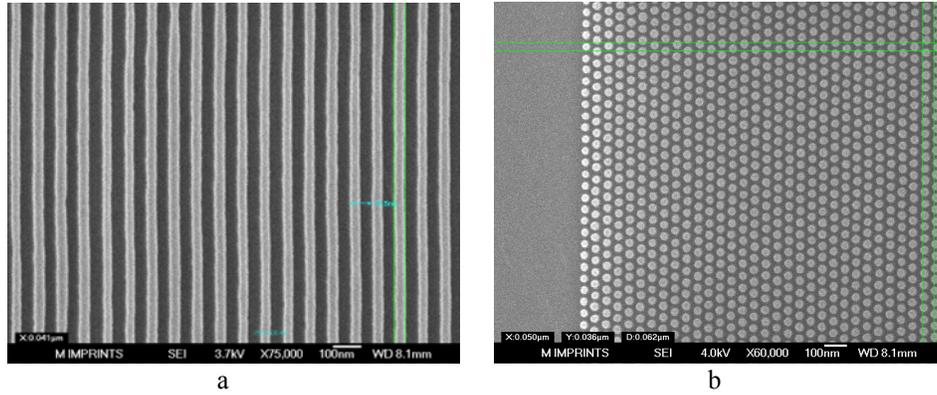


Figure 6. Imprints from replicas with pitches of 70nm (a) and 50nm (b).

3. Mask Replication

a. Mask Process Flow

A process flow similar to that presented for patterned media templates is also required for fabricating semiconductor imprint replica masks. The steps required for fabrication are outlined in Figure 7. It is anticipated that different inspection strategies will be required for these replicas, due to the defect sensitivity of the final devices. The Master will require a high resolution electron beam-based inspection, while we expect the replica mask to be inspected optically. This inspection approach has been discussed previously.¹¹

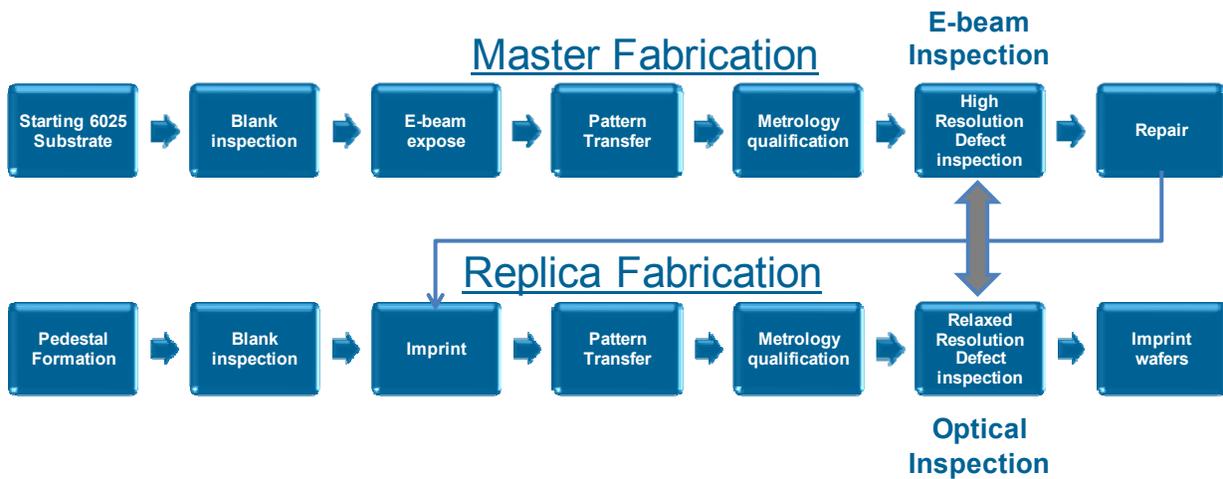


Figure 7. Schematic representation of the process steps required for semiconductor mask replication. Note that both the master and replica mask will employ a 6025 form factor.

It is important to note that a 6025 form factor is used for both the master and replica. There are two important consequences as a result of adopting this form factor. First, as an industry standard, it is possible to take advantage of the already established mask infrastructure. Second, since a final dice and polish step is no longer required, it is possible to eliminate the mask defects caused in this post-processing sequence. The replica mask, as is the case for the replica template, also has a preformed mesa. Again, the objective is to eliminate defectivity caused by any post-processing steps once the fine features are formed on the mask.

b. Mask Pattern and Pattern Transfer

A mask replication tool is now being designed and built specifically to address the requirements of the semiconductor industry. In addition to pattern imprinting, the system will also address defectivity and image placement. Subsystems are currently being integrated, and defectivity and image placement will be addressed in the future. For this work, a test stand capable of imprinting masks was used for replication. Creation of the relief images in the replica mask was achieved using the same etch tool used for template replication.

In order to study pattern transfer, a Master mask was fabricated by DNP. The field size was 26 x 32mm, and contained critical dimensions of 28, 32 and 48nm. For this work, fluorine-based chemistry was used to etch the residual layer. Pattern transfer examples of all three feature sizes are shown in Figure 8. Figure 8a shows the imprints from the master. Figure 8b shows cross-sections of the same features on the replica mask. Note the near vertical profile obtained for all three line sizes.

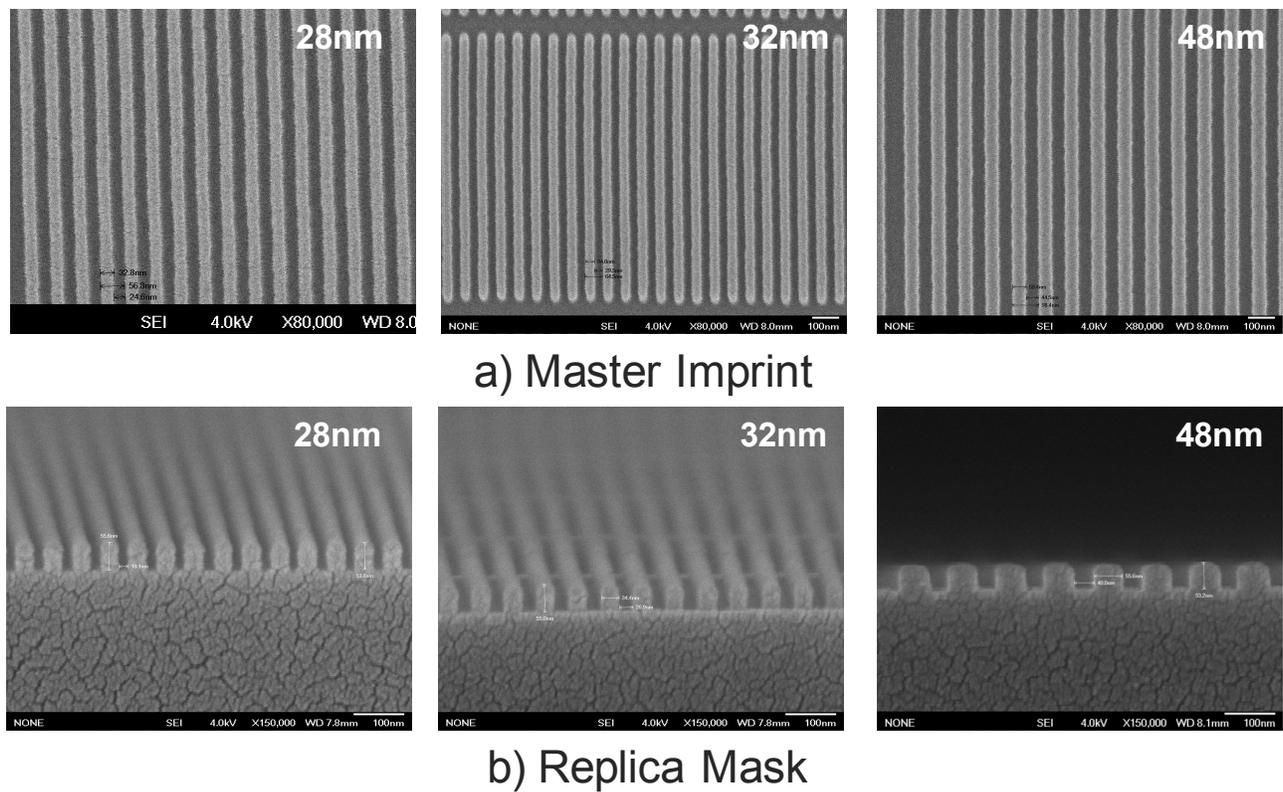


Figure 8. Pattern transfer of a semiconductor replica mask. a) Imprints of the master onto the mesa of the replica substrate. b) The same features etched into the replica mask.

A final test was conducted in order to take an initial look at etch depth uniformity and CD uniformity. Figure 9 shows a map of the 26 x 32mm field, along with the sites used for measurement. The lettered points indicate the regions where etch depth was measured. Note that one of the measurement points is located within 100 μm of the mesa edge. To determine etch depth, an AFM was used to measure the trench depth of the 48nm features. The AFM process capability excluded an accurate study of trenches less than 48nm. A resulting etch depth of 60.5 nm was achieved with a 3 sigma variation of only 2.5nm.

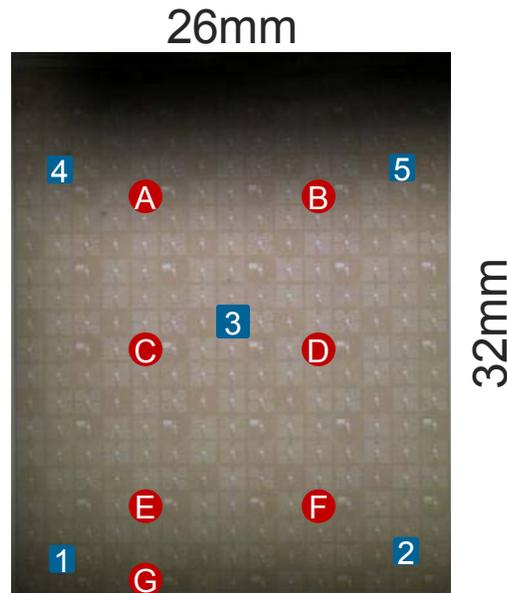


Figure 9. Mask replication field. The lettered points indicate where etch measurements were made on the replica mask. The numbered points indicate where CD measurements were made both on the master imprint and on the replica mask.

The numbered points indicate areas where CD measurements were taken both on the imprint made from the master and on the etched replica mask. The results for the 28, 32, and 48nm lines are shown in Figure 10. Note that the imprinted CDs are slightly oversized relative to target. After pattern transfer the CDs align well with the coded data. Although the data set is limited, the CD across the field appears to be well controlled. More extensive studies will be required to qualify both etch depth and CD uniformity.

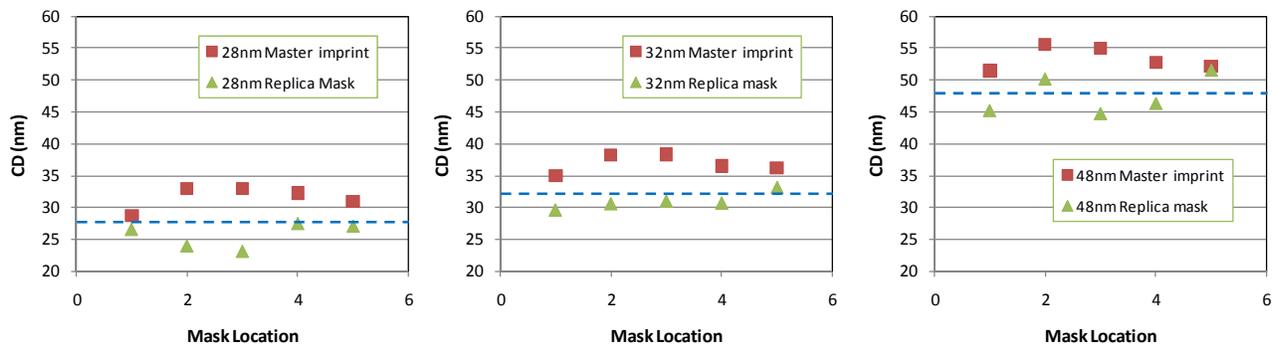


Figure 10. Critical dimension for 5 points in the field. Plotted are both the imprinted lines from the master mask and the lines etched into the replica. The dashed lines indicates intended final CD on the replica mask.

Conclusions

A first look has been taken at replication on both patterned media templates and semiconductor masks. The initial data is promising. Resolution down to 25nm has been demonstrated for bit patterned media replication. In addition, resolution on a semiconductor mask of 28nm has been confirmed. The early results on both etch depth and CD uniformity are promising but more extensive work is required to characterize the pattern transfer process. Future work will examine the critical issues of defectivity and image placement, in particular for semiconductor masks.

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