Defect inspection of imprinted 32 nm half pitch patterns

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Abstract

Step and Flash Imprint Lithography redefines nanoimprinting. This novel technique involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed leaving a patterned solid on the substrate. Compatibility with existing CMOS processes requires a mask infrastructure in which resolution, inspection and repair are all addressed. The purpose of this paper is to understand the limitations of inspection at half pitches of 32 nm and below.

A 32 nm programmed defect mask was fabricated. Patterns included in the mask consisted of an SRAM Metal 1 cell, dense lines, and dense arrays of pillars. Programmed defect sizes started at 4 nm and increased to 48 nm in increments of 4 nm. Defects in both the mask and imprinted wafers were characterized scanning electron microscopy and the measured defect areas were calculated. These defects were then inspected using a KLA-T eS35 electron beam wafer inspection system. Defect sizes as small as 12 nm were detected, and detection limits were found to be a function of defect type.

Keywords: step and flash imprint lithography, S-FIL, imprint lithography, template, imprint mask, electron beam, electron beam inspection

1. Introduction

The continued extension of optical lithography has become increasingly difficult and expensive. The use of sub-wavelength imaging has come at a significant price in terms of cost, complexity and design rule restrictions. Double patterning was employed as an extension strategy, but it came with a significant economic penalty due to its additional complexity that only worsens at 2Xnm nodes. Despite the vast number of researchers and the >$1B funding to date, Extreme Ultra Violet Lithography (EUVL) – also known as soft x-ray – has yet to solve source power, resist RLS tradeoff, optics lifetime, and mask blank contamination problems that have pushed its introduction several nodes out. Even if all of these issues are eventually addressed, EUVL, with the price of a single lithography tool rumored to be inching ever closer to US$100 million, may prove to be too expensive for adoption in a production setting.

Step and Flash Imprint Lithography redefines nanoimprinting. This novel technique involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[1] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the template is removed leaving a patterned solid on the substrate.[2]

Feature sizes below 10 nm are possible using this process, making it well-suited for CMOS applications far into the future. However, to be adopted as a mainstream CMOS fabrication process, three critical criteria must be satisfied:

1. Compatibility with existing CMOS processes,
2. Low cost-of-ownership (CoO) relative to other options, and
3. Extendibility beyond current capability needs (multi-node lifetime).

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Compatibility with existing CMOS processes requires a mask infrastructure in which resolution, inspection and repair are all addressed. The purpose of this paper is to understand the limitations of inspection at half pitches of 32 nm and below.

The mask fabrication sequence is very similar to the chromeless phase shift mask (PSM) process currently used in mask shops. Four 1X masks are fabricated on a standard fused silica quartz 6025 blank (6" x 6" x 0.25") with a <15 nm chromium layer. A standard positive tone resist is coated and exposed using either a fast shaped-beam pattern generator (common in mask shops) or a slower but higher resolution Gaussian-beam pattern generator. The patterned resist serves as an etch mask for the thin Cr film. The Cr, in turn, is used as an etch block for the fused silica.[3-5]

In both the Cr-less PSM and S-FIL template route, the second level lithography step is exposed using a fast optical writer, such as an Alta 3700 laser pattern generator. This step for Cr-less PSM is designed to expose the active area. In the case of an S-FIL template, it must protect the active area to enable formation of the 15 µm mesa or pedestal. The mesa is formed by etching the non-active areas using a wet buffered oxide etch (BOE) solution. The final step in the mask process is a dice and polish step used to separate the plate into four distinct masks.

Previous work using a KLA-T optical inspection tools to directly inspect 100nm features in a 1X mask was successful in identifying many types of defects smaller than the actual pixel size (90 nm) used the inspection.[6] Table 1 lists the defect sizes as measured at 90% capture rate using the KT-576 with a sensitivity setting of 100/100. Images of these defects are shown in Figure 1.

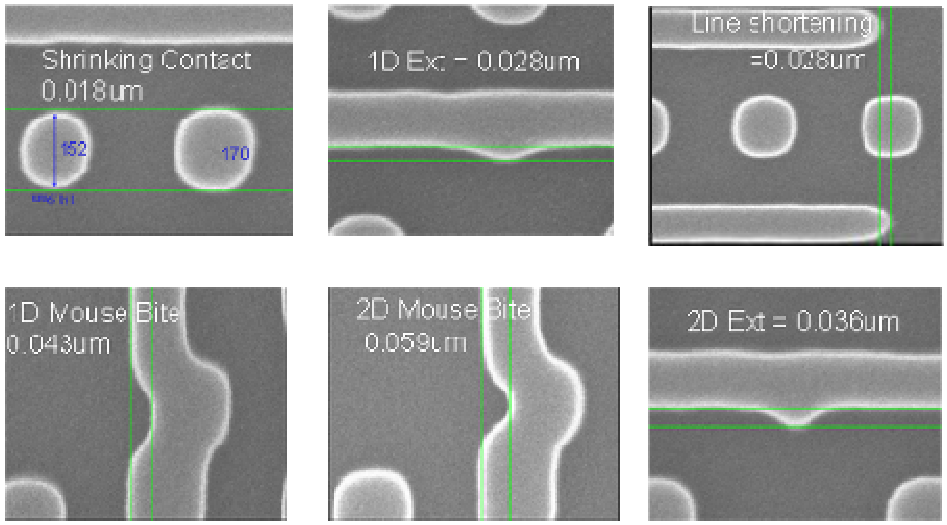

Figure 1. SEM images of the program defects. The images are of defects with sizes that are at the limit of detection for KT-576 inspection tool.

Defect Type	Reflected mode quartz (actual defect size nm)
Shrinking contact	21
1D mouse bite	69
2D mouse bite	78
1D Extension	37
Line End Shortening	39
2D extension	50

Table 1 Program defect size at a capture rate of 90% with a KT-576 mask inspection tool.

A second study examined the ability to inspect defects on a printed wafer using a KLA-T eS32 electron beam inspection system.[7] Defects were clearly observed in 32 nm half pitch patterns. An example of a captured defect is depicted in Figure 2.

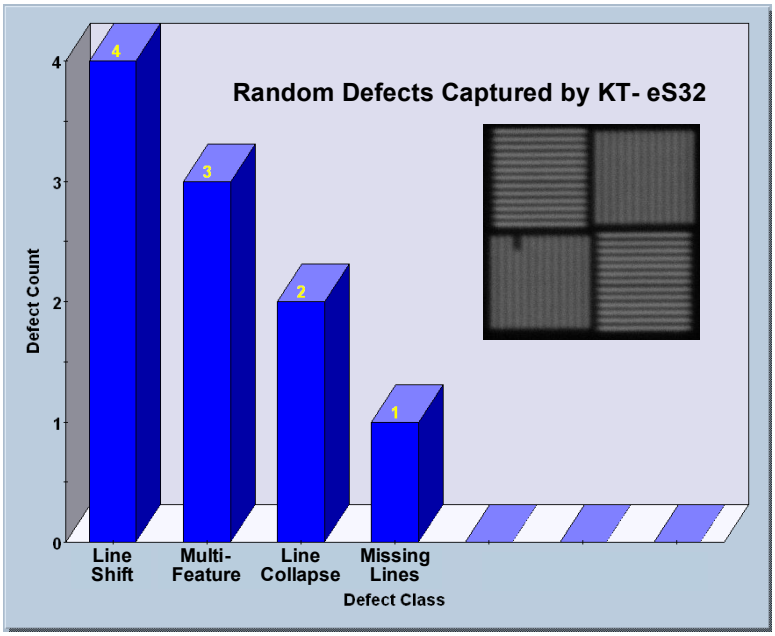

Figure 2. Pareto chart of the random defects by type. Also shown is a defect in the 32 nm half pitch pattern.

In this study, die-to-die electron beam inspections of 32 nm half pitch features were performed on imprinted wafers patterned by an Imprio 250 system. A customized pattern was developed in which programmed defects were inserted in to the 32 nm patterns. The details of this pattern are discussed in the next section.

2. Experimental Details

To generate the mask, patterns were exposed by Dai Nippon Printing using a JEOL 9300 Gaussian beam pattern generator. ZEP520A resist was chosen as the positive imaging resist. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process, followed by a dice and polish step were employed to create a finished 65 mm x 65 mm template.[8]

Three patterns were chosen to represent typical features observed in devices: lines spaces gratings, dense pillar arrays, and an SRAM Metal 1 (M1) device cell. Each of these patterns was scaled to 3 different half pitches: 48 nm, 40 nm and 32 nm. Including the feature types and half pitch sizing, a total of 9 designs as shown in Figure 3 were evaluated in this study. Each design, in turn, had an assortment of additive and subtractive programmed defect types which included horizontal and vertical orientations, or specific cell locations. Figure 4 shows two examples of these defects for the lines and spaces gratings and the SRAM M1 cell. The programmed defects were incrementally varied in 12 sizes. The 32nm designs contained programmed defects starting at 48nm with incremental shrinks by 4nm. The 40nm designs contained PD's starting at 60nm with incremental shrinks by 5nm. Lastly, the 48nm designs contained PD's starting at 72nm with incremental shrinks by 6nm. Each array of programmed defect types was repeated 3 times per field to insure repeatability. The programmed defects were interspersed within normal cells on a grid for identification purposes. Each of the 9 designs contains 144 programmed defects (4 types, 12 sizes, and 3 repeats) for a total of 1296 PDs within the field.

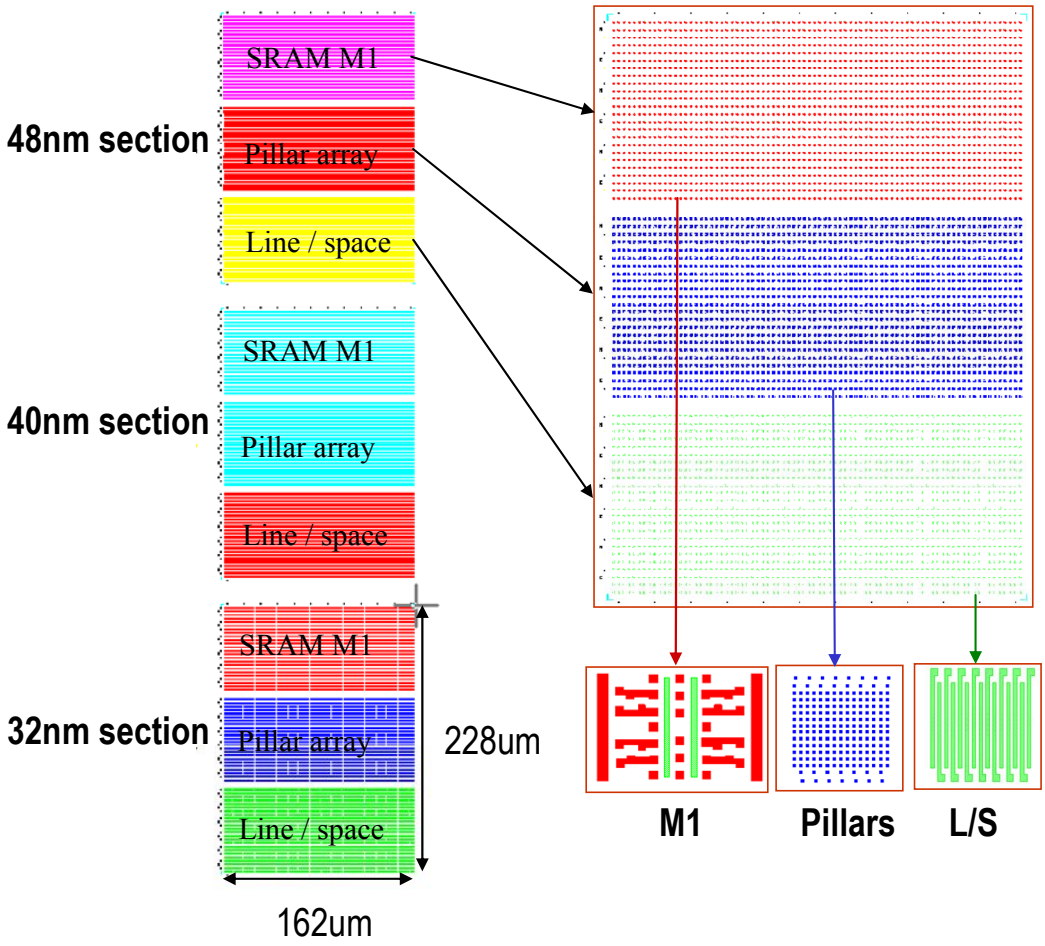

Figure 3. Programmed defect layout

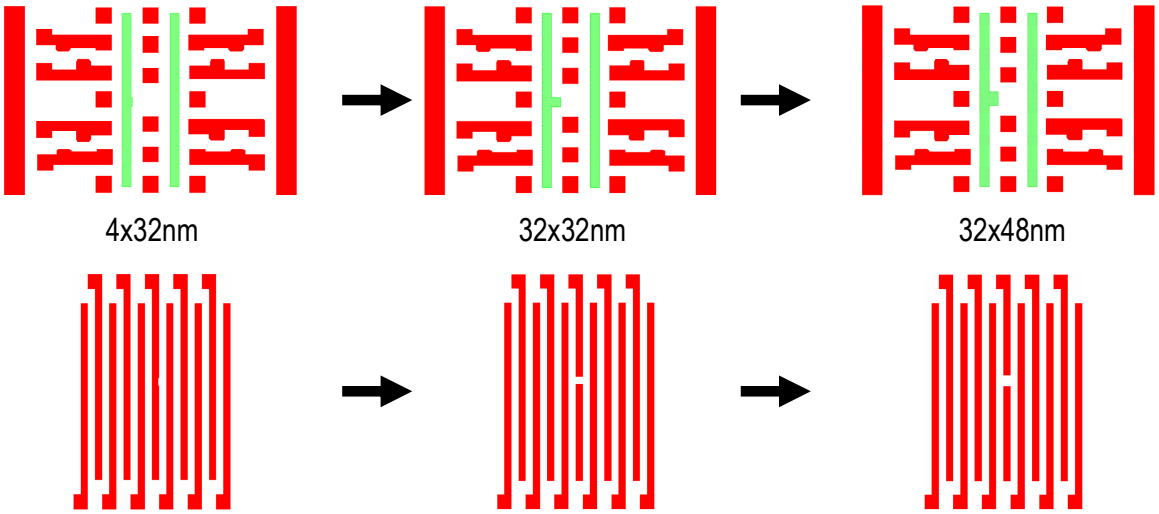

Figure 4. a) Extension defects in the SRAM Metal1 pattern. B) Mousebites in the line/space array.

Initial characterization of the imprint mask was done using a Holon EMU-270A SEM. The system is capable of 1.5 nm resolution at 1.0 kV when applying aberration correction. Low vacuum operation, combined with proprietary charge control enables high quality imaging on uncoated fused silica masks.

Imprinting of the mask pattern was performed by using a Molecular Imprints Imprio 250 imprint tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 300mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process have previously been reported.[9]

Critical dimension (CD) images of the imprinted patterns were captured with a JEOL JSM-6340F field emission cold cathode SEM equipped with a tungsten emitter. The accelerating voltage can be varied from 0.5 to 30 kV. The system has intrinsic 1.2 nm resolution capability at 15 kV accelerating voltage, and 2.5nm at 1 kV. CD measurements and line width roughness data were then extracted offline using the SIMAGIS® automated image metrology software suite from Smart Imaging Technologies.[10]

Wafer inspection was done with a KLA-Tencor eS35 electron beam inspection tool. Improved performance of the eS35 relative to previous generation of tools is based on:

- Higher beam current density, a smaller pixel and hardware advancements that allow an overall lower noise floor
- Advanced algorithms, ported from and proven on KLA-Tencor's optical inspectors
- Enhanced on-board review capability that provides high resolution images of defects of interest
- New defect binning algorithms that convert defect data to an actionable Pareto
- Innovative μLoop technology that provides accelerated detection of systematic defects

3. Results

a. Mask SEM inspection

Images of the programmed defects for all pattern types were captured with the Holon EMU-270A SEM. Examples of the 32 nm Metal 1 extension defects are shown in Figure 5. From smallest to largest, the 4 nm defect is difficult to discern, but starting at 8 nm, all of the programmed defects are visible.

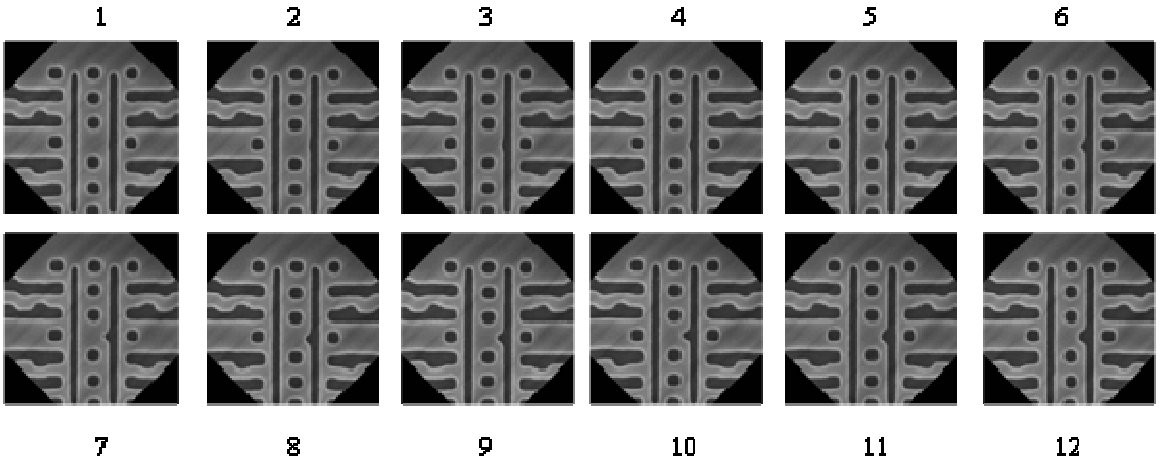

Figure 5. Programmed extension defects in the 32 nm Metal 1 pattern

A second example is shown in Figure 6. In this case, mousebite defects were included in the line/space pattern. Once again it is difficult to discern the 4 nm programmed defect. The 8nm, 12nm and 16nm programmed defects cause a pinching of the center black line along the edge. At 20 nm (Image 5, top row), the black line opens, causing a non-linear behavior in the progression of the defective area.

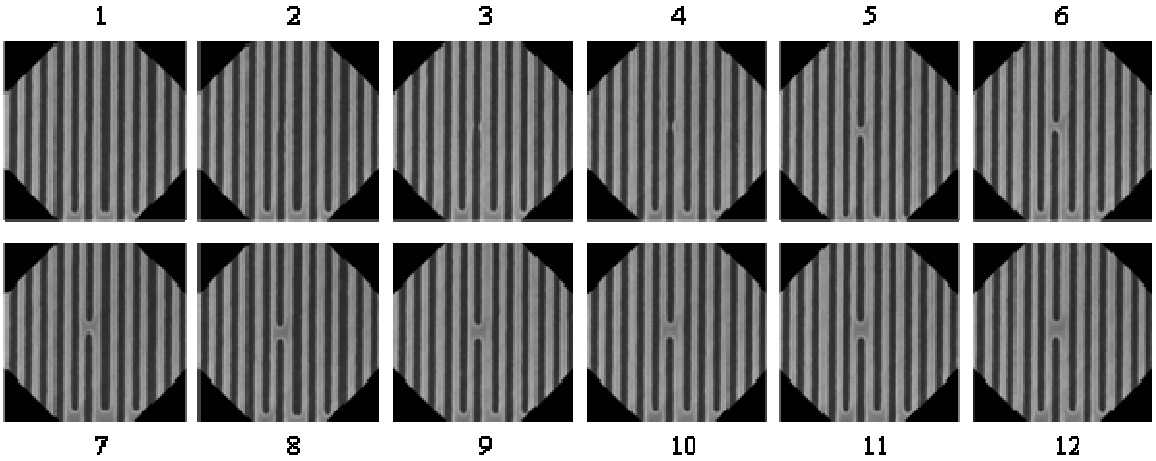

Figure 6. Mousebite defects in the line/space pattern

b. Imprint analysis

Following the imprinting on 300 mm silicon wafers, SEMs were again collected in the programmed defect areas in order to understand the correlation between the defects on the mask and the actual printed defects. Figure 7 depicts the programmed defects in the 32 nm Metal 1 patterns. Note that the location of the defect is mirrored in x relative to the mask images shown in Figure 5, because of the imprint process. Imprinted lines with the mousebite defects described earlier are shown in Figure 8. Again, note the nonlinear behavior in the actual programmed defect size.

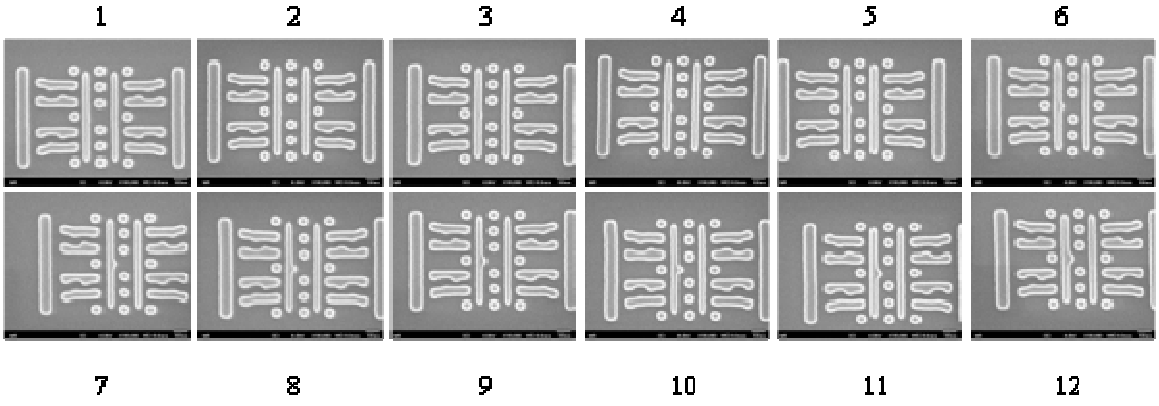

Figure 7. Programmed defects from the 32 nm Metal 1 pattern imprinted on to a 300 mm silicon wafer.

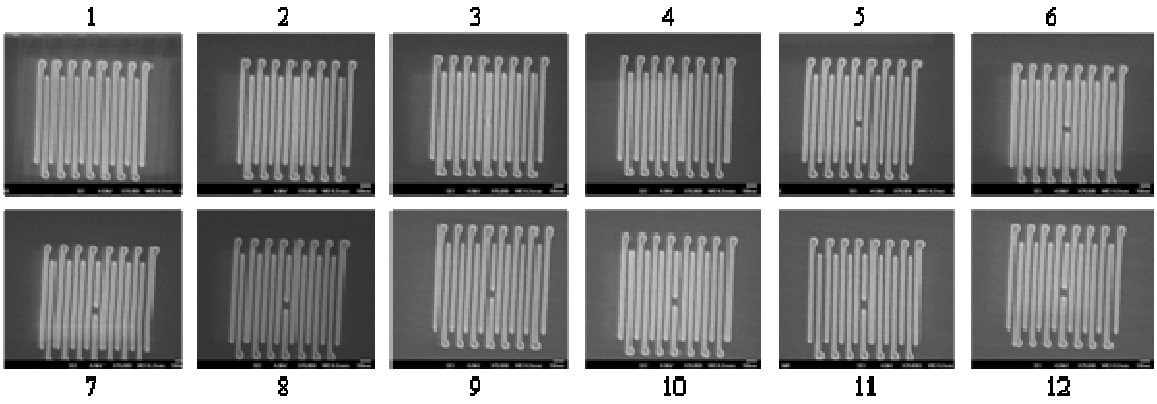

Figure 8. Programmed defects from the 32 nm line/space pattern imprinted on to a 300 mm silicon wafer.

SIMAGIS analysis software was used to calculate the actual defect area on the mask and on the imprinted wafer for each programmed defect as a function of the coded defect size. The defect area was obtained by taking the defect image, adjusting the image threshold, shifting the image by a single pitch, and then subtracting the shifted image from the original. The pixilated difference can then be converted into a defect area. An example of this technique is shown in Figure 9.

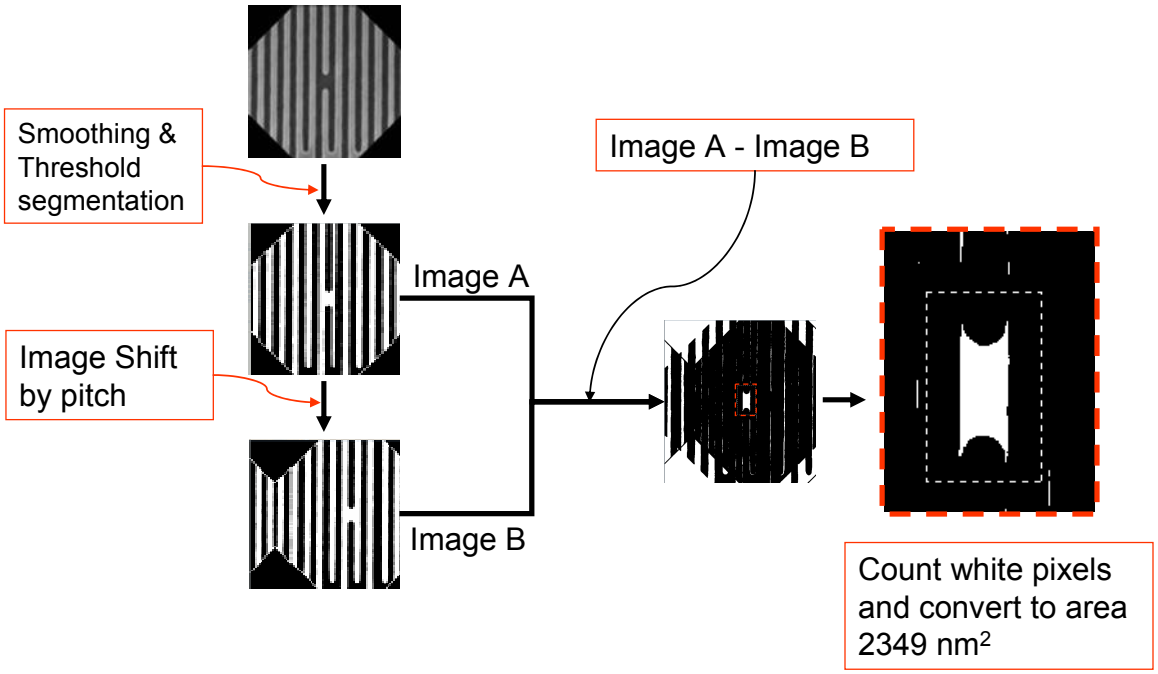

Figure 9. Determination of the actual defect area using SIMAGIS analysis software.

The defect size trend for both mask and imprint are shown in Figure 10. Pictured are the trends for the Metal 1 defects and the shrinking pillars. Both graphs show excellent agreement in defect size between the mask and imprint. As expected, the Metal 1 trend line is linear. In comparison, a discontinuity (similar to that seen in the line/space pattern) is observed in the chart of the dense pillars. As the pillar is shrunk to a diameter less than 16 nm, the feature is no longer resolved on the mask, and the defective area jumps in size. The defective area then remains constant until the programmed pillar above the central pillar is also shrunk.

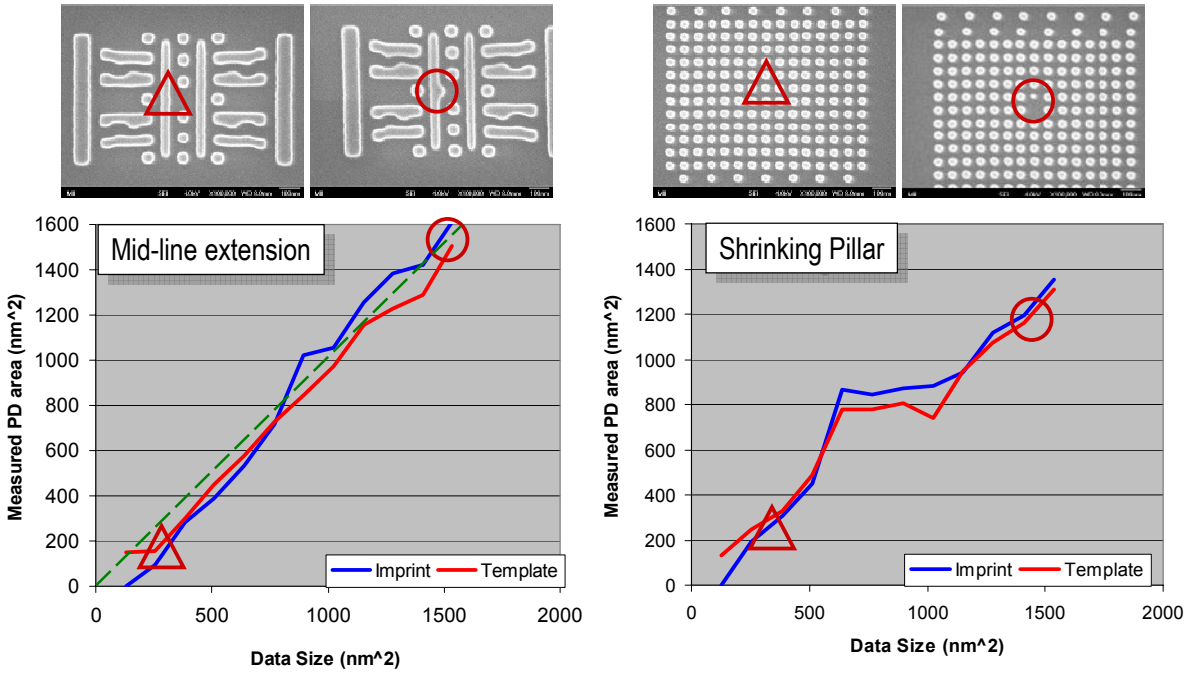

Figure 10. Measured defect size as a function of the coded defect size for both the Metal 1 pattern and the dense pillar array.

c. eS35 Inspection Results

The eS35 wafer inspection system was used to observe the patterned defects. The system operated at a data rate of 50 megapixels per second, with a pixel settings of 15, 20, and 25nm. Landing energy was set to 1750 volts and eight scans were collected.

An example of the resulting data is shown in Figure 11. Pictured is the capture rate of all of the various programmed defect types for the 32 nm patterns as a function of the coded defect size at two different pixel sizes. Two trends are clearly observed: 1) Pixel setting has a significant effect on defect detection. As the pixel size decreases from 25 nm to 15 nm, the minimum defect size observed decreases from 18 nm to 11 nm. 2) Minimum defect size is dependent on the programmed defect type. The eS35 was most sensitive to shrinking pillars and least sensitive to extensions in the Metal 1 pattern. These two particular trend lines are shown more clearly in Figure 12. Figure 12 depicts the capture rate as a function of the actual measured defect area and indicates a sensitivity in the shrinking pillar array and Metal 1 extension of 10 nm and 18 nm, respectively. These results align well with the ITRS requirements for NAND Flash at 22 nm.

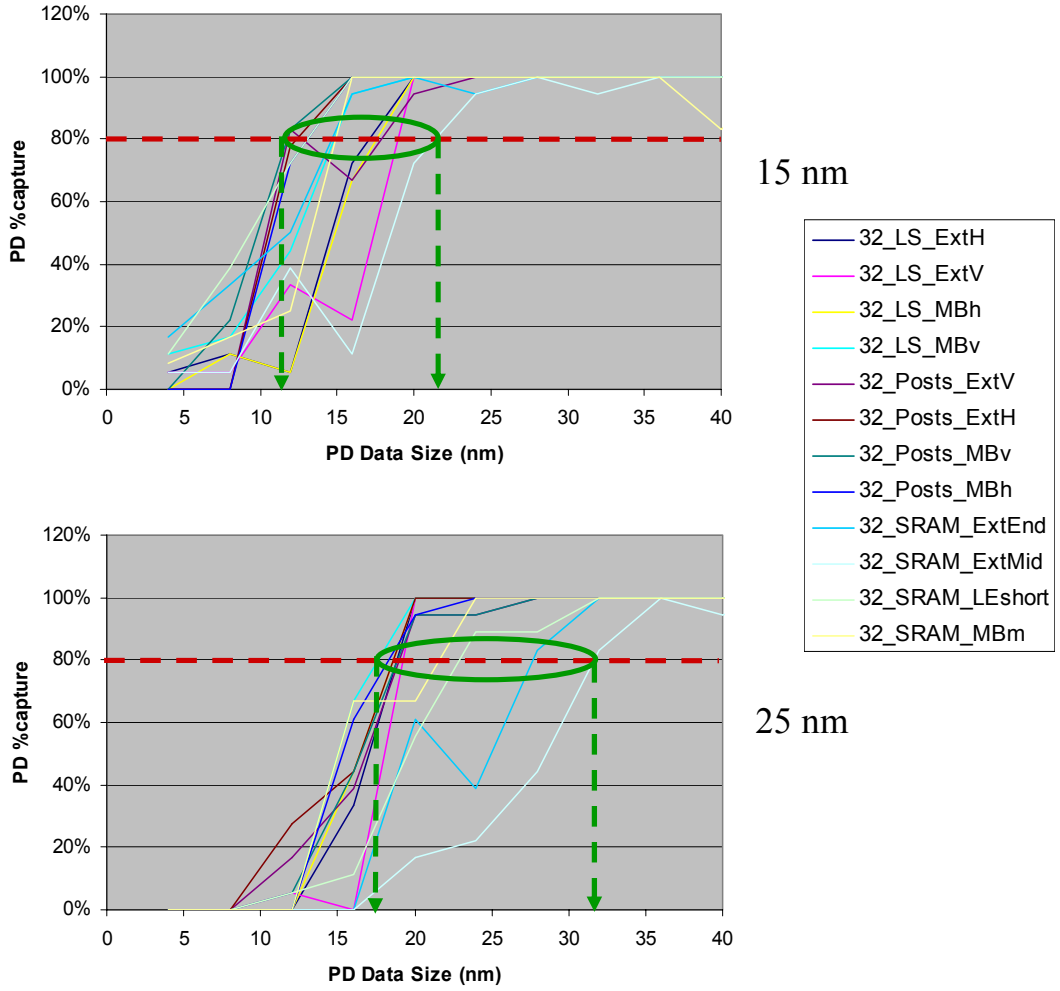

Figure 11. Imprinted 32 nm half pitch lines are resolved over an electron beam exposure dose range of nearly 20 percent.

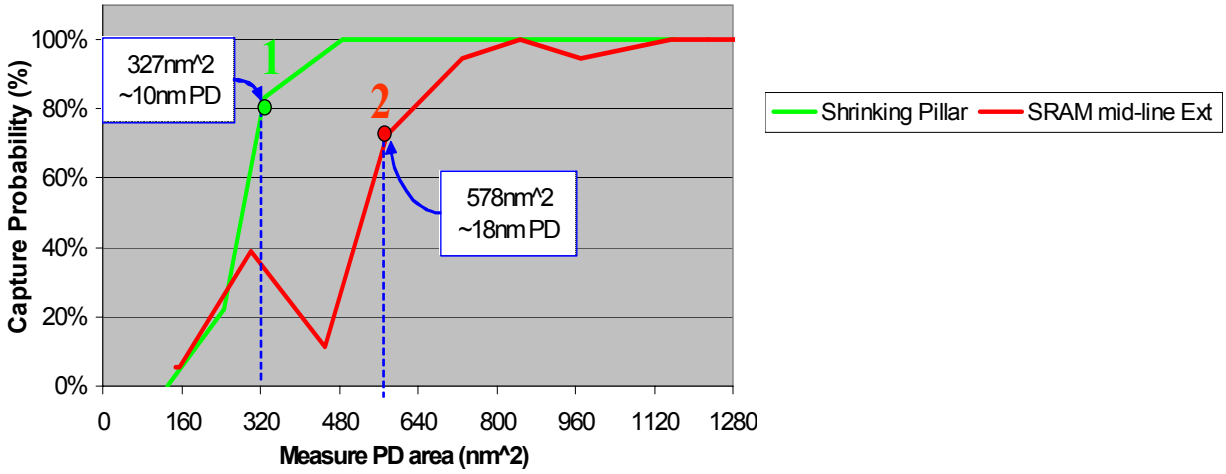

Figure 12. Capture rate as a function of the measured programmed defect area.

4. Conclusion

The ITRS roadmap calls for sensitivity to 20 nm defects on an imprint mask for 22 nm NAND Flash design rules. The es35, at a pixel setting of 15 nm demonstrated the capability to detect defects as small as 10 nm, depending on defect type. Inspection times still need to be reduced, however. As an example, for a 26 mm x 33 mm field inspection at 50 Mpps and a pixel size of 20 nm, approximately 12.5 hours would be required for the inspection. It is possible to increase data rates, but process development would be required to maintain the sensitivity levels demonstrated in this work. Finally, an eventual transition to direct inspection of the imprint mask, along with the ability to do die-to-database inspection would be beneficial. Future papers will discuss both improved sensitivity as well as die-to-database inspection.

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