High throughput Jet and Flash Imprint Lithography for advanced semiconductor memory

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Abstract

Imprint lithography has been shown to be an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography (J-FIL) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Non-fill defectivity must always be considered within the context of process throughput. Processing steps such as resist exposure time and mask/wafer separation are well understood, and typical times for the steps are on the order of 0.10 to 0.20 seconds. To achieve a total process throughput of 20 wafers per hour (wph), it is necessary to complete the fluid fill step in 1.0 seconds, making it the key limiting step in an imprint process. Recently, defect densities of less than 1.0/cm^2 have been achieved at a fill time of 1.2 seconds by reducing resist drop size and optimizing the drop pattern.

There are several parameters that can impact resist filling. Key parameters include resist drop volume (smaller is better), system controls (which address drop spreading after jetting), Design for Imprint or DFI (to accelerate drop spreading) and material engineering (to promote wetting between the resist and underlying adhesion layer). In addition, it is mandatory to maintain fast filling, even for edge field imprinting. This paper addresses the improvements made with reduced drop volume and enhanced surface wetting to demonstrate that fast filling can be achieved for both full fields and edge fields. By incorporating the changes to the process noted above, we are now attaining fill times of 1 second with non-fill defectivity of ~ 0.1 defects/cm^2.

Keywords: Jet and Flash Imprint Lithography, J-FIL, throughput, defectivity, imprint lithography

1. Introduction

Imprint lithography is an effective technique for replication of nano-scale features.[1,2] Jet and Flash Imprint Lithography (J-FIL™) involves the field-by-field deposition and exposure of a low viscosity resist deposited by Drop-On-Demand inkjet onto the substrate.[3-8] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, the mask is removed, and leaves a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there is no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

There are many other criteria besides resolution that determine whether a particular technology is ready for manufacturing. On the mask side, there are stringent criteria for imprint mask defectivity, critical dimension uniformity (CDU), image placement (IP) and imprint defectivity. The master mask blank, which consists of a thin (< 10nm) layer of chromium on the 6” x 6” x 0.25” fused silica was recently reported to have a defectivity of only 0.04/cm^2 as measured by a Lasertec tool with 50 nm sensitivity.[9] Presently, Dai Nippon Printing (DNP) has exceeded the targets for both CDU and IP. DNP has fabricated master masks containing no defects, as measured by an HMI electron beam mask inspection tool with a sensitivity of < 20 nm.[10]

With respect to the imprint stepper, both CDU and line edge roughness meet the criteria of 2nm. Toshiba has achieved overlay of 10nm (with a target of 8nm)[11] and defect levels ~ 5/cm^2 across a lot of 25 wafers (see Figure 1.).[REF 12 – defect paper from 2013]

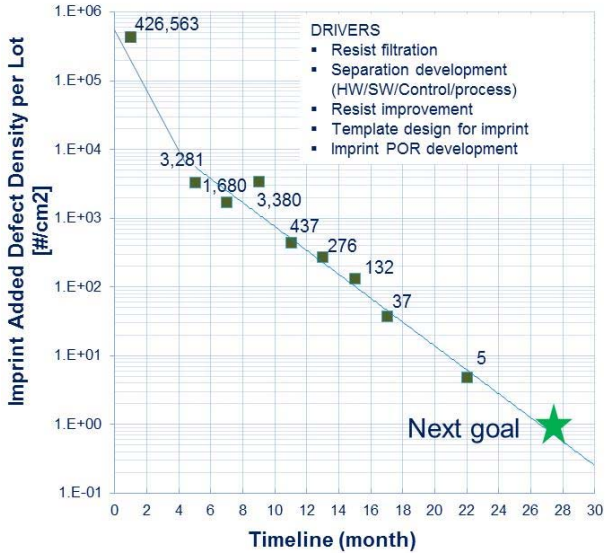

Figure 1. Defectivity reduction to the 5/cm^2 by imprint stepper.

Non-fill defectivity is always considered within the context of process throughput. Resist exposure time and mask/wafer separation are well understood processing steps with typical durations on the order of 0.10 to 0.20 seconds. To achieve a total process throughput of 20 wafers per hour (wph), it is necessary to complete the fluid fill step in 1.0 seconds, making it the key limiting step in an imprint process. A non-fill defect density of 1.2 def/cm^2 was demonstrated at fill times of 1.5 seconds. For longer fill times, the defectivity dropped to zero. More recently, defect densities of less than 1.0 def/cm^2 have been achieved at a fill time of 1.2 seconds by reducing resist drop size and optimizing the drop pattern. It is interesting to note that all of the non-fill defects occurred either at boundaries where pattern densities were significantly different or near the Moiré align marks (Figure 2). Both defects can likely be addressed with specific imprint patterns designed to enhance filling in these areas.[13]

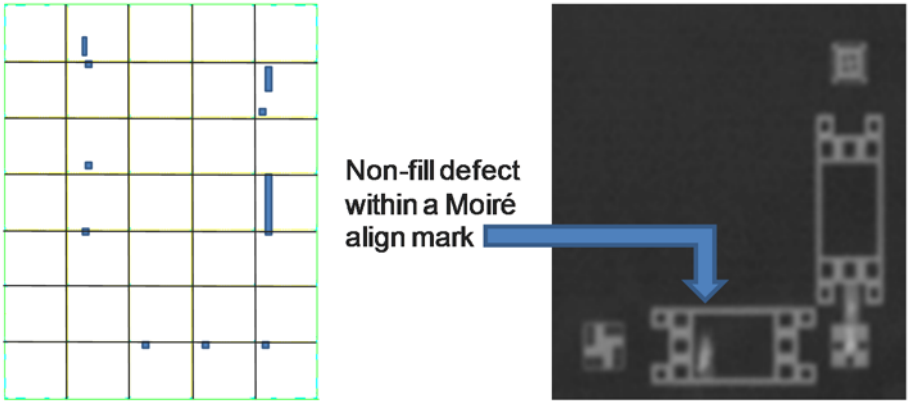

Figure 2. a) Field defect map showing the locations of non-fill defects using a fill time of 1.5 seconds. b) An example of a non-fill defect within a printed Moiré align mark.[13]

The key parameters impacting resist filling are:

- Resist drop volume (smaller is better)
- System controls (addresses drop spreading after jetting)
- Design for Imprint or DFI (accelerates drop spreading)
- Material engineering (promotes wetting between the resist and underlying adhesion layer)

In this paper, we address the improvements made in drop volume and surface engineering to reduce the duration of the filling step. An important consideration in J-FIL is to maintain fast filling for the edge fields. We demonstrate that fast filling can be addressed for both full fields and edge fields. By incorporating the changes to the process noted above, we are now achieving fill times of 1 second with non-fill defectivity of ~ 0.1 defects/cm^2.

2. Experimental Details

To generate the inspection test masks, patterns were exposed by Dai Nippon Printing using a NuFlare EBM7000 shaped beam pattern generator. ZEP520A resist was chosen as the positive imaging resist. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process were employed to create a master imprint mask for the Imprio 500 tool

The pattern chosen for evaluation of non-fill defects was a 26mm x 33mm mask consisting 28nm Flash-like device gate patterns and dummy fill die surrounding the device die. The mask also included peripheral structures such as align marks and metrology marks.

Imprinting with the replica mask was performed by using a Molecular Imprints Imprio® 500 imprint tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 300 mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process have previously been reported.[14]

Resist filling was visually observed with a large field of view camera that is capable of imaging the entire 26mm x 33mm field. Defectivity was measured on an in-house KLA-Tencor 2132 wafer inspection tool. All inspections were performed in array mode.

3. Defect Results

Resist drop volume plays a key role in resist fill time. In general, the smaller the drop volume, the smaller the drop pitch. As drop pitch decreases, so does the drop merging time. The results of using 1.5 pL drops has previously been reported. In this work, drop volume has been decreased to 0.9 pL.

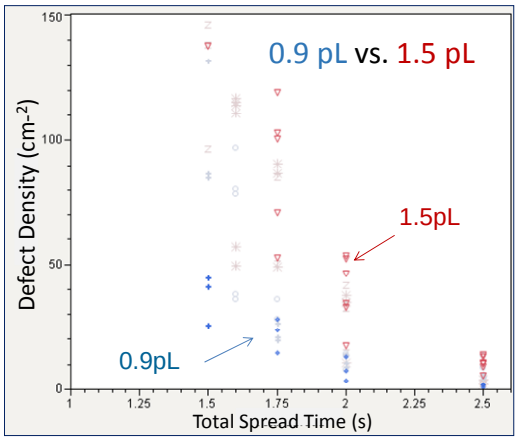

Figure 3. Defect density and spread time improvements when reducing the drop volume from 1.5pL to 0.9pL.

To understand the impact of decreasing drop volume, defect density was measured at different resist fill times for arrays of both 1.5 pL and 0.9 pL drop volumes. Fill times ranged from 1.5 to 2.5 seconds. The results are shown in Figure 3. The decrease in total spread time is apparent, and a fill time improvement of approximately 0.5 seconds was realized.

The second step taken to improve throughput was to adjust the wetting properties of the underlying adhesion layer. Adjustments to the material properties were first examined by measuring the contact angle between the resist and adhesion layer film. Unfortunately, this was not a good metric, as the contact angle for the old adhesion layer film and the modified film measured less than 5° (better than the tool measurement capability).

As a result, a second approach was adopted to quantify the wetting for the adhesion layer. The drop diameter for a 0.9 pL was measured for three different substrate cases: 1) resist deposited directly on bare silicon, 2) resist deposited on MII's original TranSpin adhesion layer material, and 3) resist deposited on a modified adhesion layer surface. After resist jetting, the drops were UV exposed approximately 500 msec. The results are reported in Figure 4 with the modified adhesion layer spreading the most of the three cases, reaching a nominal drop diameter of 215 µm.

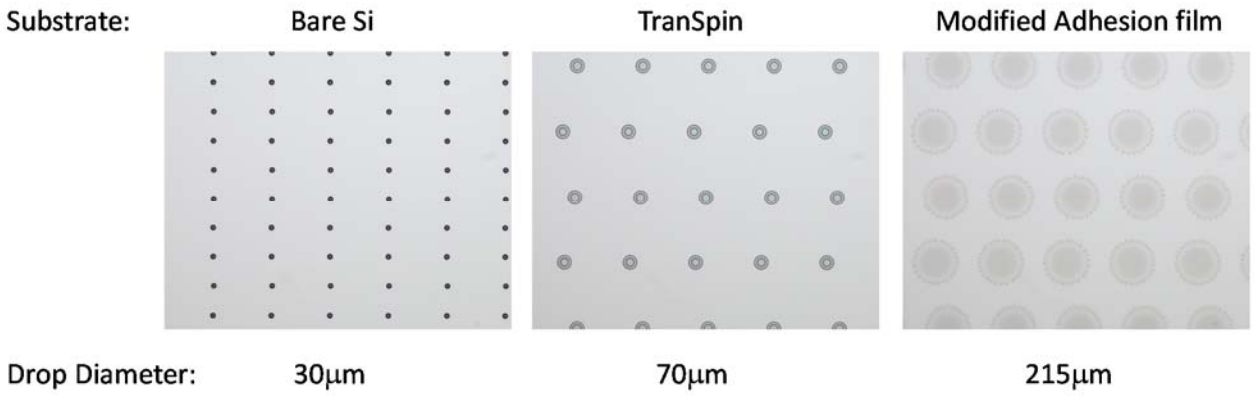

Figure 4. Drop diameter for three different surfaces. A modified adhesion layer promotes fast wetting of the resist.

The combination of the 0.9 pL drop volume and the modified adhesion layer was then used to study defect density as a function of resist spread time. The matrix experiment used to study defectivity is shown in Figure 5.

Imprint conditions:

- Tool: MII Imprio 500 stepper
- 28nm HP template with DFI
- Wafer: bare Si + modified adhesion layer
- Filling times: 0.7~5sec
- RLT target: 15 nm
- Dispense: 1.0 pL

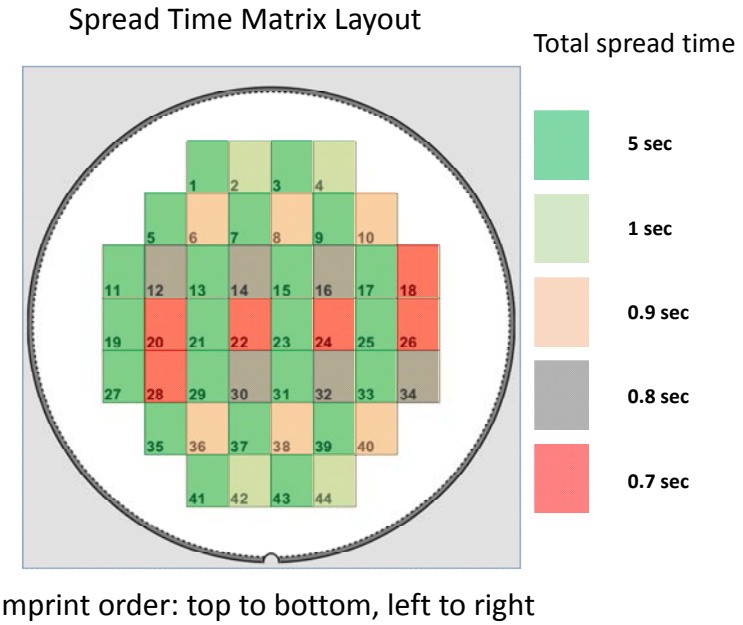

Figure 5. Matrix experiment used to study defectivity as a function of resist spread time.

Fill time was varied between 0.7 and 5 seconds, using an Imprio 500 stepper. A 28nm half pitch imprint mask was used for all fill time experiments and the residual layer thickness (RLT) was targeted for 15nm. The results of the experiment are shown in Figure 6. Plotted is non-fill defect density as a function of total spread time. Defect density is reduced to 0.1/cm^2 after a total spread time of 1 second.

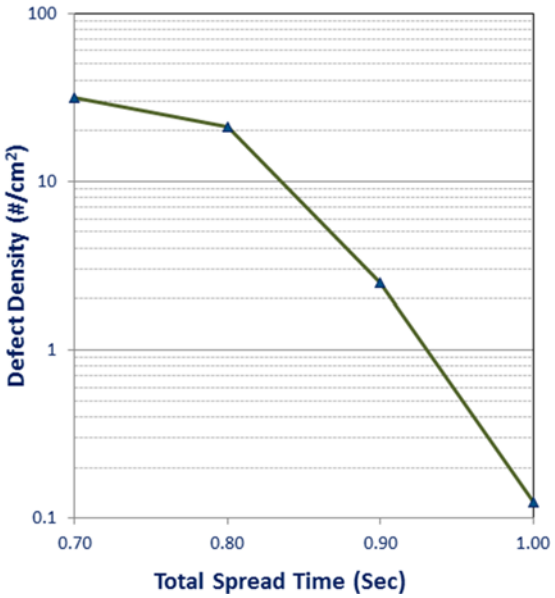

Figure 6. Defect density vs. total spread time. After one second the defect density is close to 0.1/cm^2.

An additional experiment was run to understand whether RLT uniformity was impacted as a result of implementing shorter spread times. Two different RLT values were targeted, and RLT uniformity was mapped within the 26 x 33 mm field. The results are shown below in Figure 7. For both cases (13 nm and 20 nm), the RLT variation was 1.4 nm, 3 sigma.

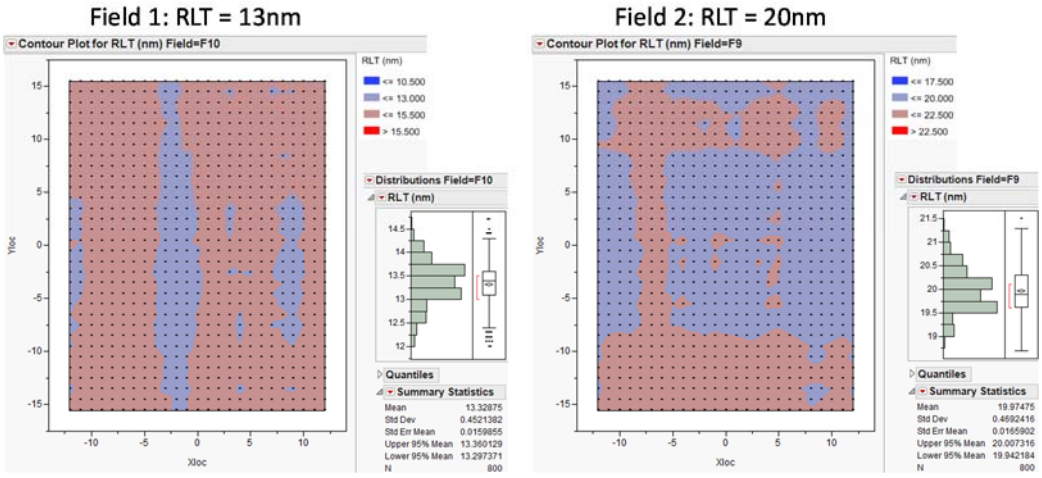

Figure 7. Residual layer thickness uniformity within a field, using 1 pL drop volumes and total resist spread time of 1 second. The in-field variation for both 13 nm and 20 nm was 1.4 nm, 3 sigma.

A final test was performed to verify that edge fields could also be printed at fill times of one second. Edge fields are challenging, since additional hardware and software controls are necessary to ensure uniform resist filling. One second fill times were achieved for all edge field cases. The photographs, in Figure 8, show a fully imprinted wafer (left) and a close up of several imprinted edge fields (right).

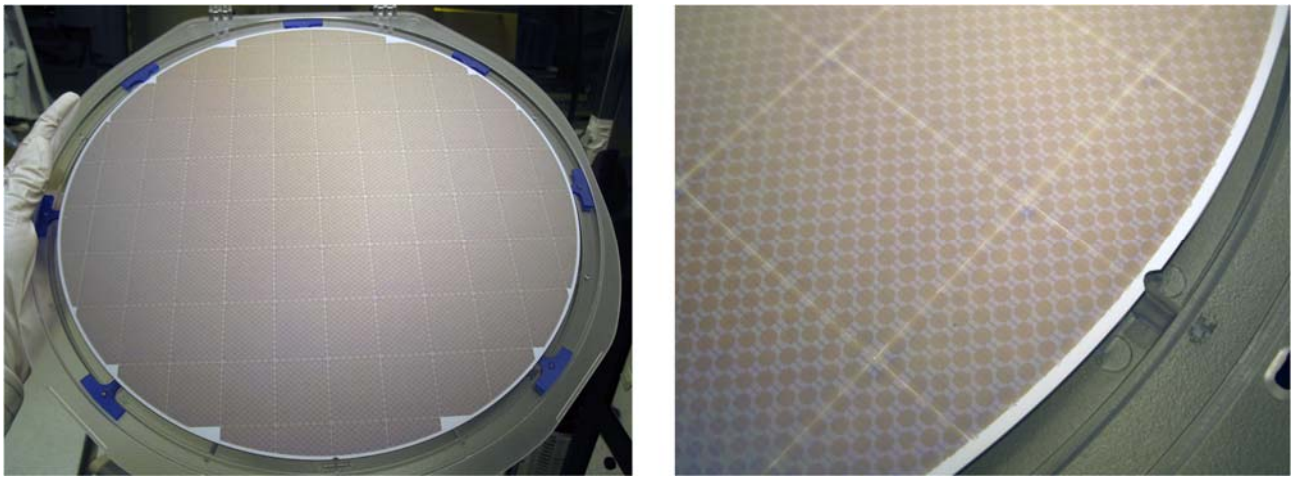

Figure 8. A fully imprinted wafer (left) and a close up of several imprinted edge fields (right).

Conclusions

To achieve a total process throughput of 20 wafers per hour, it is necessary to complete the resist fluid fill step in 1.0 seconds, making it the key limiting step in an imprint process. This work has demonstrated that defectivities of close to 0.1/cm^2 can be achieved, thereby enabling an imprint module throughput of 20 wafers per hour. Clustering of these modules will then result in tool throughputs of greater than 100 wafers/hour.

The next target is a total defectivity of 1 def/cm^2 after 10 lots, within an overall program goal of < 1 def/cm^2 after 20 lots. It should be noted that complimentary electrical test data has confirmed that the yield of 10 meter testers is greater than 90% for both open and short defects at 28nm. By addressing defect target requirements over the next 18 months, production readiness is anticipated for 2015.

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