New Methods for Fabricating Step and Flash Imprint Lithography Templates

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ABSTRACT

Step and Flash Imprint Lithography (SFIL) is an attractive method for printing sub-100 nm geometries. Relative to other imprinting processes SFIL has the advantage that the template is transparent, thereby facilitating conventional overlay techniques. The purpose of this work is to investigate alternative methods for defining features on an SFIL template. The first method used a much thinner (< 20 nm) layer of Cr as a hard mask. Thinner layers still suppress charging during e-beam exposure of the template, and have the advantage that CD losses encountered during the pattern transfer of the Cr are minimized. The second fabrication scheme addresses some of the weaknesses associated with a solid glass substrate. Because there is no conductive layer on the final template, SEM and defect inspection are compromised. By incorporating a conductive and transparent layer of indium tin oxide on the glass substrate, charging is suppressed during inspection, and the UV characteristics of the final template are not affected. Templates have been fabricated using the two methods described above. Features as small as 30 nm have been resolved on the templates. Sub-80 nm features were resolved on the first test wafer printed.

Keywords: SFIL, Imprint, Lithography, Templates

INTRODUCTION

Step and Flash Imprint Lithography (SFIL) is an attractive method for printing sub-100 nm geometries. Relative to other imprinting processes SFIL has the advantage that the template is transparent, thereby facilitating conventional overlay techniques. In addition, the imprint process is performed at low pressures and at room temperature, which minimizes magnification and distortion errors [1].

Early template fabrication schemes started with a 6" x 6" x 0.25" conventional photomask plate and used established Cr and phase shift etch processes to define features in the glass substrate [2]. Although sub-100 nm geometries were demonstrated, critical dimension (CD) losses during the etching of the thick Cr layer etch make the fabrication scheme impractical for 1X templates [3]. It is not unusual, for example, to see etch biases as high as 100 nm [4]. The purpose of this work is to investigate alternative processes for defining features on an SFIL template.

The first method considered used a much thinner (< 20 nm) layer of Cr as a hard mask. Thinner layers still suppress charging during the e-beam exposure of the template, and have the advantage that CD losses encountered during the pattern transfer through the Cr are minimized. Because the etch selectivity of glass to Cr is better than 18:1 in a fluorine based process, a sub-20 nm Cr layer is also sufficient as a hard mask during the etching of the glass substrate. The second fabrication scheme attempts to address some of the weaknesses associated with a solid glass substrate. Because there is no conductive layer on the final template, SEM and defect inspection are compromised. By incorporating a conductive and transparent layer of indium tin oxide (ITO) on the glass substrate, charging is suppressed during inspection, and the transparent nature of the final template is not affected.

2. EXPERIMENTAL DETAILS

In order to quickly establish baseline conditions, all experiments were run on either 100 mm Pyrex 7740 wafers or 150 mm quartz wafers. NEB-22 negative resist was exposed on a Leica VB6 system operating at 100 kV. The resist process used has been described previously [5]. Cr was deposited in an MRC 603 D.C. magnetron load locked sputtering system. A 1200 watt, 35 mTorr process run in a single pass mode was employed. The first test samples of ITO were supplied by Silicon Quest. Those films were D.C. sputtered at a power of 1 kwatt in 100% Ar at a pressure of 8 mTorr. Subsequent development was done internally in a customized RF sputter system operating at a power of 100 watts and an Ar/O_2 pressure of 6 mTorr. To further improve optical transmission and conductivity, the films were then annealed at 300 C for one hour. PECVD oxide was deposited in a Novellus Concept 1 system at a temperature of 250 ?C. All pattern transfer experiments were performed in a Unaxis VLR system. A chlorine and oxygen mixture was used to etch the Cr films. A CHF_3 based etch was used to pattern transfer either the PECVD oxide or the quartz substrates.

CD measurements and top down micrographs were taken with a Hitachi S7800 CD-SEM equipped with a cold cathode source and an automated pattern recognition system. The repeatability of the CD-SEM is 3.5 nm (3) for line measurements and 1.4 nm (3) for pitch. Cross-sectioned images were obtained with a Hitachi S4500 SEM operating at 5 kV.

3. THIN CR TEMPLATE PROCESS

To minimize CD loss Cr film layers as thin as 10 nm were deposited on 150 mm quartz wafers. A 180 nm thick NEB-22 resist was exposed on the VB6 and served as the hard mask for the pattern transfer of the Cr. The Cr was then used as the hard mask for the transfer of the image into the quartz. Following the quartz etch, the remaining resist and Cr were stripped away, thereby producing a final template. Typical etch depths into the quartz were 100 nm. A schematic of the process is depicted in Figure 1.

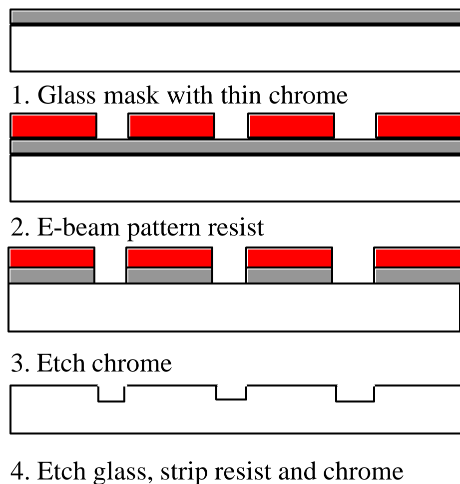


Figure 1. Schematic of a Cr based template

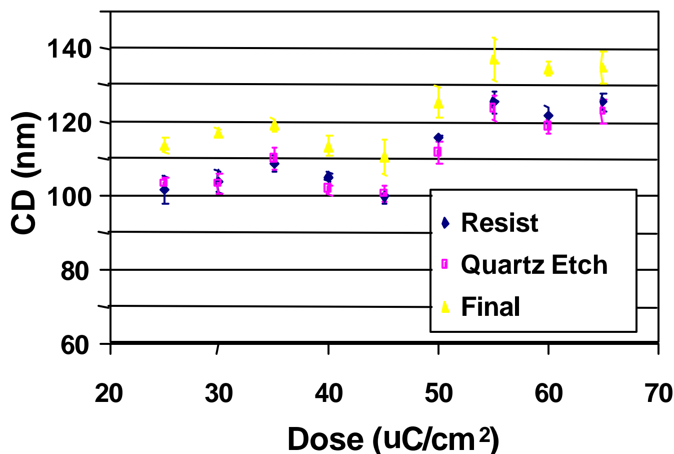


Figure 2. CD vs. exposure dose, before and after process pattern transfer.

Figure 2 depicts the change in CD for 100 nm lines as the template was processed. No discernable shift in CD was detected after the etching of both the Cr and quartz. After stripping the resist and Cr, the template was coated with a 5 nm blanket film of Cr (to avoid charging in the SEM) and measured again. A 10 nm shift was observed, and is most likely a consequence of the blanket charge reduction layer.

Figure 3 depicts SEM images of 30 nm trenches and 50 nm lines in the final template. These are the smallest features fabricated on an SFIL template to date.

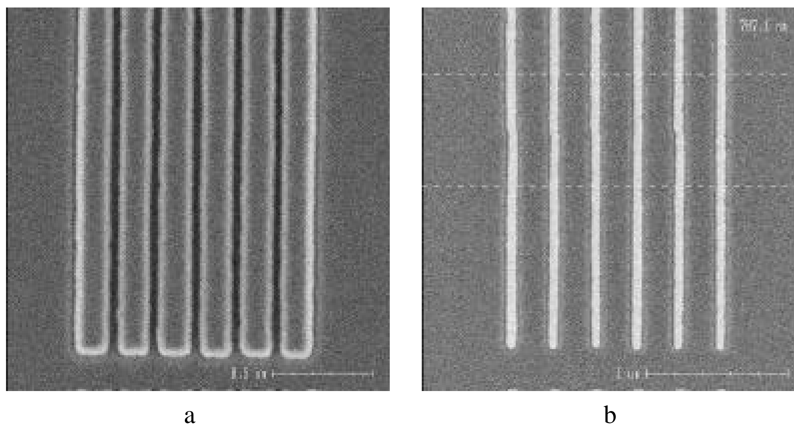


Figure 3. 30 nm trenches and 50 lines defined in an SFIL template.

4. OXIDE/ITO TEMPLATE PROCESS

Although the thin Cr process successfully maintains CD control, the final template presents several problems. SEM inspection is compromised, since the quartz substrate has no means for dissipating charge. Defect inspection is also difficult, since there is no material-based contrast. It is also very likely that sub-50 nm templates will require e-beam based defect detection schemes, which will also suffer from a lack of a charge dissipation layer.

To overcome these issues, we propose that a transparent conductive oxide, such as ITO, be deposited on the quartz. A PECVD oxide can then be deposited on the ITO. This oxide is coated with an e-beam resist, which is patterned and subsequently used as an etch mask for the oxide pattern transfer. Because fluorine forms no volatile products with either indium or tin, the ITO serves as an excellent etch stop. One possible fabrication scheme is depicted in Figure 4.

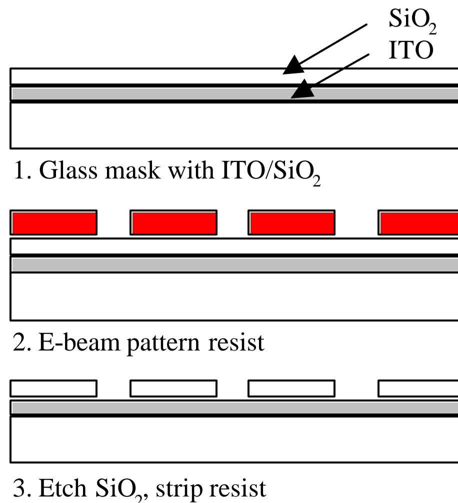


Figure 4. Template fabrication scheme incorporating an ITO layer.

Another advantage of the proposed process is improved selectivity between oxide and resist. Selectivities of better than 5:1 have been reported [7]. As a result, it should be possible to further thin the starting e-beam resist and obtain

even smaller features in both the resist and final template. Cross section images (using the process described above) of dense 70 nm and 100 nm lines are shown in Figure 5.

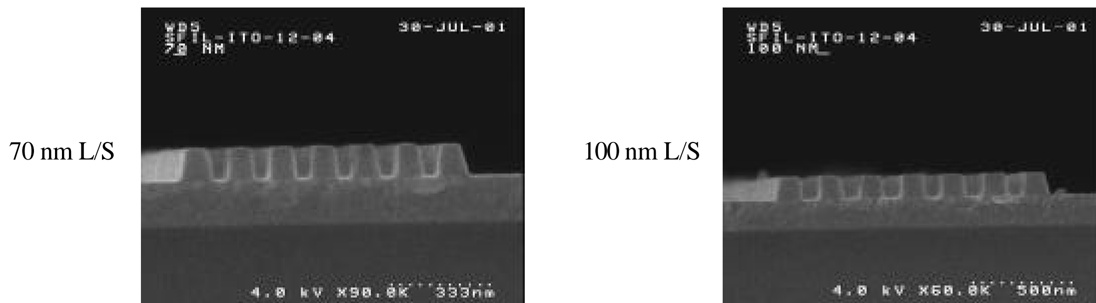


Figure 5. Cross section SEM images of dense 70 nm (a) and 100 nm (b) lines.

5. ITO PROPERTIES

The transparent conducting oxide, ITO in this case, must satisfy a large number of criteria to be successfully implemented. The material must be transparent at 365 nm (in order to polymerize the etch barrier layer during the SFIL imprinting process), but be reflective enough at 780 nm to allow the laser height sensor system of the VB6 to locate the template surface during template exposure. Resistivity must be low enough to allow e-beam writing and template inspection without charging. Additionally, the ITO must have minimal surface roughness, possess sufficient adhesion to SiO_2 in order to withstand the imprint process, and be compatible with the release layer that is applied to the template prior to imprinting.

To expedite process development, ITO samples were initially obtained from Silicon Quest. A parallel effort was also started in-house to develop an ITO deposition process. Although surface roughness is superior for the externally supplied material, there is a big difference in optical transmission between the two films. A comparison of 150 nm films is depicted in Figure 6. Transmission at 365 nm differs by about a factor of two. Although 80% transmission should be more than sufficient for the imprint process, further improvements are possible by optimizing the ITO thickness and surface characteristics. It is interesting to note that although there is a large disparity in transmission, resistivity of the films are nearly identical (~ 5 x 10^2 ohms/sq).

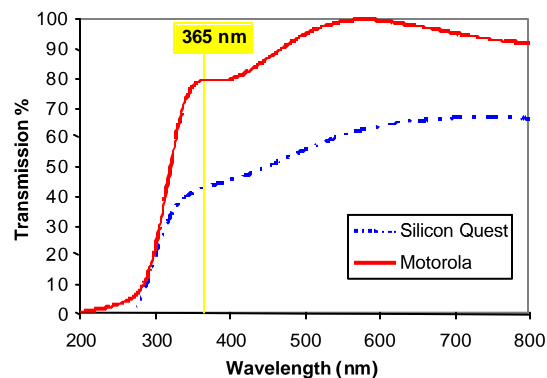
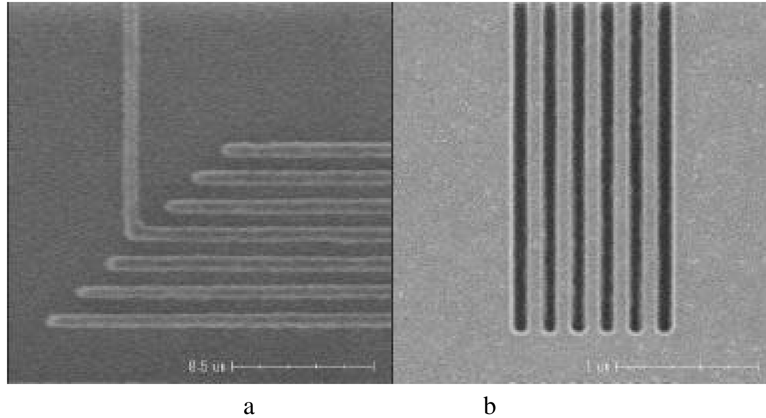


Figure 6. Transmission spectrum for two ITO films.

The ITO films also appear to be sufficiently conductive. Figure 7 depicts SEM images from an ITO based template taken after resist development, and after oxide etch and resist strip. No blanket charge dissipation layer was

applied prior to obtaining the images. 50 nm iso-dense features were well-resolved in the resist (Figure 7a), indicating that no local beam blurring occurred during writing. Figure 7b depicts 100 nm dense features after oxide etch and resist strip. Line edges are well delineated and the ITO surface texture is easily observed.



a b

Figure 7. SEM micrographs of an oxide/ITO template after resist development (a) and after oxide etch and resist strip (b).

6. IMPRINT PROCESS

A 248 nm Ultratech stepper has been converted to function as an imprint step and repeat tool, and has been detailed previously [3]. Templates and wafers were loaded and unloaded manually. Printing operations, including x-y positioning of the wafer, dispensing etch barrier liquid, z-translation of the template to close the gap between the template and wafer, UV curing of etch barrier, and controlled separation are all automated [8] and controlled with a LabVIEW interface. The system is currently configured to handle 1 inch square x 0.25 inch templates. For this study, a 0.75 x 0.75 inch section was cut from ... hed to a one-inch square with an optical adhesive .

An example of 70 nm features print... n Figure 8. The features are well defined and faithfully reproduce the images of th...

Figure 8. 70 nm images in the etch barrier, after imprinting.

7. DISCUSSION

Sub-70 nm features were resolved on templates using two different fabrication schemes. It should be possible to produce templates with even smaller geometries by decreasing both the electron beam resist thickness and the oxide thickness (or equivalently, the etch depth into the quartz). Future work will target feature sizes smaller than 25 nm. Because aerial image issues are avoided in the printing process, line shortening problems should be eliminated, bypassing the need for costly optical proximity correction on the template. One way to study this effect is to fabricate

a device with performance characteristics that are closely linked to the fidelity of the critical feature that needs to be printed. One possibility is an MRAM device. Variations in the MRAM bit shape are well known to cause fluctuations in the switching fields.

For applications more closely linked to CMOS technology, image placement and overlay (in addition to defect density) will require very tight template tolerances. Today's e-beam writing tools cannot meet the specifications for sub 50 nm image placement on either 1X masks or templates. Overlay issues during the imprint process must also be addressed. A recent study has indicated that it is feasible to align template and wafer by deliberately distorting the template with an array of piezo-electric actuators [9]. Experimental corroboration is still forthcoming.

CONCLUSIONS

Two methods for fabricating an SFIL template have been demonstrated. Both approaches are capable of defining features well below 100 nm. The oxide/ITO method is more appealing, however, since it shows promise for eliminating charging effects, rendering the final template suitable for both SEM and defect inspection. Both templates were also used to print features on a wafer using a prototype SFIL printing system. 70 nm features were clearly resolved after imprint. Future work will attempt to create templates with smaller geometries and improve the ITO characteristics.

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