Etching of 42 nm and 32 nm Half-Pitch Features Patterned Using Step and Flash® Imprint Lithography

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ABSTRACT

In this work, the authors demonstrate the suitability of Step and Flash® Imprint Lithography (S-FIL®) materials as a mask for patterning 42 nm and 32 nm half pitch features into a hardmask material. We present a zero etch-bias process with good silicon oxide to imprint resist selectivity and excellent line-width roughness (LWR) control. We demonstrate the required etch processes and mean value and uniformity of the residual layer thickness (RLT) necessary to maintain cross wafer CD uniformity for 42 nm and 32 nm half pitch dense lines. Finally, the authors present a mechanism for targeting the critical dimension by control of the imprint resist volume.

Keywords: Step and flash imprint lithography, S-FIL, Nanoimprint lithography, imprint lithography, hardmask etch, imprint resist volume, residual layer

INTRODUCTION

Imprint lithography has been included on the International Technology Roadmap for Semiconductors (ITRS) Lithography Roadmap at the 32 nm, 22 nm, and 16 nm nodes. As summarized in the Lithography ITRS, critical dimension control is called out as one of the key requirements of lithography.[1]

> Critical Dimension (CD) Control—The size of many features in a design needs to be precisely controlled. CD control needs to be maintained within each exposure field, over each wafer and from wafer to wafer. CD control is required for obtaining adequate transistor, interconnect and consequently overall circuit performance.[1]

Step and Flash Imprint Lithography (S-FIL) is a unique method for printing sub-50 nm geometries.[2,3,4] The authors have successfully imprinted and pattern transferred 42 nm and 32 nm half-pitch dense lines using the S-FIL process. Etching of these imprinted features is similar to etching of features obtained with conventional optical lithography. S-FIL has the added advantage of having little to no "foot" and a very straight (>86°) profile that replicates the imprint mask profile [Figure 1]. The authors demonstrate control of CDs, excellent line-width roughness control, and the suitability of S-FIL imprint materials as an etch mask for patterning sub-42 nm features.
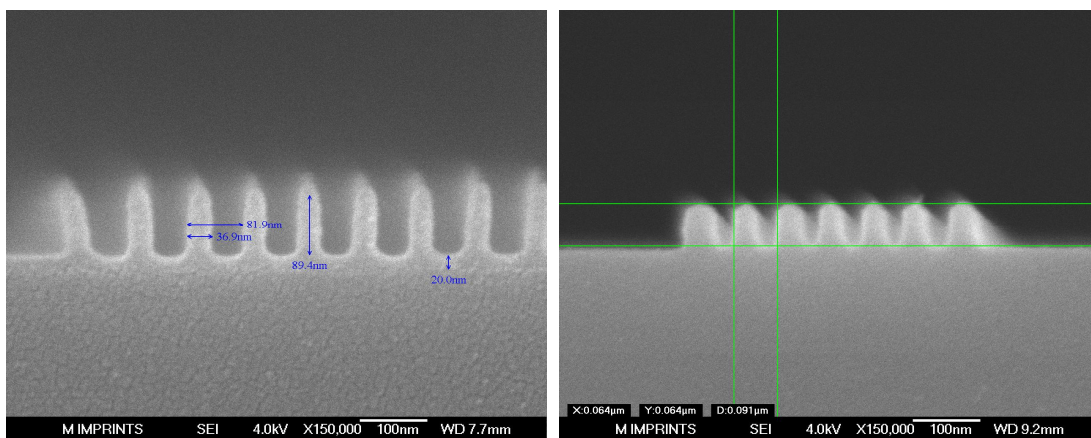

Figure 1 SEM micrograph of 42 nm half-pitch [left] and 32 nm half-pitch [right] line and space patterns at imprint over 50 nm thermal oxide on a silicon wafer.

Etch processes have been developed to etch imprinted features, based on S-FIL materials, into a 50 nm silicon oxide layer on silicon using a basic reactive ion etch tool. Such an oxide layer can perform as a hard mask for fabrication of subsequent layers. The etch processes used with S-FIL are similar to those used with conventional lithography. The CF_4-CHF_3-based silicon oxide etch process has a typical silicon oxide to imprint resist selectivity that ranges from 1:1 to 7:1. We have developed a high selectivity, zero-etch bias process over a range of CDs. This process has 100-105 nm of imprint resist before etch and 70-75 nm of imprint resist remaining after etching through 50nm of thermal silicon oxide. The imprint resist is easily stripped after pattern transfer with an *in situ* oxygen ash followed by a standard wet clean. The line width roughness (LWR) throughout the etch steps closely follows the LWR of the imprinted features.[5]

A thin residual layer of the imprint resist, the thickness of which can be controlled by the imprint process, remains below the features. This residual layer is thin enough to be easily removed by a short etch step analogous to the ubiquitous BARC removal or photoresist trim etch commonly used with conventional lithography. The residual layer thickness (RLT) uniformity is critical to pattern transfer fidelity. The authors demonstrate the required RLT uniformity to maintain cross wafer CD through pattern transfer into thermal silicon oxide. The ratio of the maximum RLT to the feature height plays an important role in determining the etch bias through pattern transfer and in defining the imprint mask specifications. Since the trim etch time is fixed, the etch bias varies with the mean residual layer thickness. Etch process conditions will be presented that control the slope of this relationship allowing fine control of CDs across the wafer.

IMPRINT LITHOGRAPHY VS. OPTICAL LITHOGRAPHY

The process flow for standard, optical lithography usually includes a "descum" step to remove any undeveloped resist, developer residue, or footing at the base of the resist. An antireflective coating (ARC) layer etch normally follows the descum step. The descum process is typically a process rich in oxygen. The ARC etch is either an oxygen-rich process for an organic ARC or a process similar to hardmask etch chemistry for a dielectric ARC (DARC). The residual layer etch used with imprint lithography can be performed with either etch chemistry and with comparable etch time [Figure 2]. After this residual layer etch step, the process flow is identical to that for optical lithography. Figure 3 compares the imprinted and optical lithography pattern stacks.
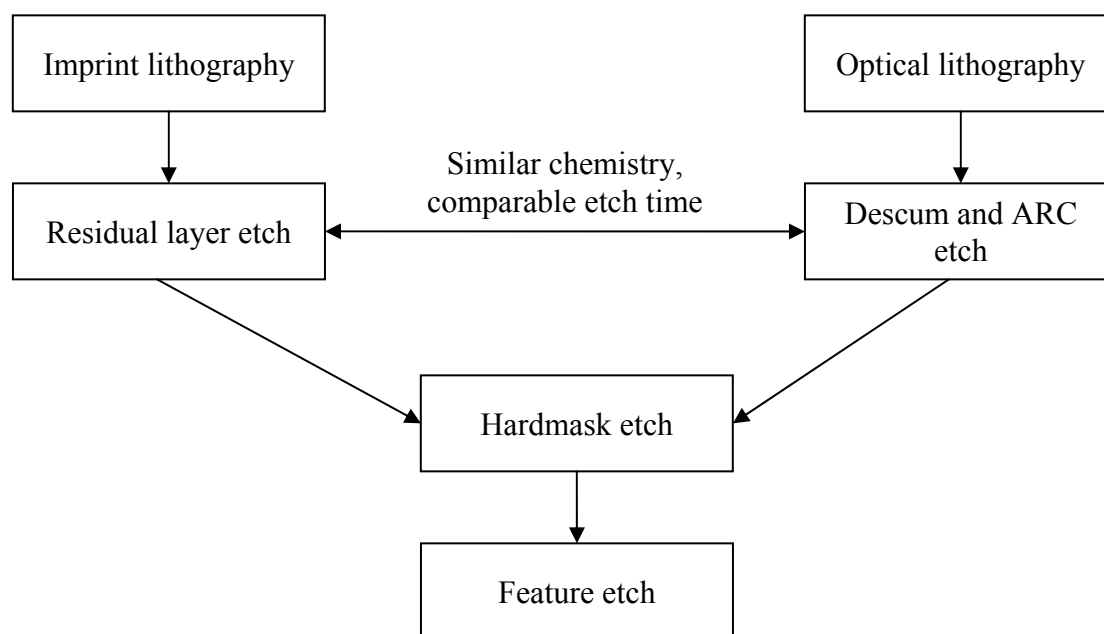

Figure 2 The process flow for imprint lithography is analogous to the process flow for optical lithography.
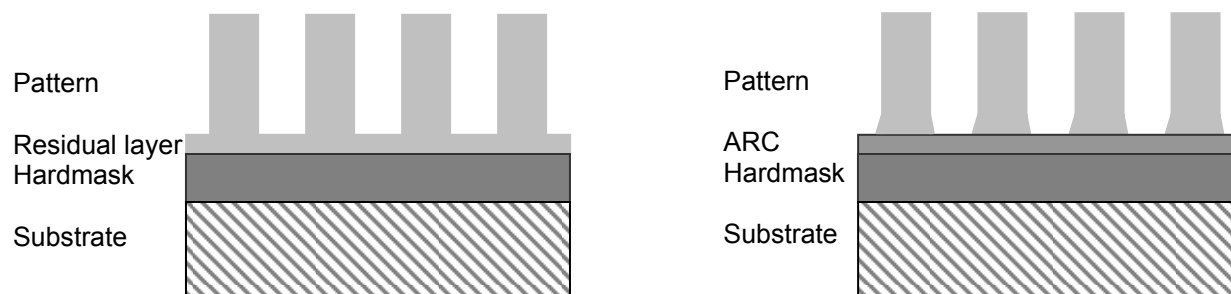
Figure 3 The imprint pattern stack (left) includes a small residual layer above the hardmask layer and the optical lithography stack (right) includes an antireflective coating layer.

HARDMASK ETCH PROCESS DEVELOPMENT

A hardmask etch process for 50 nm of silicon oxide was developed that followed the flow introduced in section 2. The wafers used in this development included the imprint pattern with a residual layer thickness (RLT) over 50 nm silicon oxide. This silicon oxide thickness models a typical hardmask.

1.1 Processing equipment

This etch process development was undertaken using a research-grade reactive ion etch system manufactured by Trion Technology, Inc [Figure 4]. This parallel plate system is powered with a 13.56 MHz RF generator. A variety of fluorine-containing gases (CF_4, CHF_3, SF_6) as well as carrier gases (Ar, He, N_2) and oxygen are available on the system. This system uses a ceramic clamp system to hold the wafer in place and to allow for helium backside cooling. Optical emission spectroscopy was available for process monitoring but was not integrated into the system for automatic endpoint and overetch control.
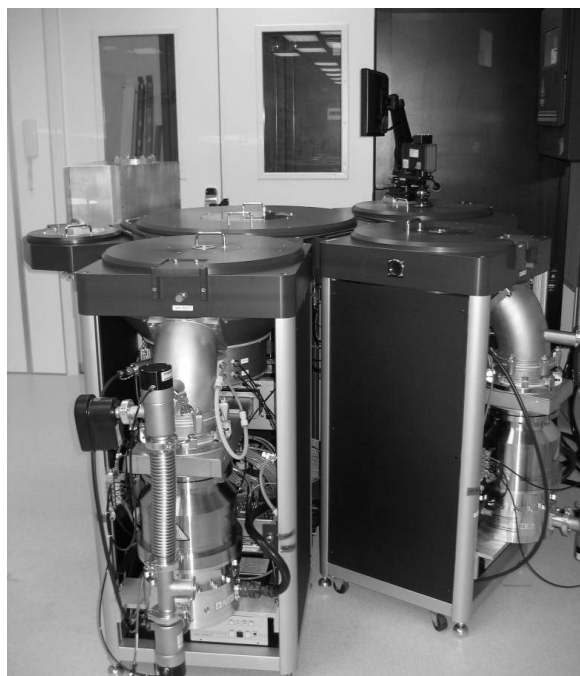

Figure 4 The Trion Technology, Inc. RIE reactor is located in the University of Texas in Austin microelectronics research facility.

1.2 Imprint mask field layout

The imprint mask used for the initial process development has a 65 mm x 65 mm overall with a 32 nm x 26 nm imprint field. The pattern includes eight groups of 2 mm lines ranging from 42 nm half-pitch to 60 nm half-pitch. The overall pattern has a dummy fill pattern with 50% loading.

A second imprint mask with minimum features 32 nm half-pitch was used for process transfer to smaller feature sizes. This second imprint mask included a 16 x 13 array of line/space patterns at 32 nm, 36 nm, 40 nm and 44 nm half-pitch. All imprinting was performed on the Imprio® imprint lithography system manufactured by Molecular Imprints, Inc.[6]

1.3 Residual layer etch development

The initial process step for imprint lithography is to remove the residual imprint resist layer. This layer is etched with a process analogous to the descum and ARC etch steps used with standard lithography and will be referred to as the "descum process" in this paper. A variety of etching conditions can be chosen for this initial step. In this work we have studied an O_2/Ar-based descum and a CF_4/CHF_3-based descum.

Isotropic, oxygen-rich processes generally reduce, or "trim," the critical dimension (CD) more than low-oxygen processes. Anisotropic processes are less likely to trim the CD. The addition of argon combined with low pressure produces a process that, if timed correctly, causes very little CD loss. The descum process chosen as a starting-point condition is a low pressure, low power process with low oxygen flow and using argon as a non-reactive, carrier gas. These conditions were expected to be highly anisotropic, and that property was confirmed by cross-sectional SEM micrographs of the profile [Figure 5].
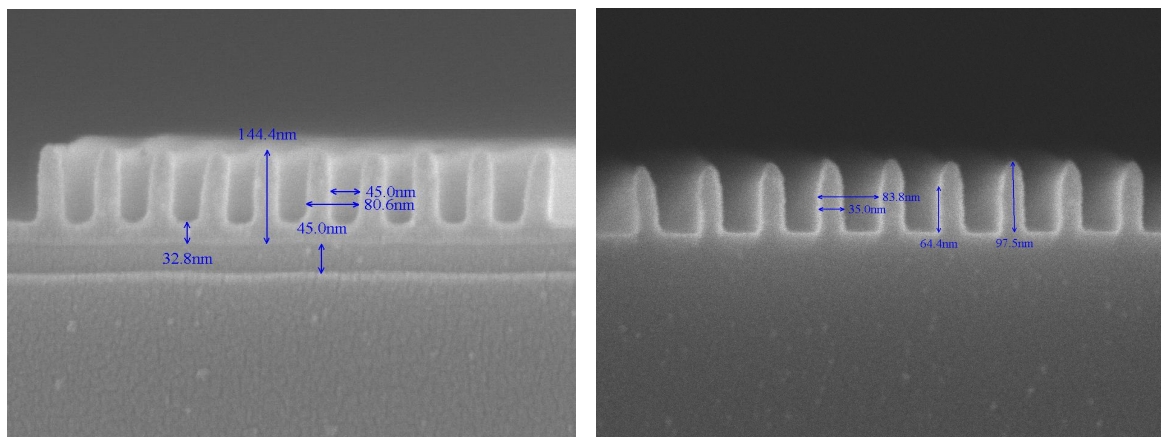

Figure 5 Cross-section of the initial imprint (left) and mask profile (right) following the descum step for 42 nm half-pitch dense lines. The post-descum imprint profile has straight sidewalls with no footing after residual layer removal.

As illustrated in Figure 5, the imprint profile has a height of 110 nm and has straight sidewalls with a small foot at the bottom. (This foot has occurred because the imprint mask did not have an optimized etch process during its manufacturing and has been corrected in development of later imprint masks.) Following the descum etch, the sidewall profile is near 90° and all the evidence of footing has been removed. The straight region of the mask, which will define the profile in the subsequent etch, is 65 nm tall and there is 95 nm of resist remaining overall.

1.4 Hardmask etch development

Anisotropic plasma etching of silicon oxide films involves the balancing of three mechanisms: sputtering, which removes material by physical bombardment; chemical etching, which removes material through a chemical reaction between the etching gases and the material being etch; and chemical deposition, which protects the sides of features. Sputtering is not very selective; i.e., it removes both resist and material to be etched at roughly the same rate. Chemical etching can be much more selective, removing the material of interest at a higher rate than the resist mask. However, chemical etching is not directional and must be enhanced by sputtering to enhance etching in the vertical direction. Chemical deposition can mitigate CD changes by protecting the sides of features.

A common etching chemistry for silicon oxide includes the gases CF_4, CHF_3, and Ar. This allows for a very flexible etch process. The process conditions, particularly the relative concentration of CF_4 and CHF_3, can be used to control the ratio

of silicon oxide to resist etch rate. This ratio is commonly referred to as the *etch selectivity*. Argon functions as a non-reactive carrier gas and enhances sputtering to provide a very anisotropic etch process. CF_4 and CHF_3 both contain fluorine, the primary chemical etching species for silicon oxide. CF_4 and CHF_3 can also be used to create polymer formation and this polymer provides sidewall protection and maintains the CD.

If a highly polymerizing process is used, the CD can actually increase as excess polymer is deposited on the sidewalls. Figure 6 illustrates this phenomenon in our initial hardmask etch process. For this starting-point process, the line width was increased by approximately 15 nm. This change in CD illustrates strong effect that the etch process can have on final CD. This phenomenon is not unique to imprint lithography. The same trend occurs with optical lithography as well.
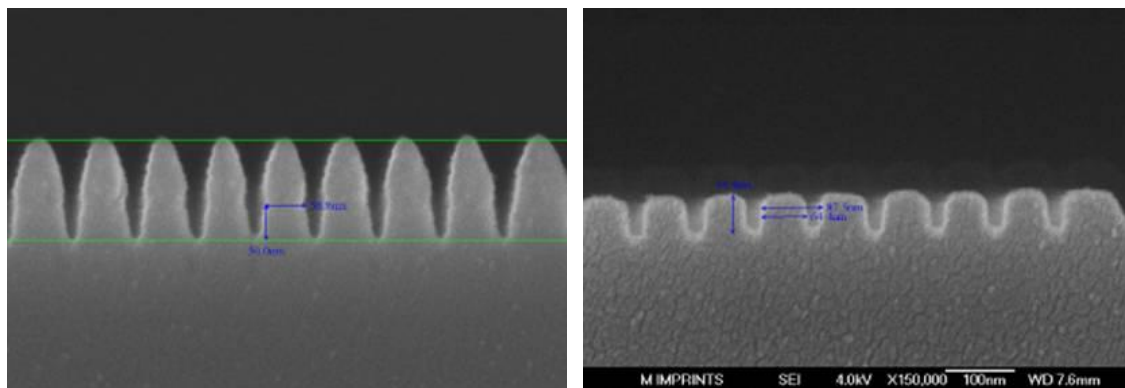

Figure 6 Cross-section of etched hardmask before (left) and after (right) resist strip for 42 nm half-pitch dense lines. This process showed high polymer formation and thus increased critical dimension on the lines.

1.5 Baseline process

The process described above was refined to better balance the polymer formation and etching. Some general trends were observed during the process development. As the CHF_3:CF_4 gas flow rate ratio is increased, polymer formation is enhanced. Pressure also significantly affects polymer formation, with the tendency of higher pressure to increase polymer formation. Higher bias power enhances argon sputtering and thus makes the process more anisotropic and the profile more vertical.

Cross-sectional images of the final profile in silicon oxide [Figure 7] show an etch profile of about 85°. This process maintains the CD throughout the etch process as shown in Figure 8. Top-down images like these were used to measure the CD and line width roughness (LWR) of the features. The CD was 36.2 ± 2.9 nm (3σ) at the imprint stage and was 36.7 ± 2.9 nm after the hardmask etch and resist strip. These measured values were calculated using the Simages® image analysis package published by Smart Imaging Technologies Co.[7] with the line edge level set at 60%.
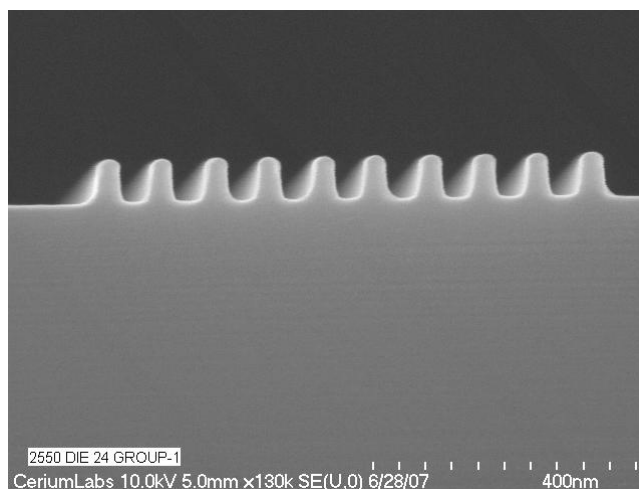

Figure 7 Cross-sectional SEM micrograph of final process etched into 50 nm thermal oxide.

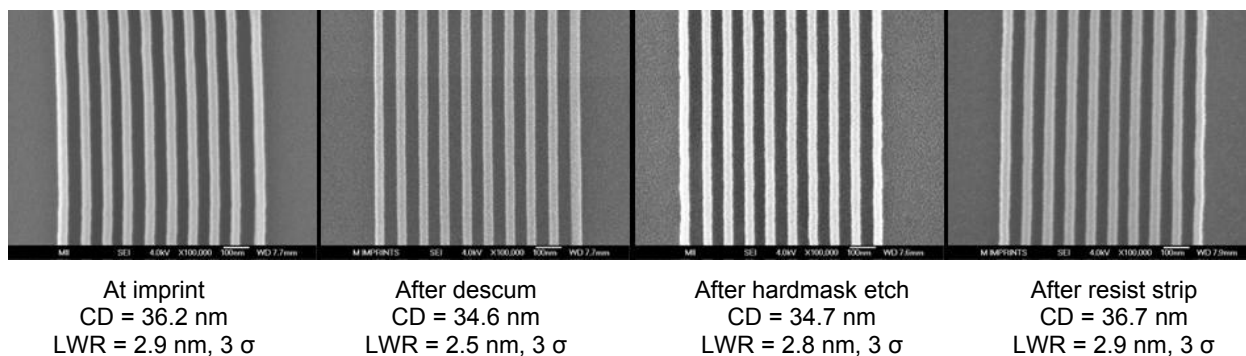| At imprint	After descum	After hardmask etch	After resist strip
CD = 36.2 nm	CD = 34.6 nm	CD = 34.7 nm	CD = 36.7 nm
LWR = 2.9 nm, 3 σ	LWR = 2.5 nm, 3 σ	LWR = 2.8 nm, 3 σ	LWR = 2.9 nm, 3 σ

Figure 8 Top-down SEM micrographs of 42 nm half-pitch lines at etch process step. The critical dimension was maintained at ~35 nm throughout the process. Line width roughness (LWR) was also monitored and remained at 2.9 nm, matching the LWR at imprint.

Following process development, a fully patterned wafer was etched using the above process: an O_2/Ar descum process followed by CF_4/CHF_3/Ar mask etch process. Optical emission spectroscopy was used to monitor the process. Carbon monoxide emission (CO I) typically decreases as the silicon oxide film is removed because carbon monoxide is a byproduct of silicon oxide etching with CF_4. The graph of CO I emission plotted as a function of time indicates that the imprint resist is robust through 100% overetch. [Figure 9]
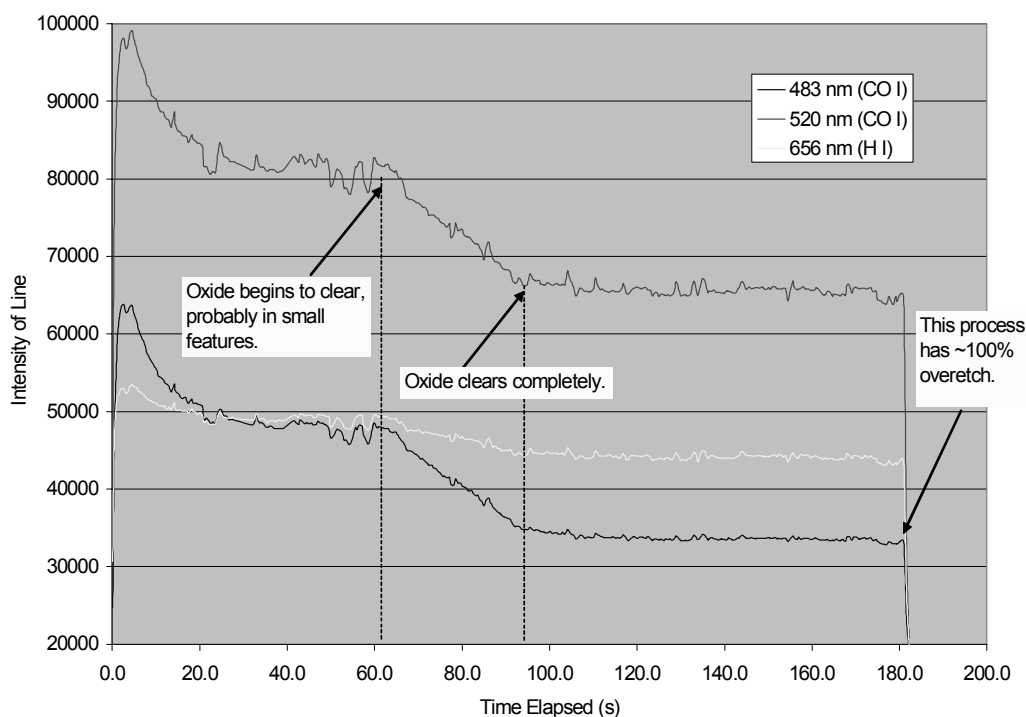

Figure 9 Optical emission as a function of time for wavelengths commonly monitored for silicon oxide endpoint.

The mask layout includes multiple CDs and pitches. For the fully patterned wafer, top-down critical dimension measurements were made at each line pitch at both imprint and after etching. These same data (CD at imprint, after descum, after hardmask etch, and after resist strip) are plotted in Figure 10 for all of the eight sets of lines and spaces. The process showed good linearity; that is, the CD change did not depend upon incoming CD.

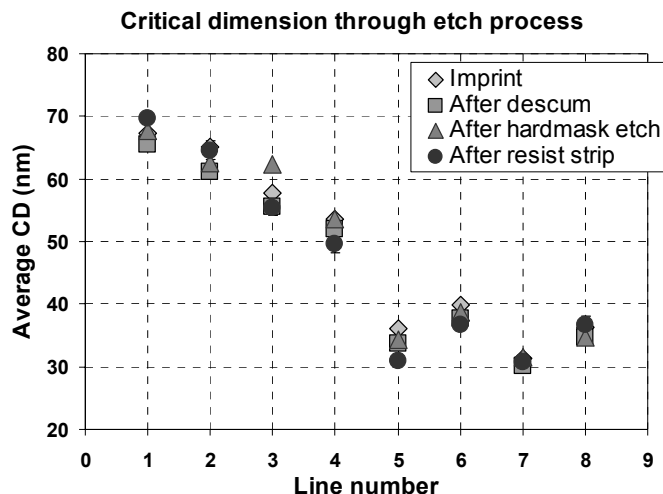**Critical dimension through etch process**

Figure 10 The critical dimension is plotted for eight nominal pitch values. The change in critical dimension between imprint and after etch and resist strip remains consistent through a variety of nominal critical dimensions.

1.6 Process transfer to 32 nm half-pitch

The baseline process developed for 42 nm half-pitch was used to etch a second pattern with 32 nm half-pitch as the smallest feature size. This baseline process showed considerable CD loss in the final oxide hardmask. Further process development created a second process that had little CD loss. [Figure 11]

To address the critical dimension loss, a $CF_4/CHF_3/Ar$ descum process was developed. This process targeted a 1:1 selectivity between the silicon oxide to imprint resist etch rate. The $CF_4/CHF_3/Ar$ descum process has the advantage of better CD control during the descum and this property was found to be particularly helpful as the line width becomes smaller.

At imprint
CD = 35.5 nm

O_2/Ar descum
CD = 19.3 nm
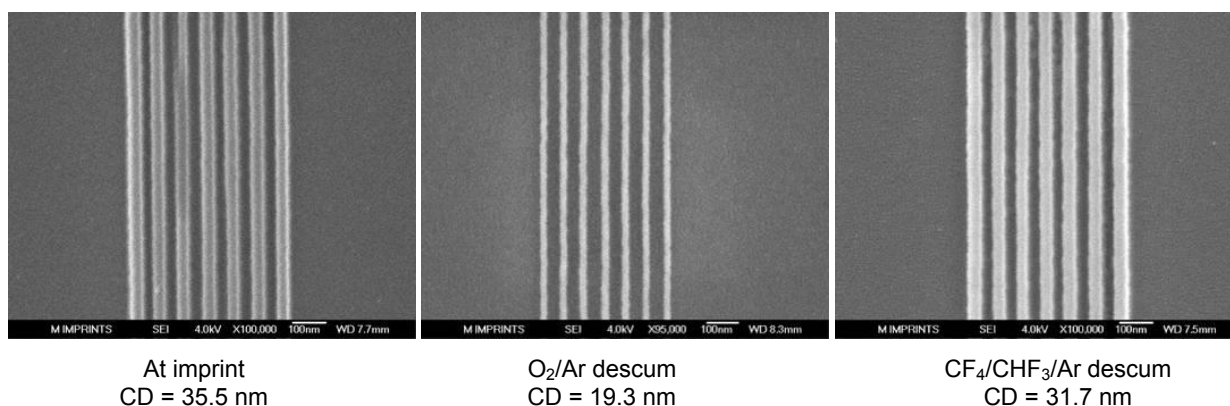
$CF_4/CHF_3/Ar$ descum
CD = 31.7 nm

Figure 11 Top-down SEM micrographs illustrating the critical dimension comparison for two different etch processes. The SEM images are taken at imprint (left), after O_2/Ar descum (center), and after $CF_4/CHF_3/Ar$ descum (right) followed by the same hardmask etch process.

CONTROL OF CRITICAL DIMENSION USING IMPRINT VOLUME

Consider the relationship between residual layer thickness (RLT) and critical dimension (CD). If the CD does not strongly depend upon RLT or varies only weakly with RLT (Process A in Figure 12) then small variations in residual layer will have minimal effect upon the final CD. Consider the case in which the critical dimension does vary with RLT (Process B or Process C in Figure 12). This relationship could be used to target a desired final CD as a function of field location or within different regions of a single field. Such a relationship could function as a means to offset non-uniformities from other process steps, similar to "dose control" using in photo and e-beam lithography.
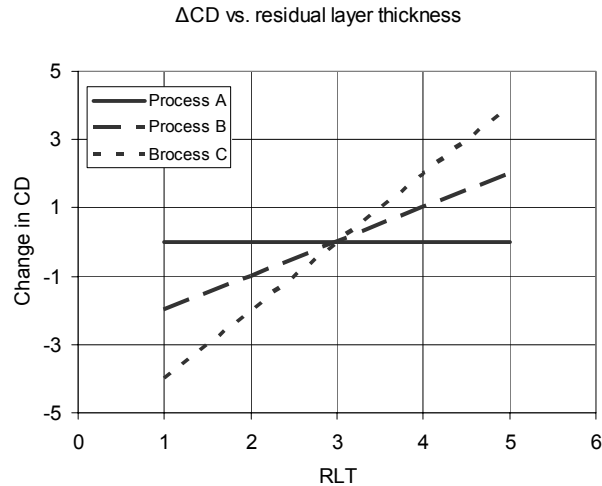
ΔCD vs. residual layer thickness

Figure 12 Hypothetical relationship between imprint volume and CD change through process (ΔCD). Process A illustrates ΔCD unchanged with respect to imprint volume, while Process B and Process C illustrate linear relationships.

1.7 Imprint volume and residual layer thickness

Molecular Imprints' Step and Flash Imprint Lithography (S-FIL) technology allows for precise control of the volume of imprint resist. The residual layer thickness (RLT) can be controlled by varying the drop volume or the drop placement within the pattern.

A series of imprint resist volumes was used to pattern a wafer and to target a different mean residual layer thickness at five field locations across the wafer. The residual layer thickness was allowed to vary from very thin to greater than 50 nm. Cross-sectional SEM images were taken to verify the RLT across the wafer. [Figure 13]

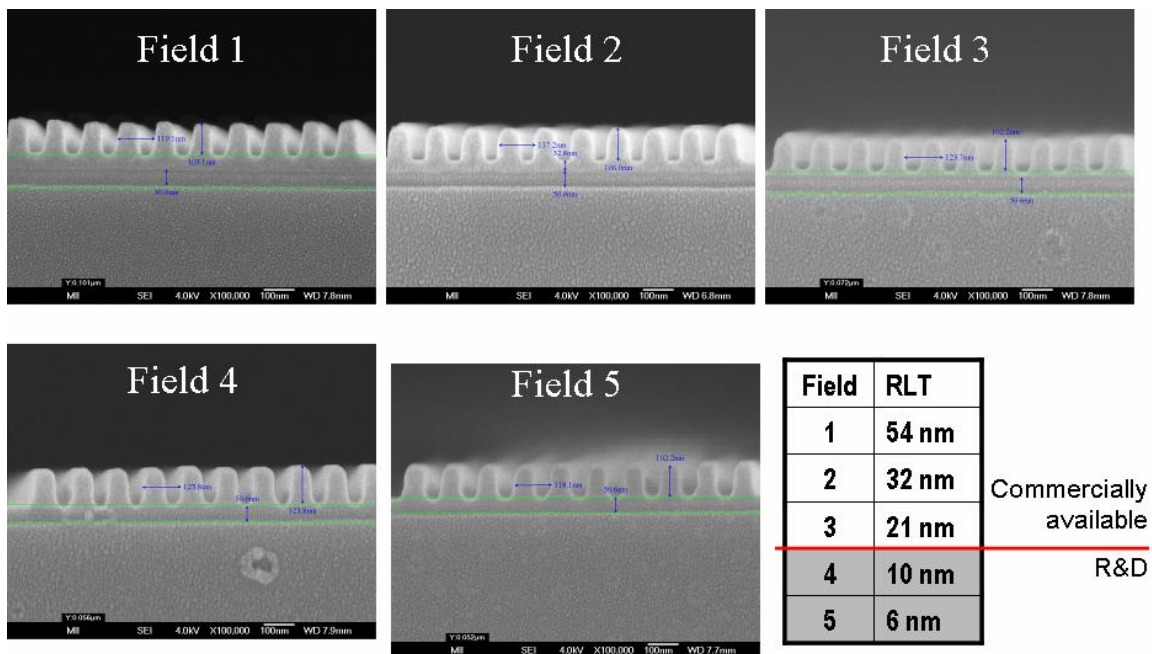| Field	RLT
1	54 nm
2	32 nm
3	21 nm
4	10 nm
5	6 nm

Commercially available

R&D

Figure 13 Cross-sectional SEM micrographs of 42 nm half-pitch dense lines for targeted residual layer thickness control across five imprinted fields. The layers were highlighted by performing a brief HF dip after cleaving the wafer to etch back about 5 nm of the silicon oxide. Residual layer thicknesses in gray are for research and development purposes and are currently not available on commercial tools.

1.8 CD control in oxide: O$_2$/Ar descum process

The etch process conditions (O$_2$/Ar descum etch followed by CF$_4$/CHF$_3$/Ar hardmask etch) described in Section 3.5 above were used to etch the targeted RLT patterns. The descum time was chosen to remove the largest (54 nm) residual layer thickness, thus the CDs were trimmed through the process. The CDs of the dense lines of each field and at each nominal pitch were measured before and after etch. The average change in CD (ΔCD or CD Bias) was recorded as a function of RLT and a strongly linear relationship was discovered. [Figure 14] The linear relationship predicts that 1 nm of CD bias can be expected from 3.3 nm of RLT variation.
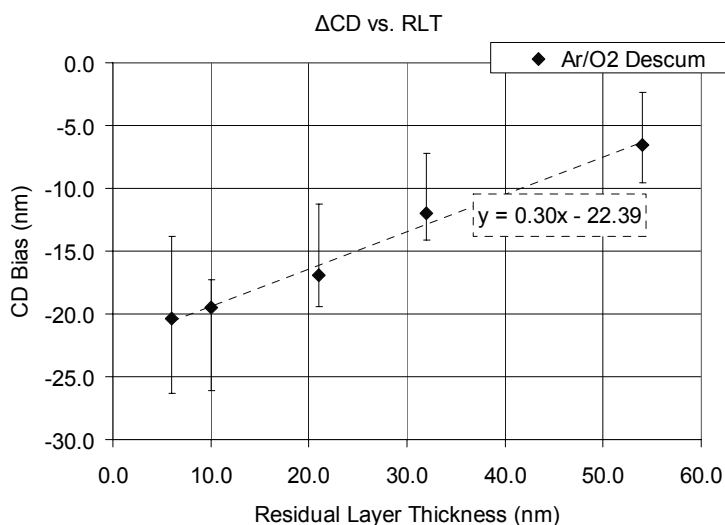

Figure 14 Change in critical dimension as a function of residual layer thickness for baseline process conditions.

1.9 CD control in oxide: CF$_4$/CHF$_3$/Ar descum process

The alternate etch process conditions (CF$_4$/CHF$_3$/Ar descum etch followed by CF$_4$/CHF$_3$/Ar hardmask etch) described in Section 3.6 above, was also used to etch the targeted RLT patterns. For this process, the overall CD bias is much smaller than with the baseline process. For these process conditions, the linear relationship predicts 1 nm of CD bias can be expected from 4.3 nm of RLT variation. However, if we look more closely in the recommended imprint regime (RLT > 15 nm) the critical dimension changes only 2.5 nm with more than 20 nm of residual layer variation. This relationship predicts 1 nm of CD bias can be expected from 8 nm of RLT variation.
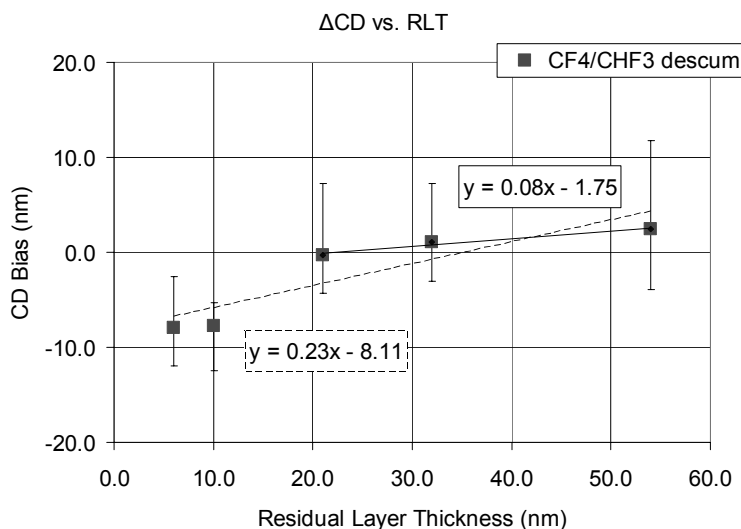

Figure 15 Change in critical dimension as a function of residual layer thickness for alternate process conditions.

S-FIL techniques control the residual layer thicknesses (RLT) at an average of 15 nm range with less than 5 nm of total thickness variation per imprint field across the wafer. Such control is possible even under a variety of imprinted features using the drop on demand technique, which directs the imprint material volume to be placed exactly where it is needed based on pattern density.

An example map of RLT for the Imprio 250 is shown in Figure 16. Further reductions in the thickness variation should be realized with the use of smaller drop volumes, technology that is currently under development at Molecular Imprints. Such control is possible even under a variety of imprinted features using the drop on demand technique, which directs the imprint material volume to be placed exactly where it is needed based on pattern density.
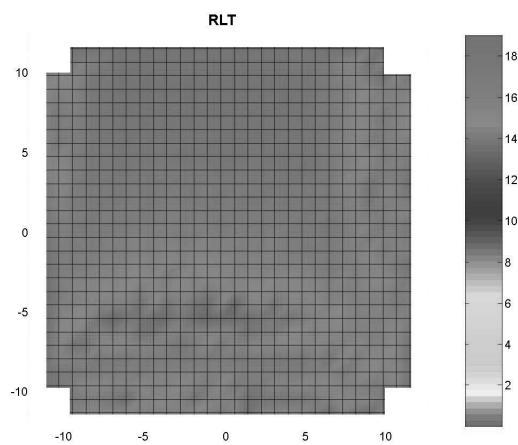

Figure 16 Graph of a typical area plot of residual layer thickness of an imprint from Molecular Imprints' Imprio 250. The mean thickness is 15 nm with a total variation of 5 nm.

DISCUSSION

We have approached the development of a hardmask etch process using Step and Flash Imprint Lithography (S-FIL) from the assumption that etching with imprint lithography is not significantly different from etching with optical lithography. Imprint lithography has a thin residual layer of imprint resist below the pattern. This residual layer is analogous to the antireflective coating layer commonly used in optical lithography. The residual layer can be removed with the same etch chemistry as is commonly used for descum of residue found in optical lithography and the ARC etch. Following the descum etch, transferring the pattern into the hardmask proceeds the same way with either imprint or optical lithography. In this work, Step and Flash Imprint Lithography (S-FIL) has been shown to be suitable for patterning a silicon oxide hardmask. Etch processes were developed for 42 nm and 32 nm half-pitch lines and spaces.

We have shown that imprint resist volume can be used to target the residual layer thickness below an imprinted pattern. We have demonstrated control of the critical dimension using targeted residual layer thickness. Additionally, we have shown that the dependence of critical dimension with respect to residual layer thickness can manipulated by using the etch process conditions.

The control of critical dimension with imprint resist volume or residual layer thickness can play an important role in compensating for process non-uniformities either earlier or later in the process flow. Drop-on-demand imprint resist allows for precise control of the residual layer thickness. The residual layer can be controlled across the wafer on a field-by-field basis. Such control could be used to compensate for systematic non-uniformity in an etch processing chamber. The residual layer thickness (RLT) could also be controlled within a single field based on, for example, the pattern density. The within-field control might be used to compensate for etching differenced due to pattern loading or critical dimension (CD) variation in different regions of the field layout.

ACKNOWLEDGEMENTS

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