Study of nanoimprint applications toward 22nm node CMOS devices

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ABSTRACT

Nanoimprint lithography is one of the candidates for NGL. Recently, the "S-FIL TM" (Step and Flash Imprint Lithography) has been developed by MII (Molecular Imprints, Inc.). Accordingly, it is necessary to build next-generation devices and study unit processes without delay. Because of good resolution, CD uniformity and LER, nanoimprint lithography is attractive. However, nanoimprint lithography (S-FIL) involves risks. In order to judge whether the S-FIL is applicable to the study of unit processes and test device fabrication, we had studied the feasibility of S-FIL technology.

As a result of previous work, we obtained the results of basic evaluation and confirmed the applicability of nanoimprint lithography for unit process study and basic test device fabrication.

However, application of nanoimprint lithography to various test devices requires the template resolution of 22nmHP, OL accuracy on multilayer resist, and defect density for various patterns. Therefore, in order to judge whether the S-FIL application is extendable to various test devices, we studied the characteristics of S-FIL.

As a result of this work, we confirmed that the nanoimprint application is extendable to fabrication of various test devices. And as a result of basic evaluation, improvement of template resolution is confirmed and the value of 22nmHP is obtained. We confirmed the robustness of the alignment process. The defect density is related in pattern density and spread time. Thus, reduced DD without throughput loss is required.

Keywords: Nanoimprint lithography, S-FIL, CMOS devices, Template

1. INTRODUCTION

In the CMOS semiconductor device (memory and logic) industry, there is a growing need to shrink the pattern size. Thus, a great deal of work has been done on the development of lithography technology. However, we have encountered several major barriers in lithography, including rising cost, delay in the development of a high-resolution tool, and poor performance of resist (materials and process).

On the other hand, nanoimprint lithography is one of the candidates for NGL. In fact, nanoimprint lithography has been included in the ITRS lithography roadmap at the 32nm node CMOS devices and beyond.

Accordingly, it is necessary to build next-generation devices and study unit processes without delay. Because of good resolution, CD uniformity and LER, nanoimprint lithography is attractive.

Recently, the "S-FILTM" (Step and Flash Imprint Lithography) has been developed by MII (Molecular Imprints, Inc.). S-FIL involves deposition of monomer droplets on the substrate across the single-shot area while controlling droplet positions and volume, making template approach a substrate, executing alignment and UV exposure, and executing template separation. These processes are performed for every shot.

However, the nanoimprint (S-FIL) involves risks concerning overlay accuracy, residual layer thickness, and defectivity. In order to judge whether the S-FIL is applicable to the study of unit processes and test device fabrication, we previously studied the feasibility of S-FIL technology.

As a result, we confirmed applicability of nanoimprint to the study of unit processes and basic test device fabrication. In detail, the CD variation was found to be less than 0.8nm. The LER was less than 2nm. Overlay accuracy of test device was less than 20nm. The RLT was controlled to the target of 15nm, and deviation was about 4nm. Template resolution of dense L&S pattern in early 2007 was about 24nm-HP. Defectivity became less than 10pcs./cm2.

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2. OBJECT

However, application of nanoimprint lithography to various test devices involves several issues. Figure 1 show those issues. The first is template resolution. The template resolution was insufficient for making 22nm node test devices. The second is robustness of OL accuracy on various film stacks. For making small feature size test device, the multilayer resist system is advantageous in terms of etch, but the alignment mark may be filled by the underlayer of multilayer resist. As a result, the alignment mark may not be visible. So we need to evaluate overlay accuracy on various film stacks. The third is defect density for various pattern densities. There are many pattern variations for real devices. So, we need to evaluate correlation with defect density and pattern density.

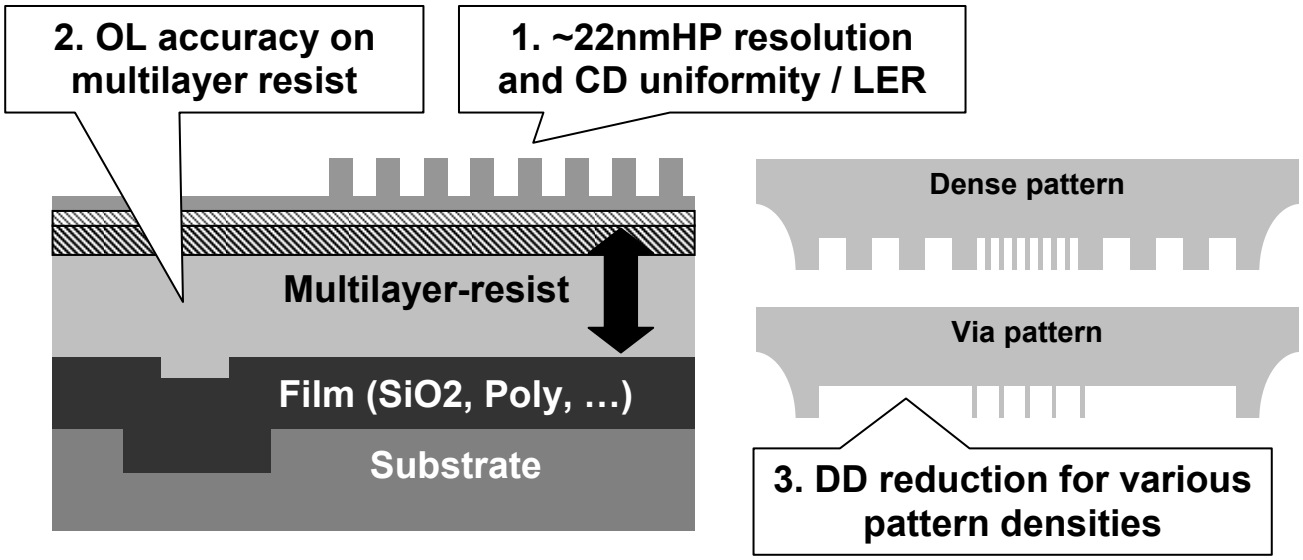


Fig. 1. Schematic drawings showing issues to be confirmed or improved

Therefore, in order to judge whether the S-FIL application is extendable to various test devices, we studied the above-mentioned three characteristics of S-FIL.

3. EVALUATIONS AND RESULTS

3.1 Template resolution, CD uniformity and LER

First, referring to the previous work, we discuss template resolution. We think dense line & space pattern is important as an indicator of resolution. So, we evaluated dense lines & spaces. Figure 2 shows the micrograph taken by CD-SEM (Hitachi). These are examples from early 2007. In the upper row are images of template etched chromium and quartz, and in the lower row are images of imprinted patterns on wafer. The template was patterned with Gaussian beam EB-writer. It seems the template could resolve 22nmHP L&S pattern, but couldn't resolve 22nmHP pattern on wafer. This reason was considered to be that the template was not resolved completely. And, above 24nm pattern, it seems there were some differences between the CD-SEM image of template and imprinted pattern. The space pattern on template seems to be wider. There were differences of image between template and imprinted pattern.

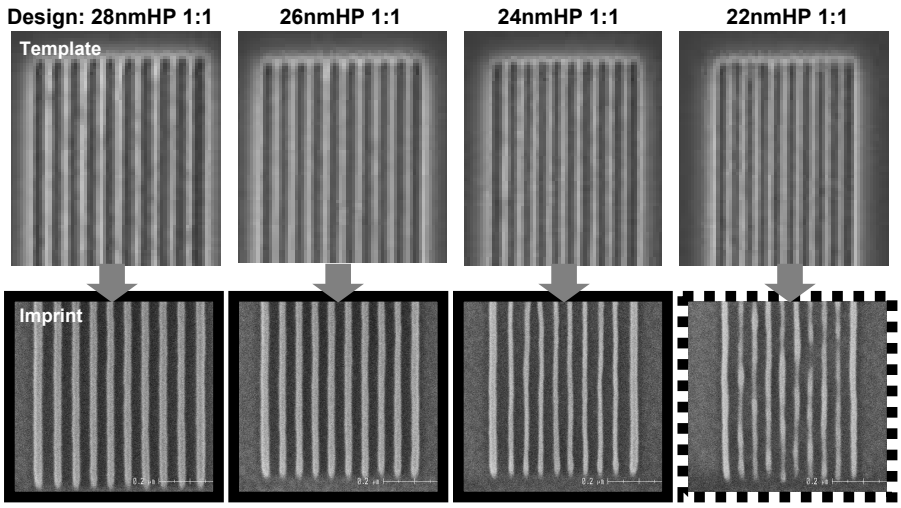


Fig. 2. SEM images of templates and imprint patterns from previous work in early 2007.

In this work, we made new templates.

The templates were patterned with Gaussian beam EB-writer. There are 9 chips in one template shot, and 7 kinds (18, 20, 22, 24, 26, 28, 32, and 42nm-HP) of fine-pattern pitches on each chip.

Figure 3 shows the updated results of template resolution. These are images of imprinted patterns. From 32nm to 22nmHP, pattern could be obtained. However, under 20nmHP, pattern couldn't be obtained.

The reason is that the 20nmHP features were not clearly resolved on the template.

So, further optimization of the template patterning process is required to resolve dense features under 20nmHP.

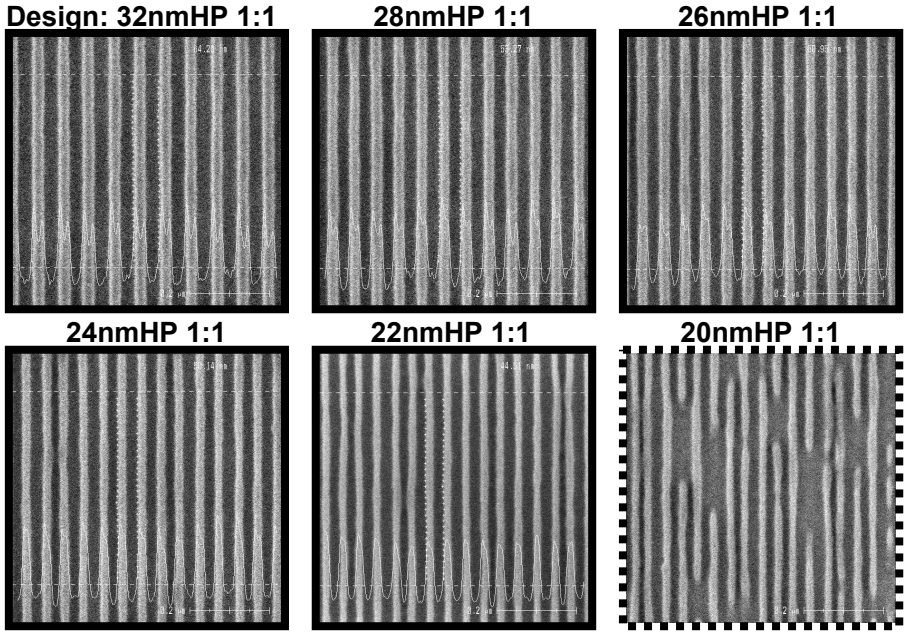


Fig. 3. SEM images of updated imprint patterns.

For CD uniformity evaluation, 5-lines-CDs in all 9 chips of 64 shots were measured. we measured 24nm-HP pattern.

Global CD uniformity was 3s-value of each CD those were averaged CD in each shot, and local CD uniformity was averaged 3s-value of each shot.

In this case, global CD uniformity and local CD uniformity are 0.92 and 3.58, respectively, and as a result, total CD uniformity is 3.69.

It seems almost all total CD errors were induced by the local CD error. Local CD error was induced by template CD error. So, further study of the template process is needed.

Figure 4 shows the results of LER for each designed HP. It seems these results are the same as those in the previous work. And, these results are good enough to compare with LER of photolithography. It seems LER minor depends on the designed hp size. We need to pay attention to the LER of the pattern at smaller feature size. Further improvement of template technology is expected.

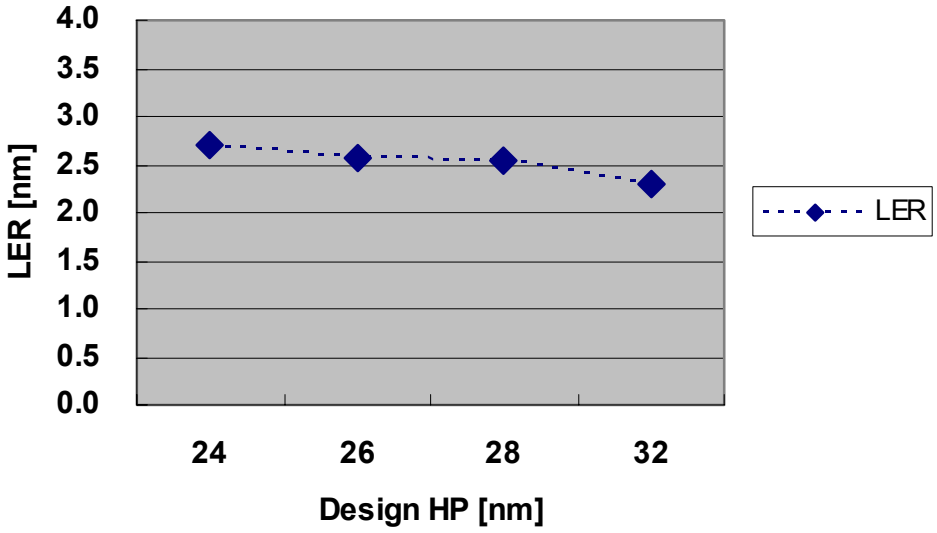


Fig. 4. The LER of imprinted pattern vs. designed pattern pitch.

3.2 Overlay accuracy on multilayer resist

Next, we discuss robustness of OL accuracy.

The tool uses a moiré alignment scheme, illuminated by broadband "white" source. Moiré is formed by interference of light from features on the wafer and template.

The left part of Figure 5 shows the signal level of alignment on single-layer resist.

On single-layer resist system, we had already confirmed that signal level is sufficient for precise alignment and OL accuracy was comparatively good.

On the other hand, as pattern CD shrinks, the multilayer resist is required in order to maintain aspect ratio limitation and etching selectivity.

However, in the multilayer resist system (right part of Figure 5), because of the large absorbance of alignment light in multilayer resist, alignment signal was insufficient.

In this condition, we can't imprint with high OL accuracy.

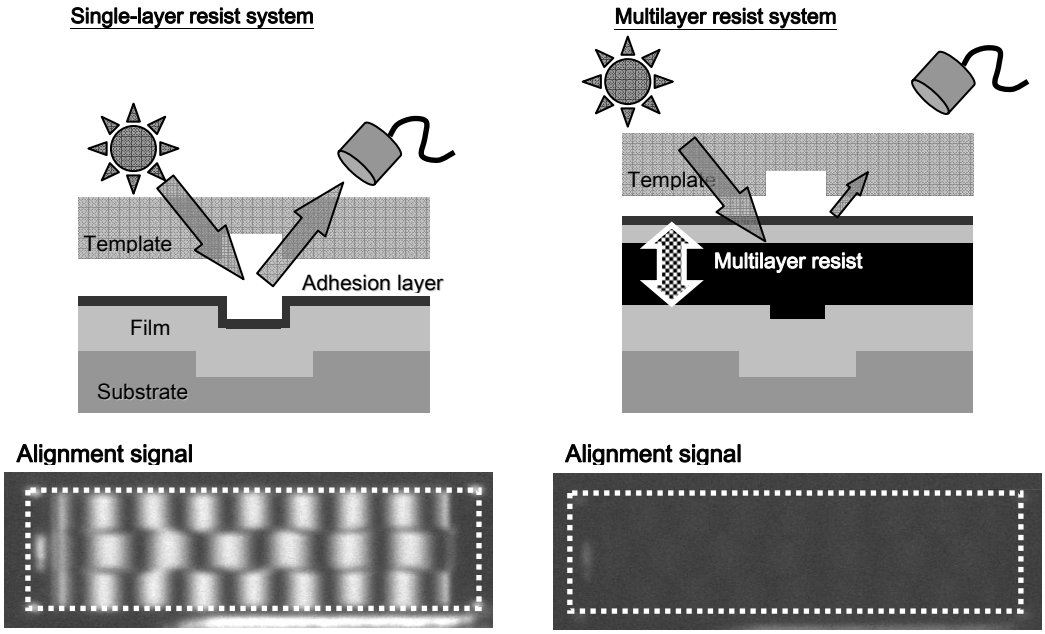


Fig. 5. The signal level difference between single-layer resist system (left) and multilayer resist system (right)

Therefore, we optimized alignment system and checked robustness of the alignment process.

In this work, wavelength and power of light source were optimized (Figure 6), and then signal level became sufficient.

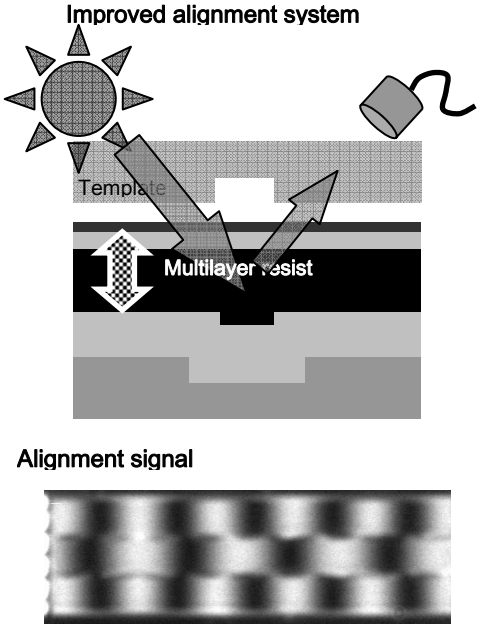
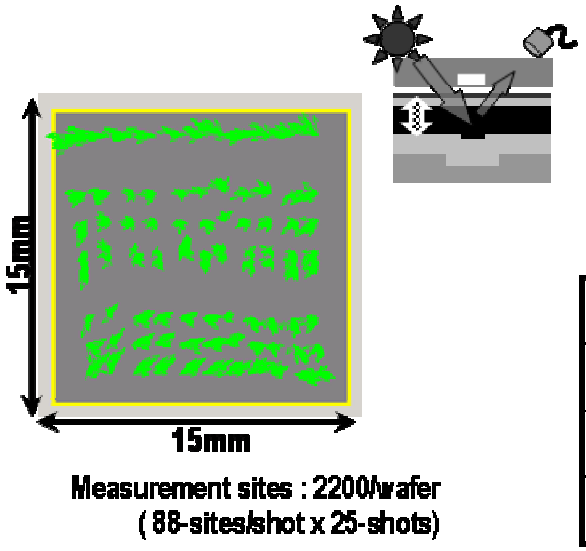


Fig. 6. The signal level of multilayer resist system with improved alignment system.

Figure 7 shows measurement results of NIL to NIL overlay accuracy on multilayer resist system with optimized alignment light source.

As a result, mean plus 3-sigma of OL accuracy are 15.7 and 10.8, respectively.

That is, good OL accuracy can be obtained on multilayer resist and we confirmed the robustness of the overlay accuracy.



	X	Y
Mean	-0.2	-0.4
3σ	15.5	10.4
|Mean|+3σ	15.7	10.8

Fig.7. The result of overlay accuracy on multilayer resist system with improved alignment system.

3.3 Defect density (DD) for various pattern density

Next, we discuss defect density for various pattern densities. We had already evaluated DD caused by imprint process in previous work. Figure 8 shows the feature of the template prepared by MII. The inspection was carried out by KT2800 with two sensitivity modes. That is, the cold inspection (low-sensitivity mode) and the hot inspection (high-sensitivity mode). At an early stage, large numbers of "Non-fill" defects were observed, but we could reduce DD by optimizations of the imprint recipe. Figure 9 is the trend of the reduction of DD. The template has a wide variety of feature densities ranging from ~10-50%. However, there is no feature density above 50%.

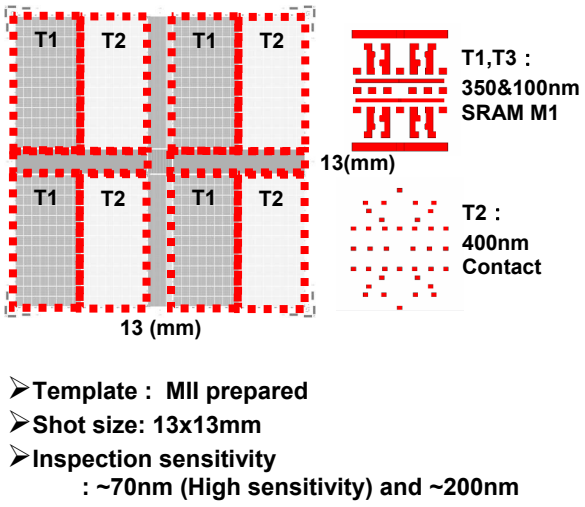


Fig. 8. The template features of previous work

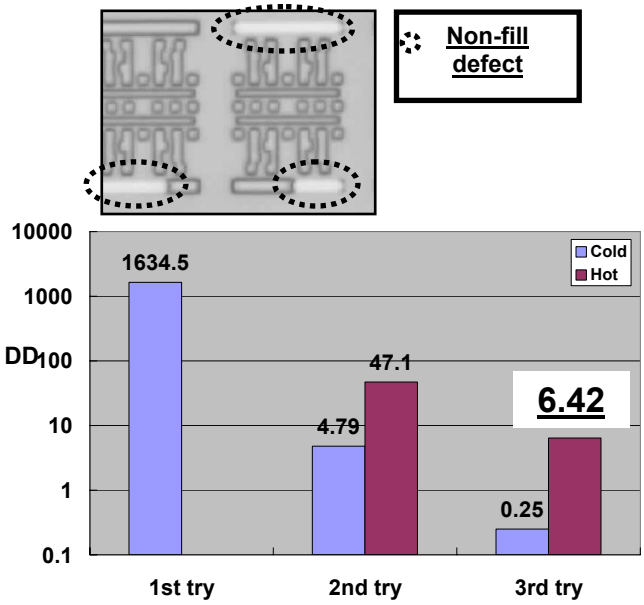


Fig. 9. DD reduction of previous work

On the other hand, there are many pattern variations for real devices.

So, we evaluated DD dependences on the pattern density. In this work, two types of pattern templates were prepared: metal-layer template and via-layer template (Figure 10). Pattern densities of metal-layer and via-layer are approximately 50% and almost 100%, respectively.

In this work, DD was evaluated for two templates with various spread times. The inspection was also carried out by KT2800 with die-to-die mode.

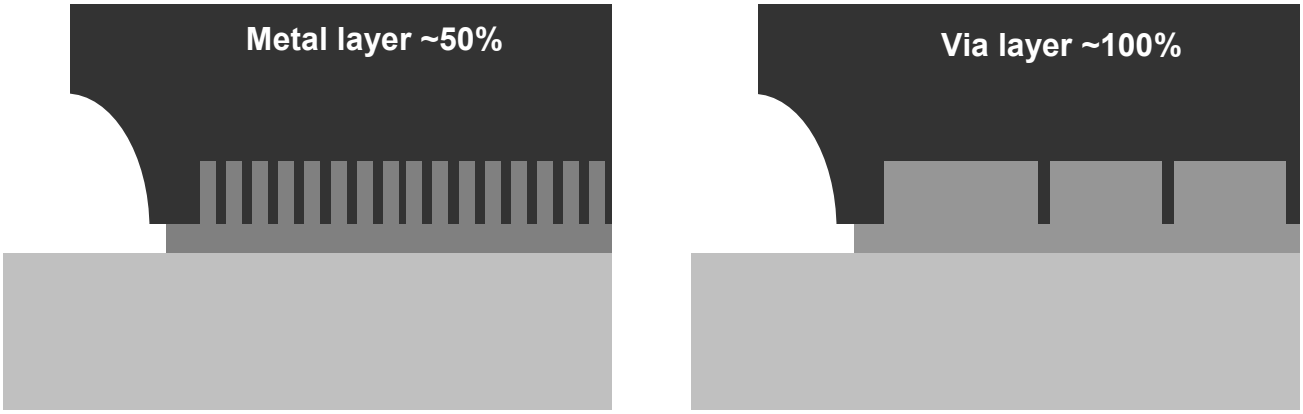


Fig. 10. DD reduction of previous work

Figure 11 shows the results of spread time vs. defect density of imprint patterns by two templates.

It seems, for metal layer, DD reduced in inverse proportion to longer spread time. However, for via layer, it was difficult to reduce non-fill defects. So, longer spread time is required for via layer to reduce DD.

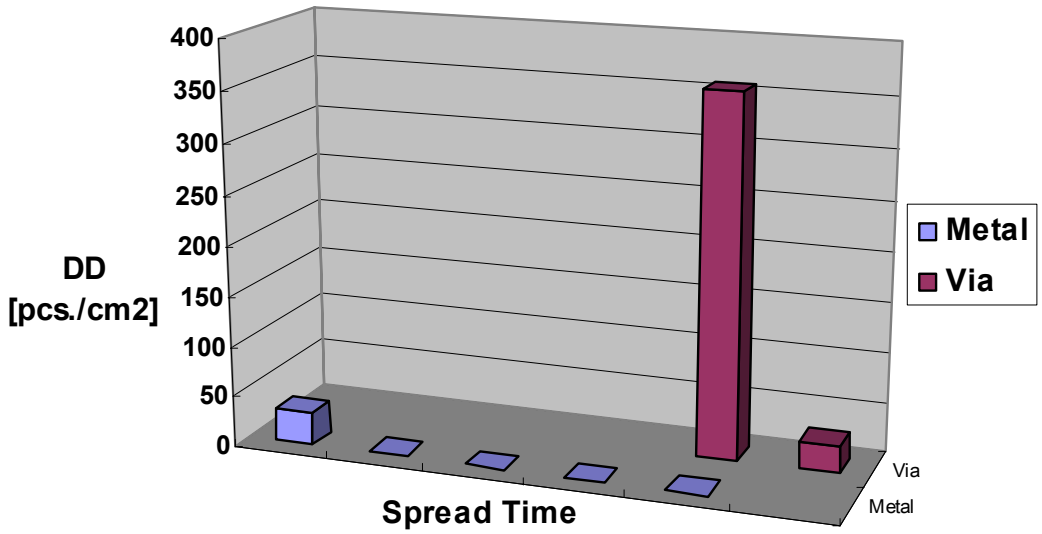


Fig. 11. DD vs. spread time by P1 and P2 imprint

Figure 12 shows the speculation as to the reason for defect density difference between metal layer and via layer.

In the metal-layer case, gas trapped minimized by vent routes formed by small features. On the other hand, in the via-layer case, large features trap larger gas volumes, so that gas dissipation is slower. As a result, the spread of metal layer is faster than that of via layer.

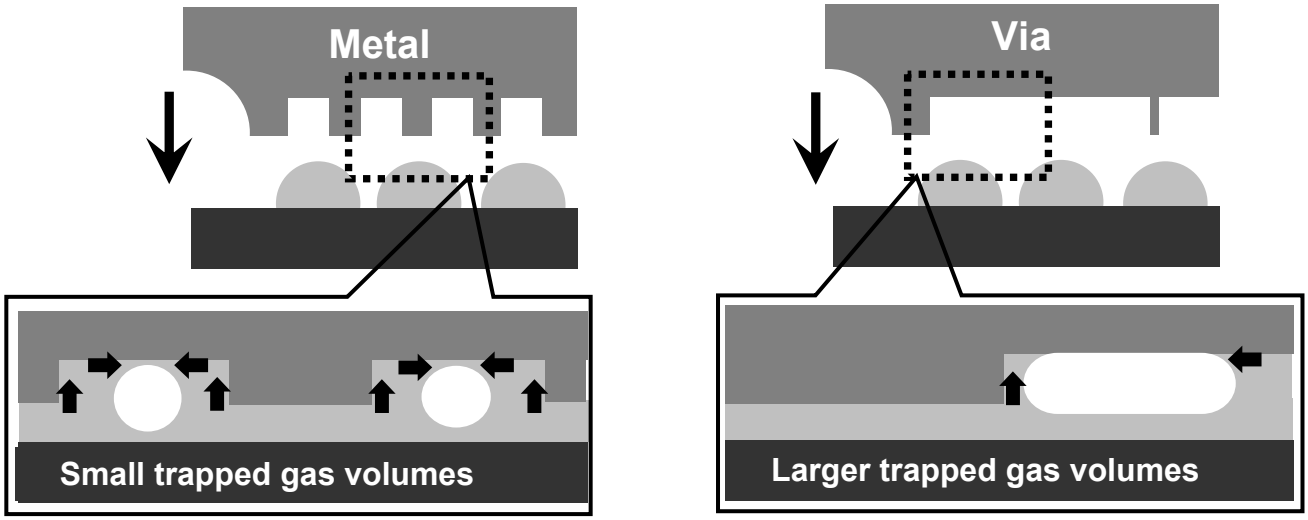


Fig. 12. Schematic drawing illustrating speculation of the reason for DD difference

However, longer spread time causes throughput loss. It is important to reduce DD without throughput loss.

Therefore, various evaluations were carried out and several solutions have been proposed.

One of the solutions proposed by MII is inclined template geometry creating a fluid wavefront to avoid trapping of air between liquid drops. According to a recent study at MII, DD become less than 1p/cm2 for shorter spread time.

4. CONCLUSIONS

As a result of evaluation, nanoimprint application is found to be extendable to fabrication of various test devices. Template resolution is improved and 22nmHP dense pattern is obtained. We confirmed robustness of OL accuracy. On the other hand, reduction of DD without throughput loss is required for application of next step.

From the discussion of this work, although we have shown results with respect to CD uniformity, overlay accuracy, and defectivity, further improvements are still required.

To extend the use of nanoimprint lithography, additional efforts are needed by tool vendors, in the imprint resist, and in the template.

We look forward to seeing these solutions implemented in the future.

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